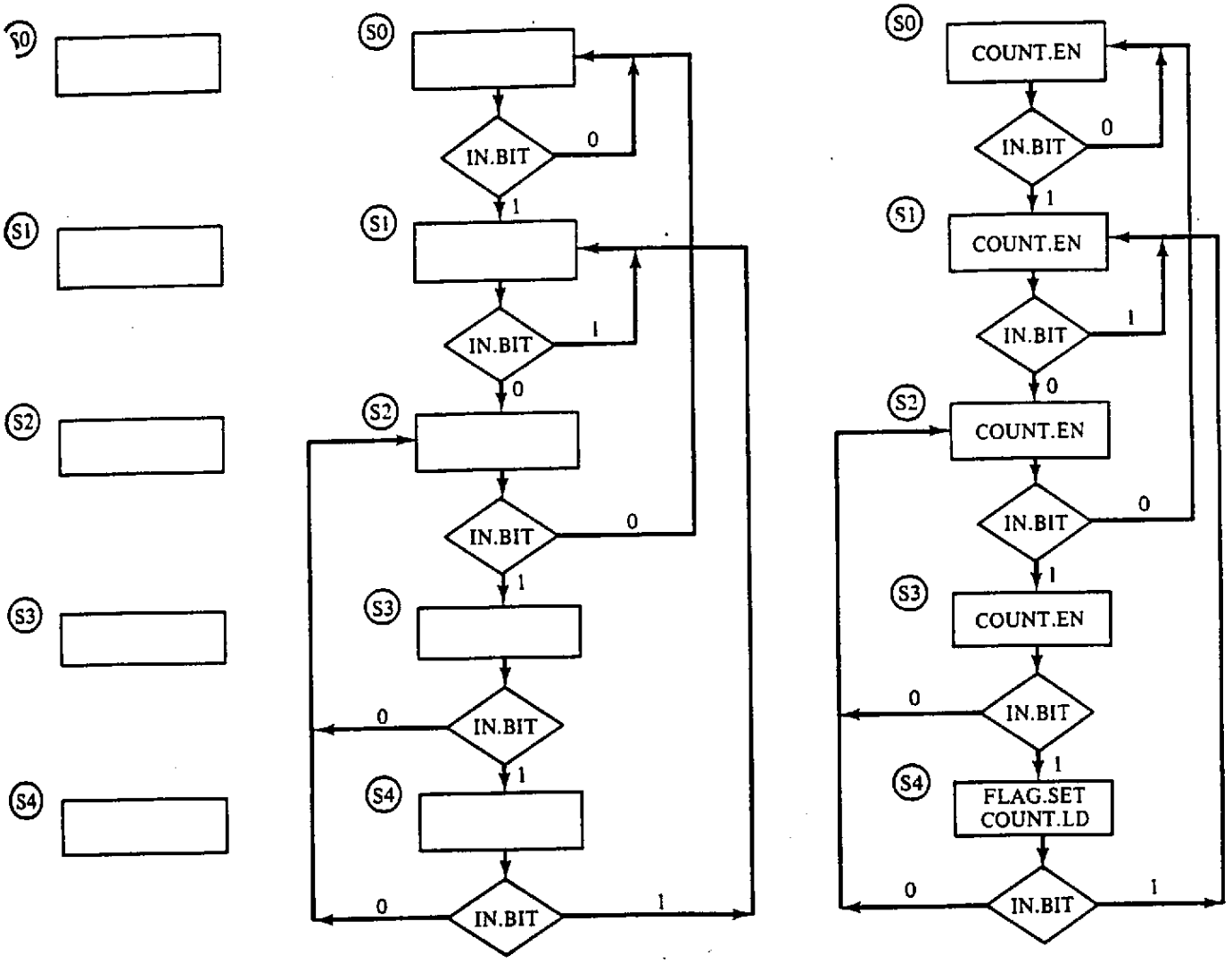


(a) Identification of states (b) Specification of state transitions (c) Specification of control outputs

Figure 7.29 Development of the ASM chart for the controller.

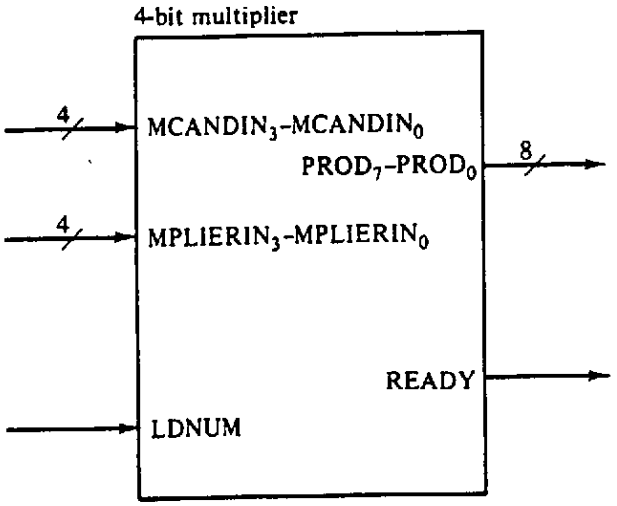
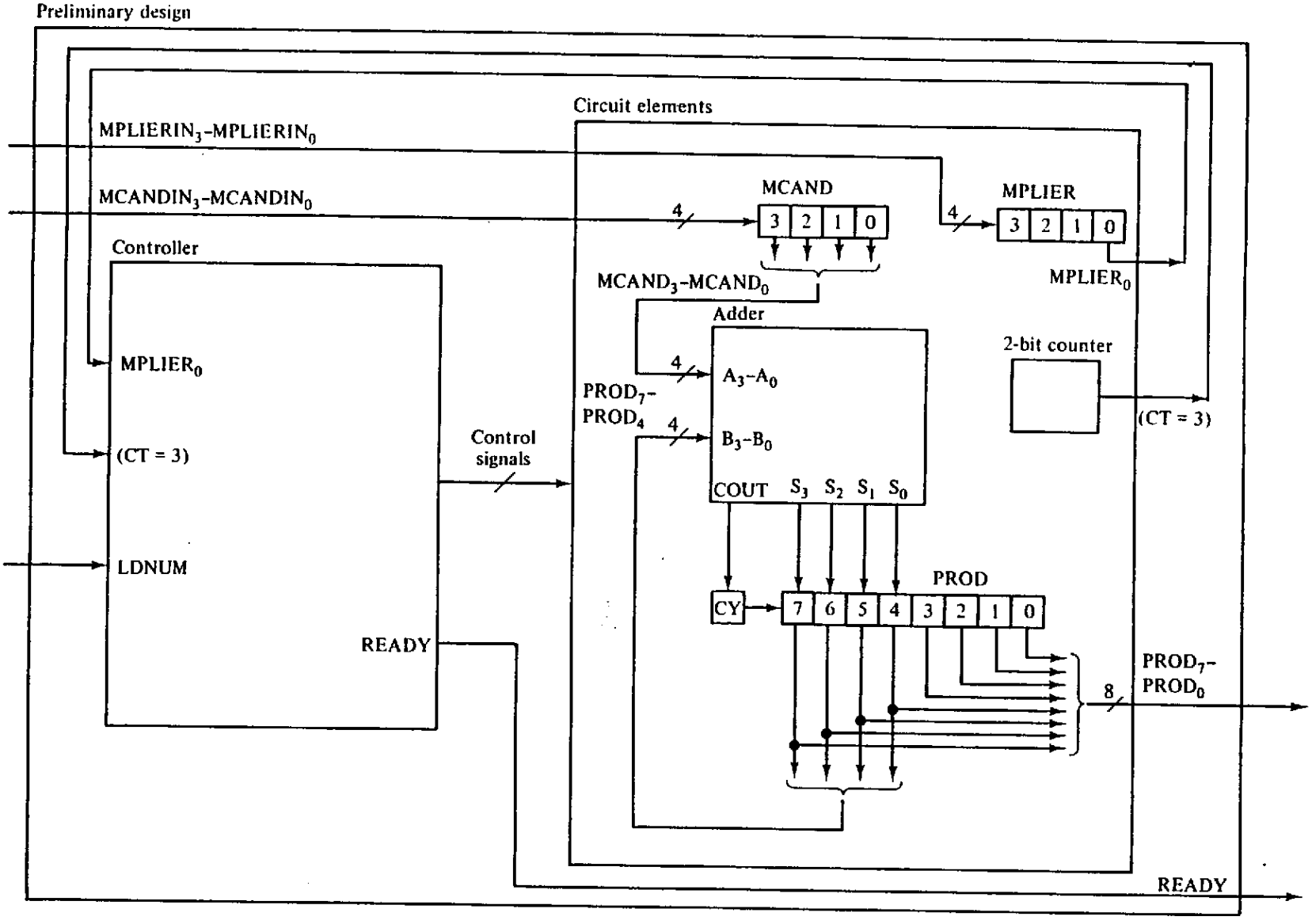
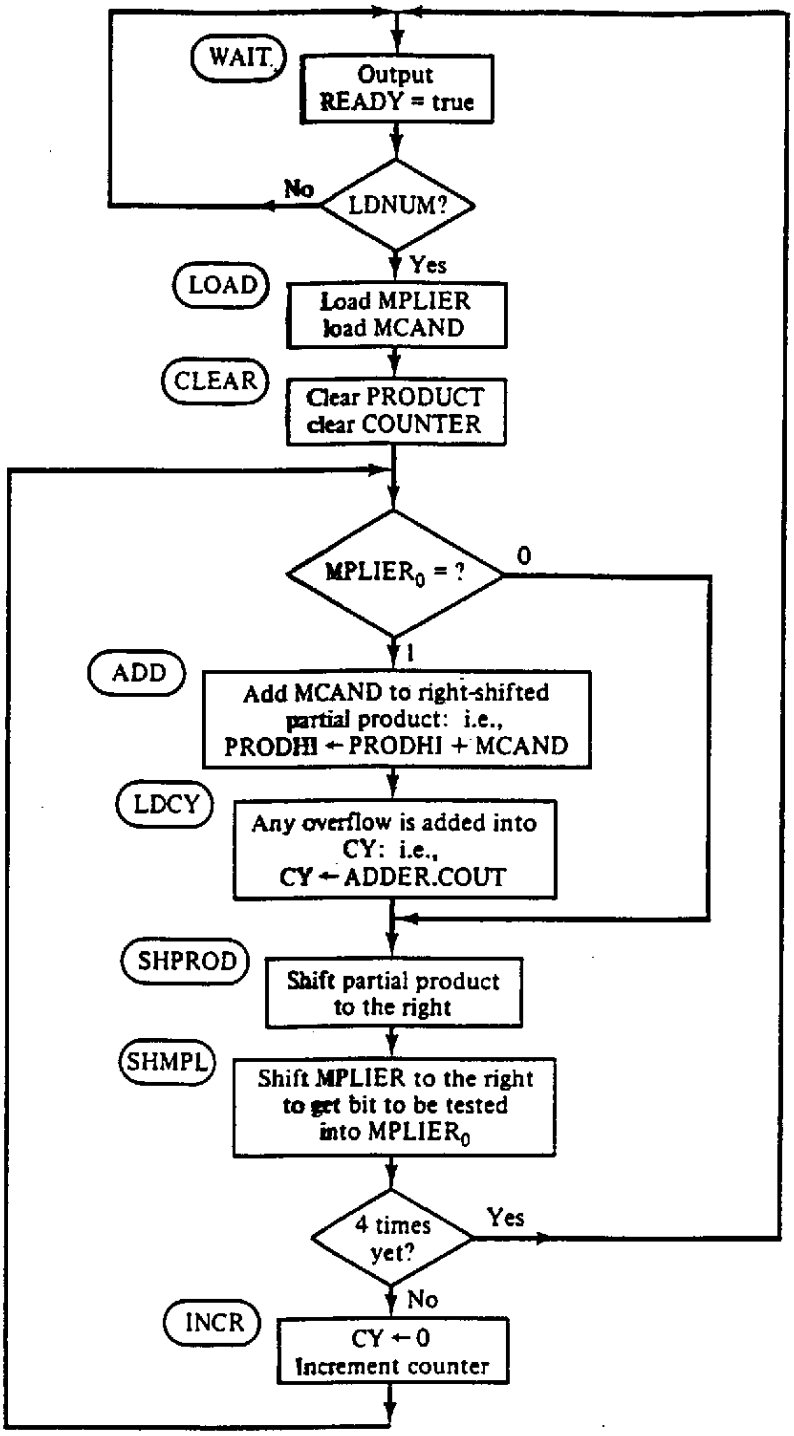


Figure 7.30 Block diagram of the multiplier.



(a) Block diagrams of the circuit elements and the controller

Figure 7.32 Prelifminary design of the multiplier circuit.



(b) Flowchart for the controller

Figure 7.32 *(cont.)*

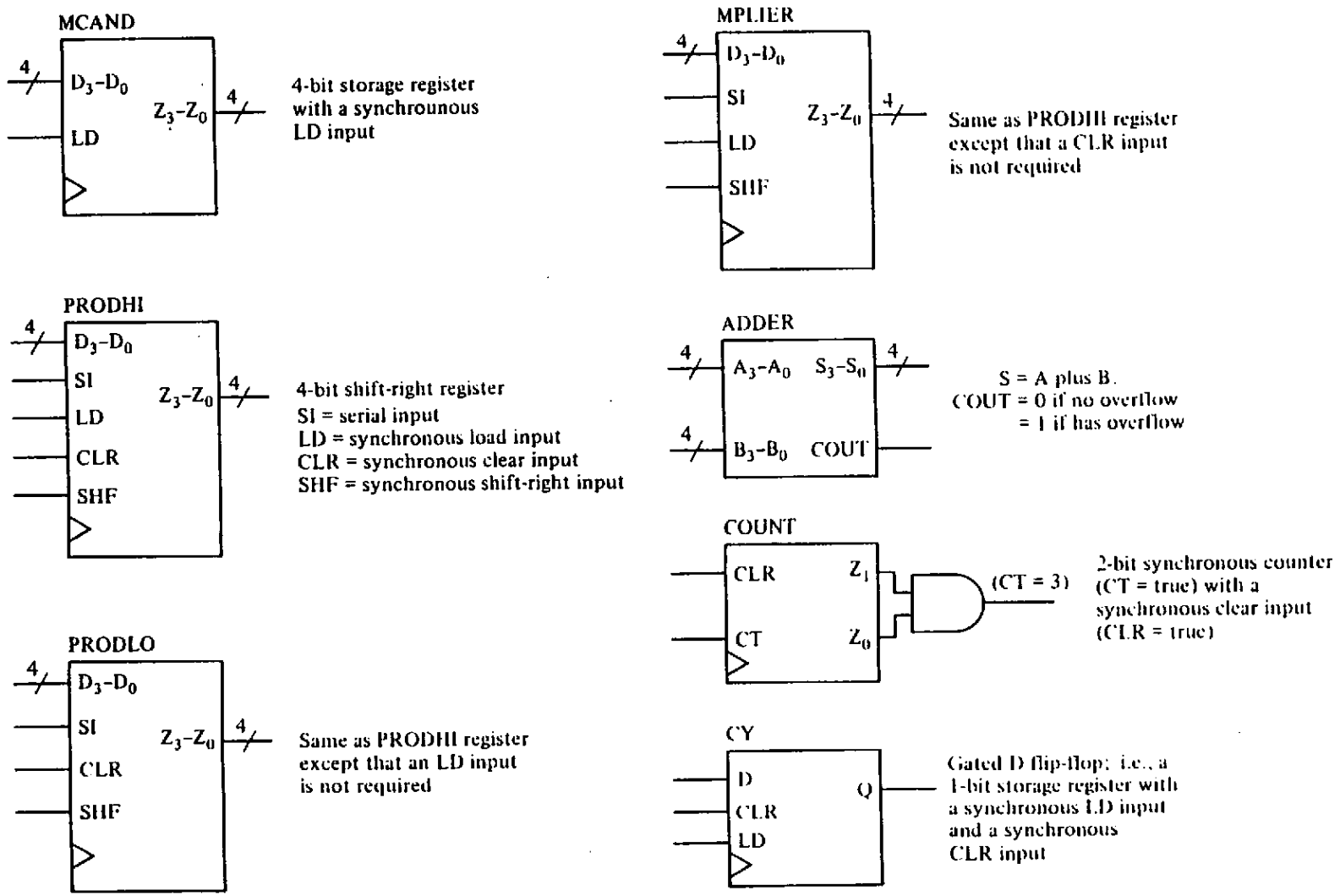
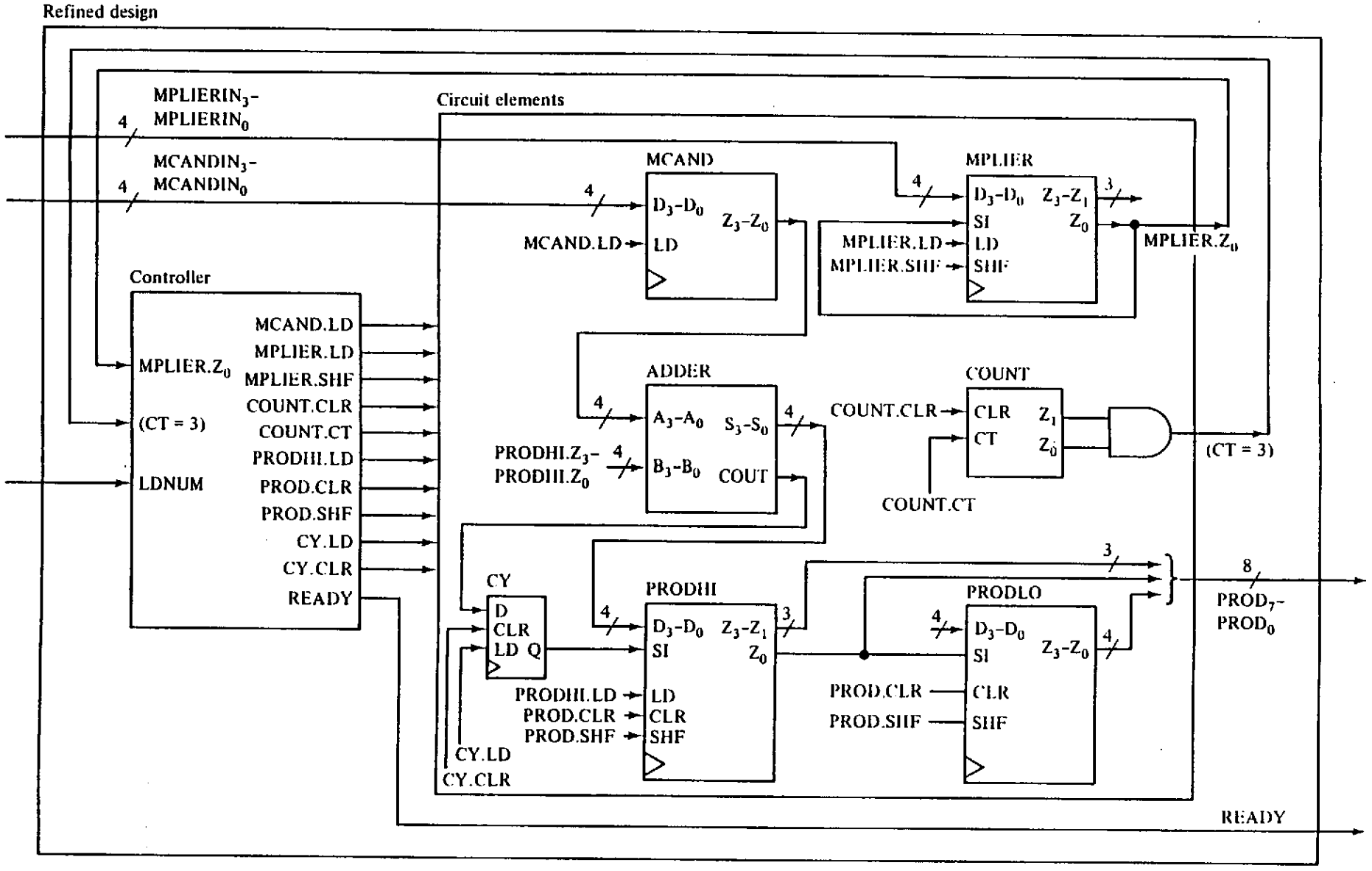
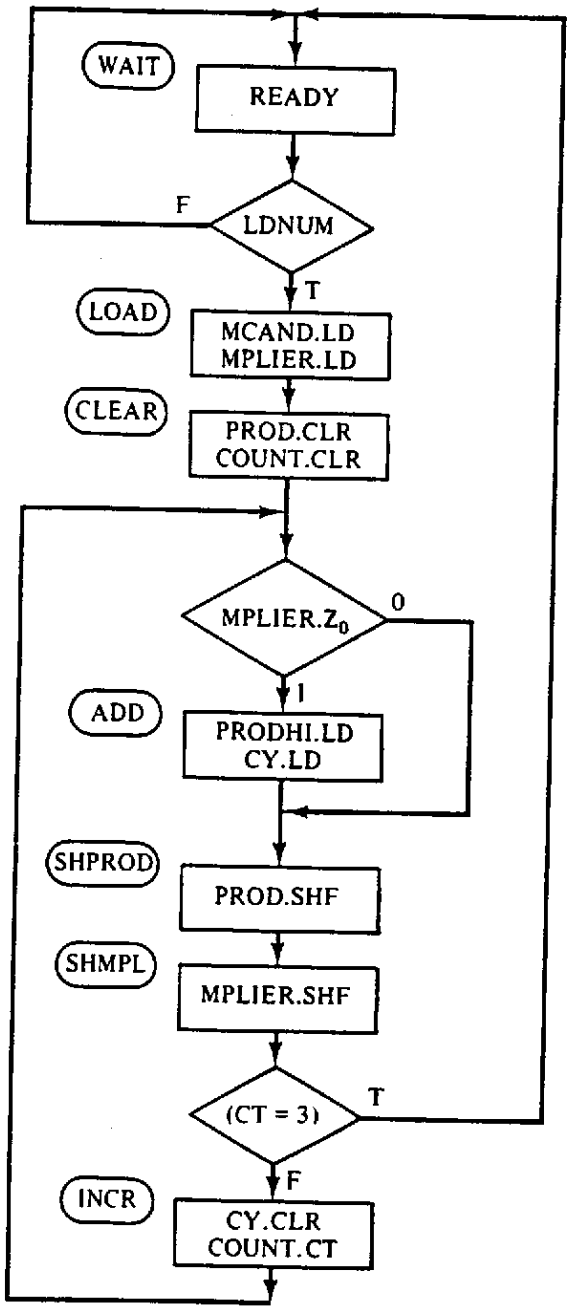


Figure 7.33 Detailed specifications for the circuit elements.



(a) Block diagram of the circuit elements and the controller

Figure 7.34 Refined design of the multiplier circuit.



(b) ASM chart for the controller

Figure 7.34 *(cont.)*

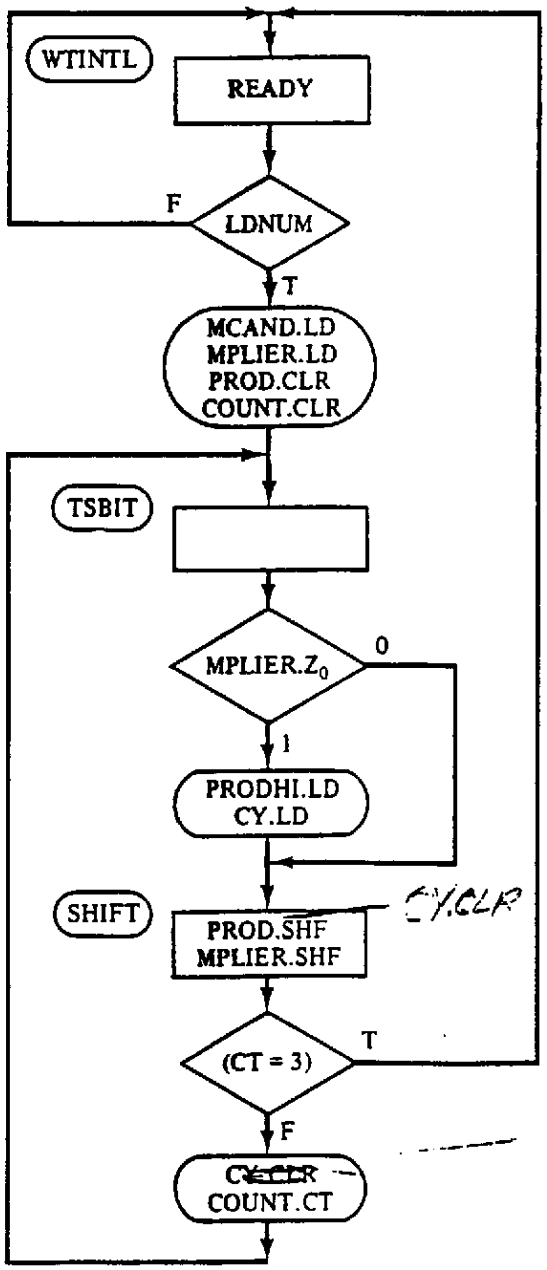
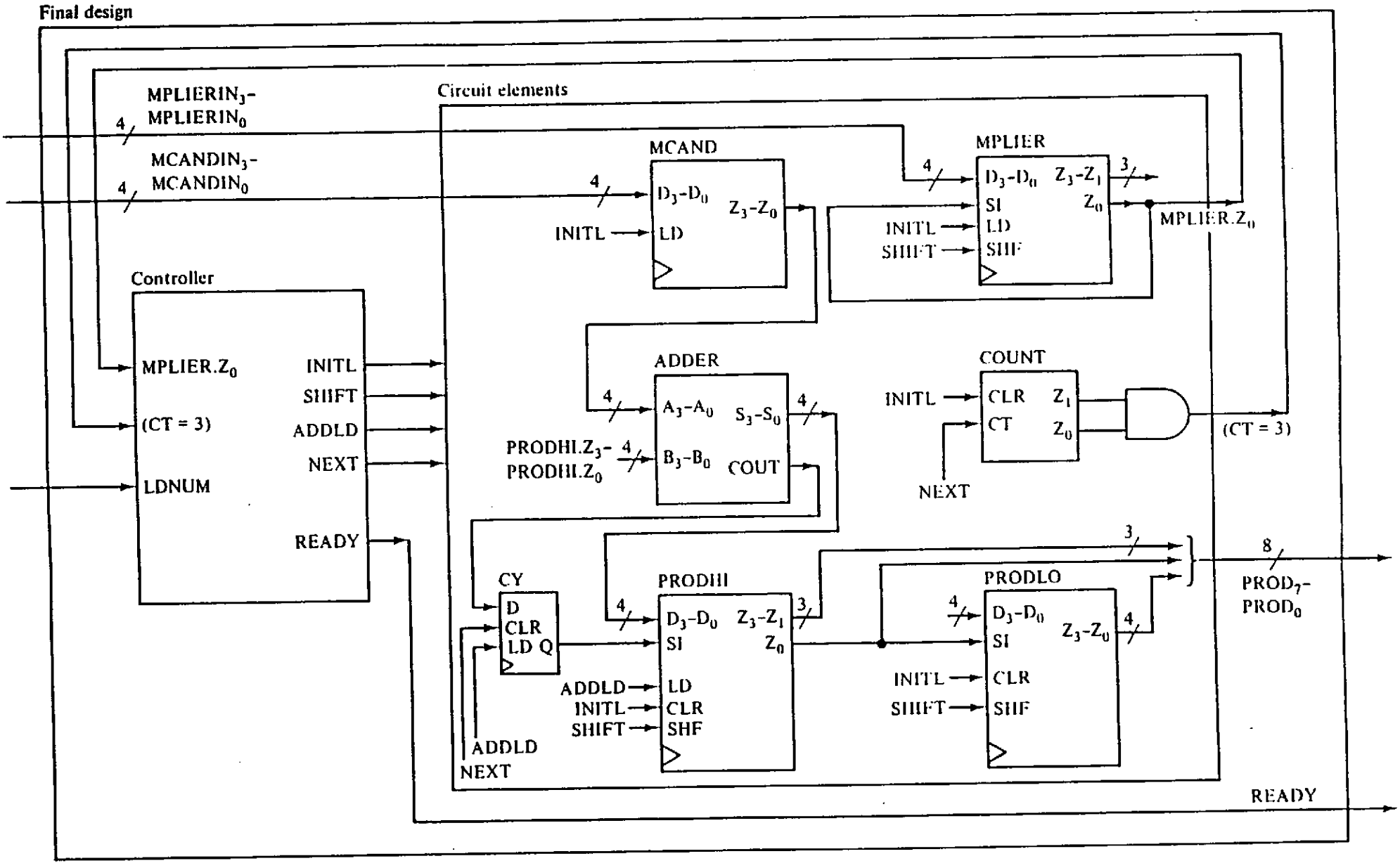
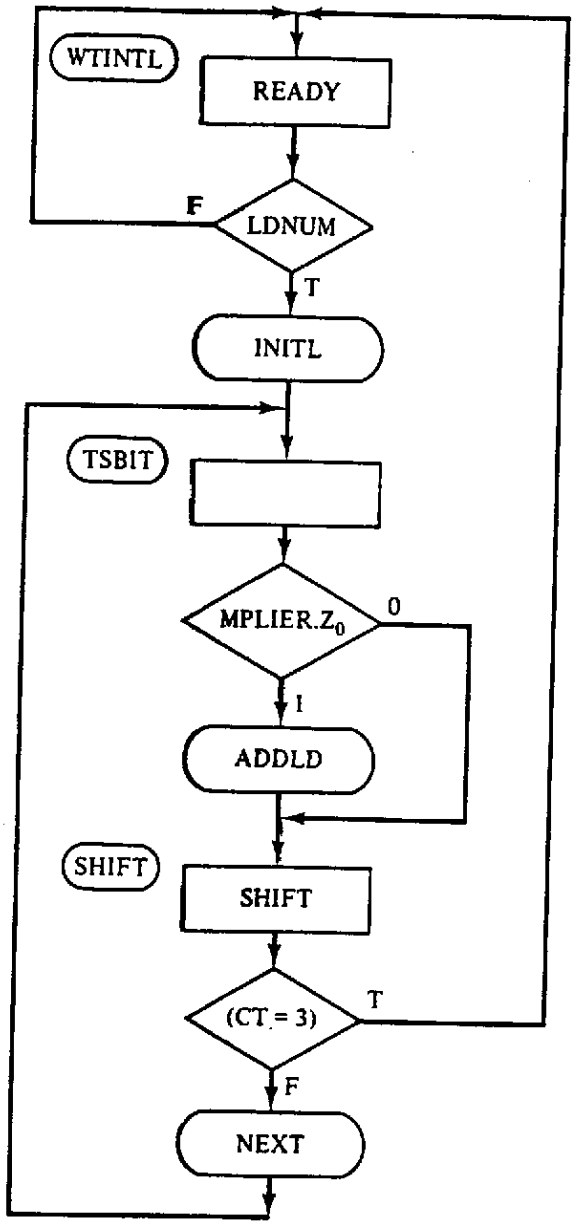


Figure 7.35 Refinement of the ASM chart for the controller.



(a) Circuit elements and the controller

Figure 7.36 Final design for the multiplier circuit.



(b) ASM chart for the controller

Figure 7.36 *(cont.)*

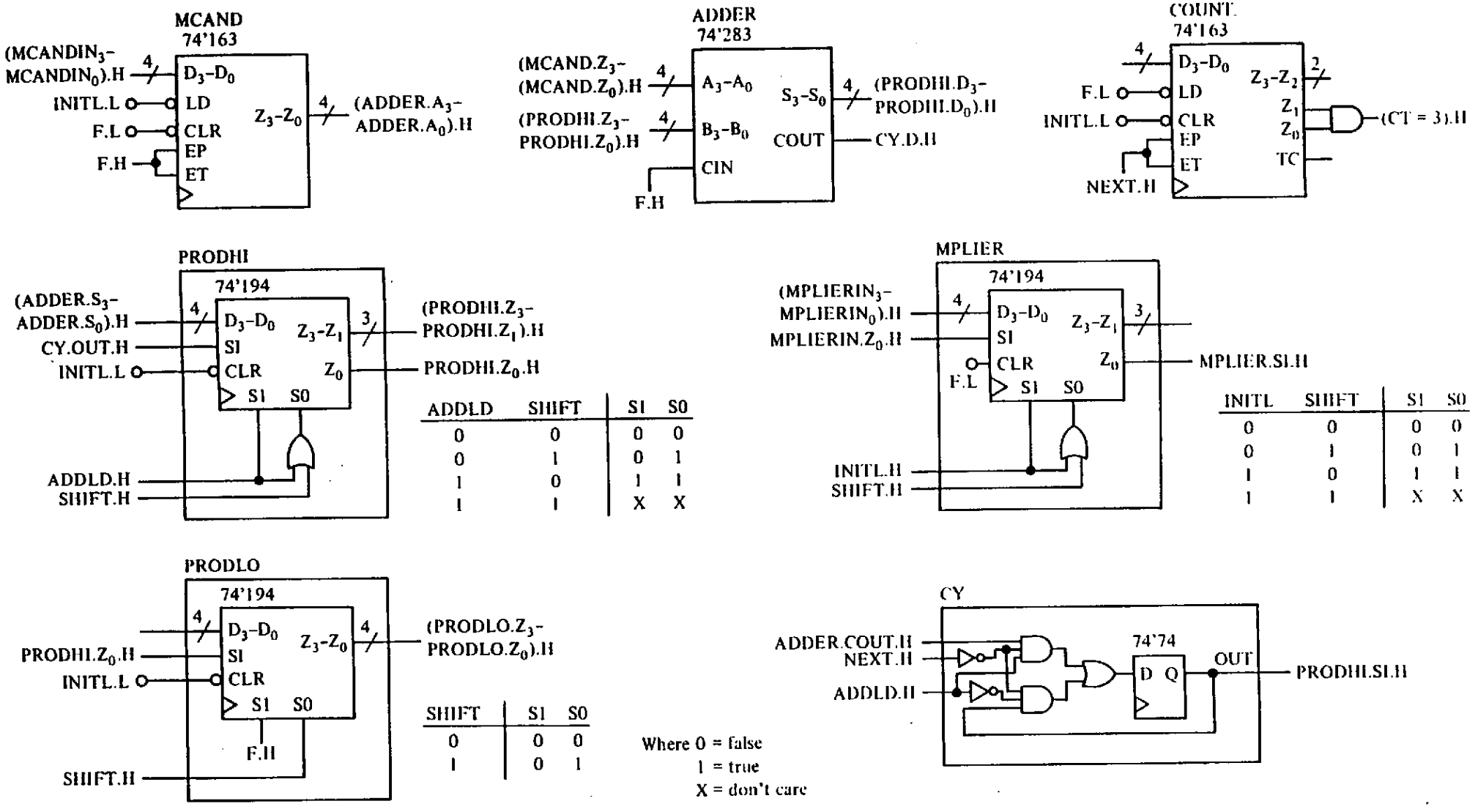
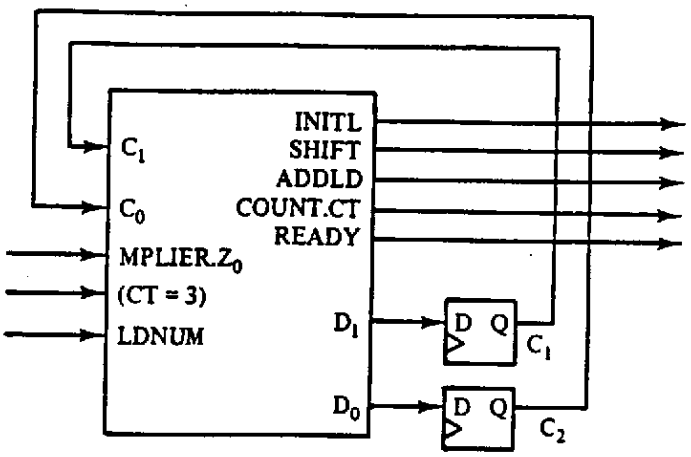


Figure 7.37 Realization of the circuit elements.



State assignments:

	C_1	C_0
WTINIT	0	0
TSBIT	0	1
SHIFT	1	0

(a) Block diagram and state assignment

present state		inputs			outputs					next state		D flip-flop inputs	
C_1	C_0	MPLIER.Z_0	(CT = 3)	LDNUM	INITL	SHIFT	ADDLD	COUNT.CT	READY	C_1^+	C_0^+	D_1	D_0
0	0	X	X	0	0	0	0	0	1	0	0	0	0
0	0	X	X	1	1	0	0	0	1	0	1	0	1
0	1	0	X	X	0	0	0	0	0	1	0	1	0
0	1	1	X	X	0	0	1	0	0	1	0	1	0
1	0	X	0	X	0	1	0	1	0	0	1	0	1
1	0	X	1	X	0	1	0	0	0	0	0	0	0
1	1	X	X	X	0	0	0	0	0	0	0	0	0

Where 0 = false
1 = true
X = don't care

(b) Next-state and output table

Figure 7.38 Outline of the realization of the controller.