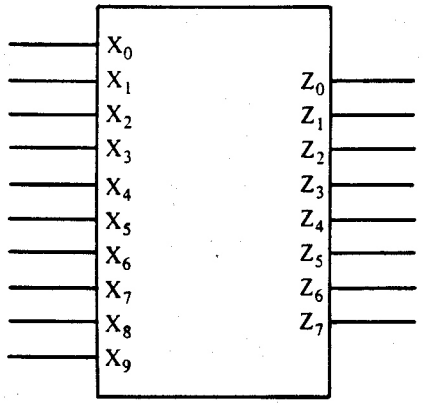
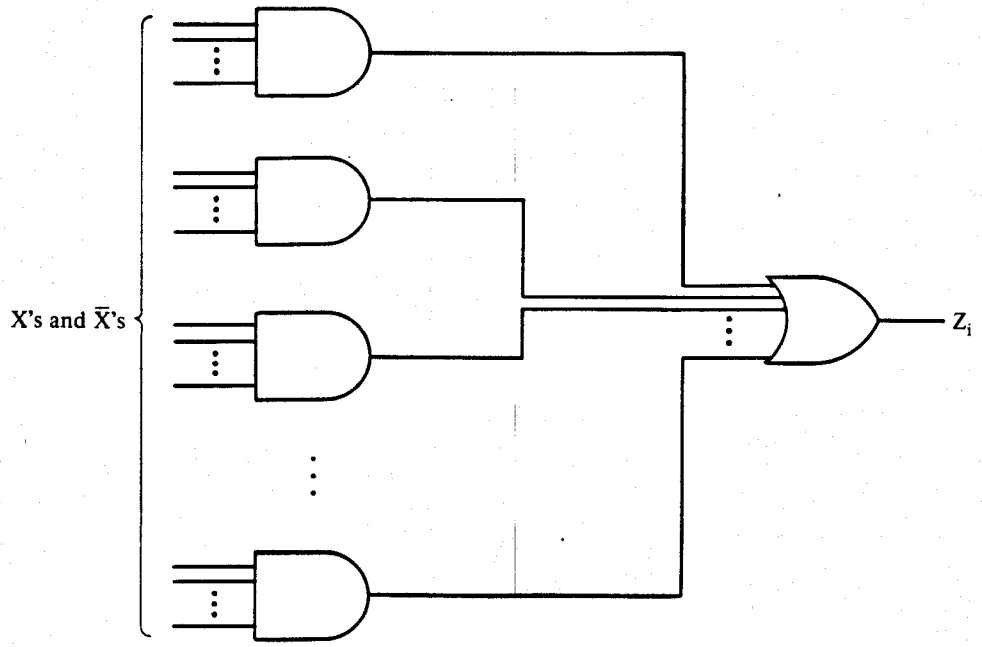
$$Z_i = f(X_0, X_1, X_2, \ldots, X_9)$$

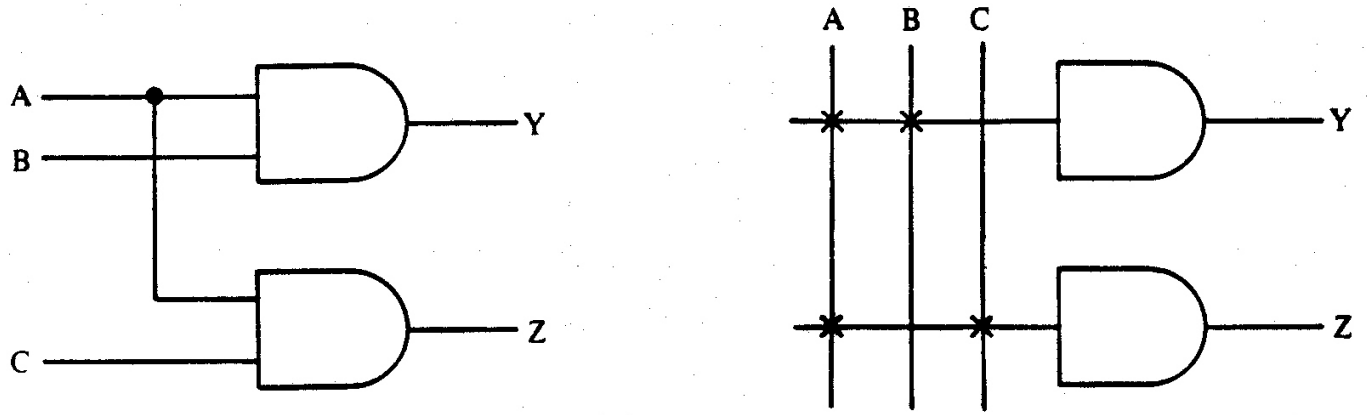


(a) Functional block diagram

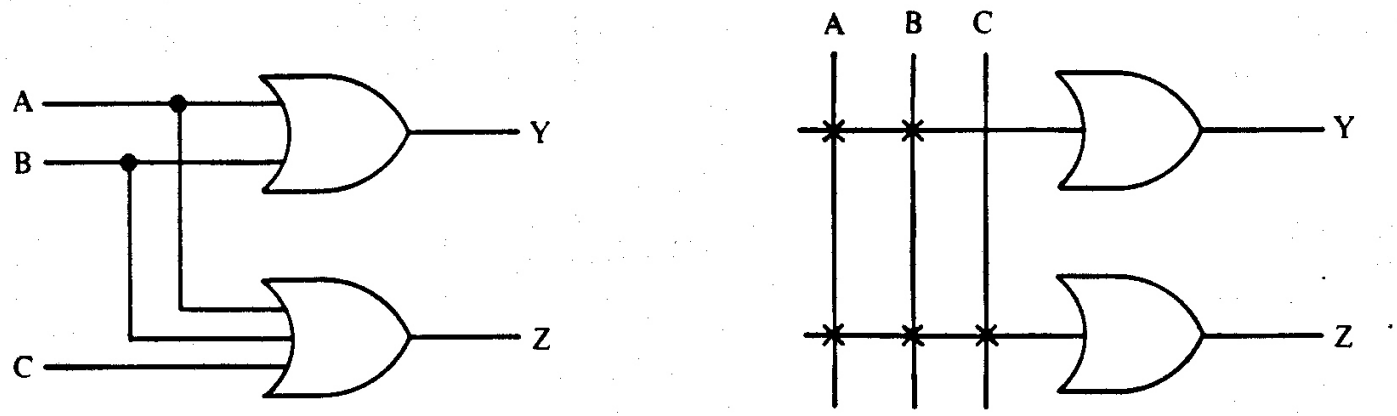


(b) Two-level AND-OR structure

Figure 6.8 Conventional realization of a multiinput and multioutput circuit.



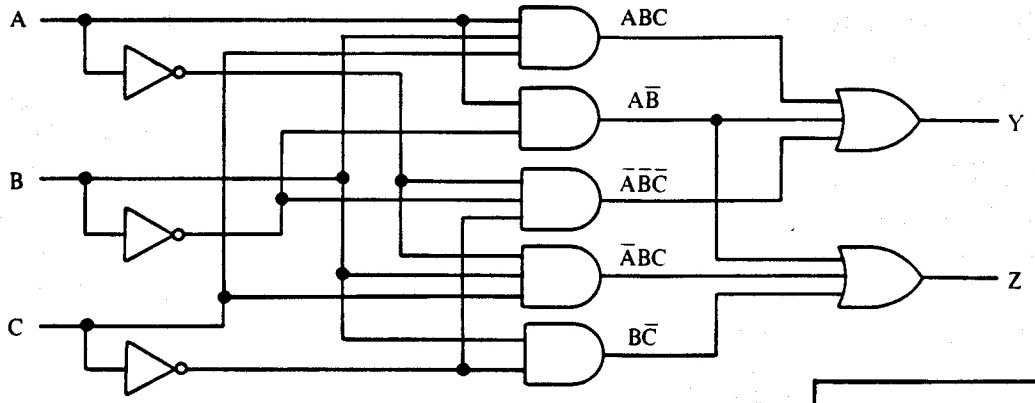
(a) AND gates



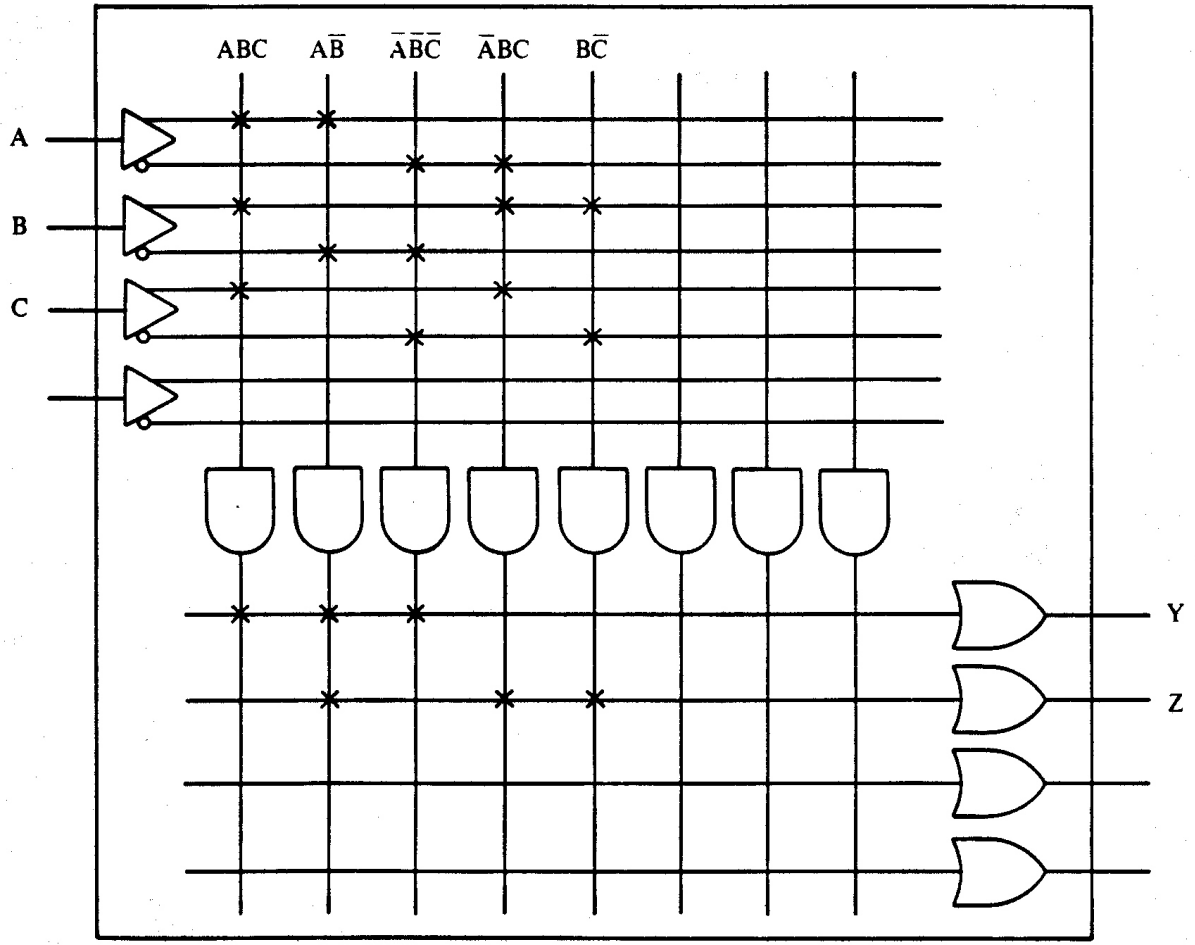
(b) OR gates

(c) Inverter

Figure 6.9 Equivalent PLA logic diagrams.

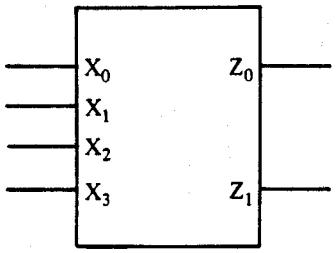


(a) Common circuit diagram



(b) PLA circuit diagram

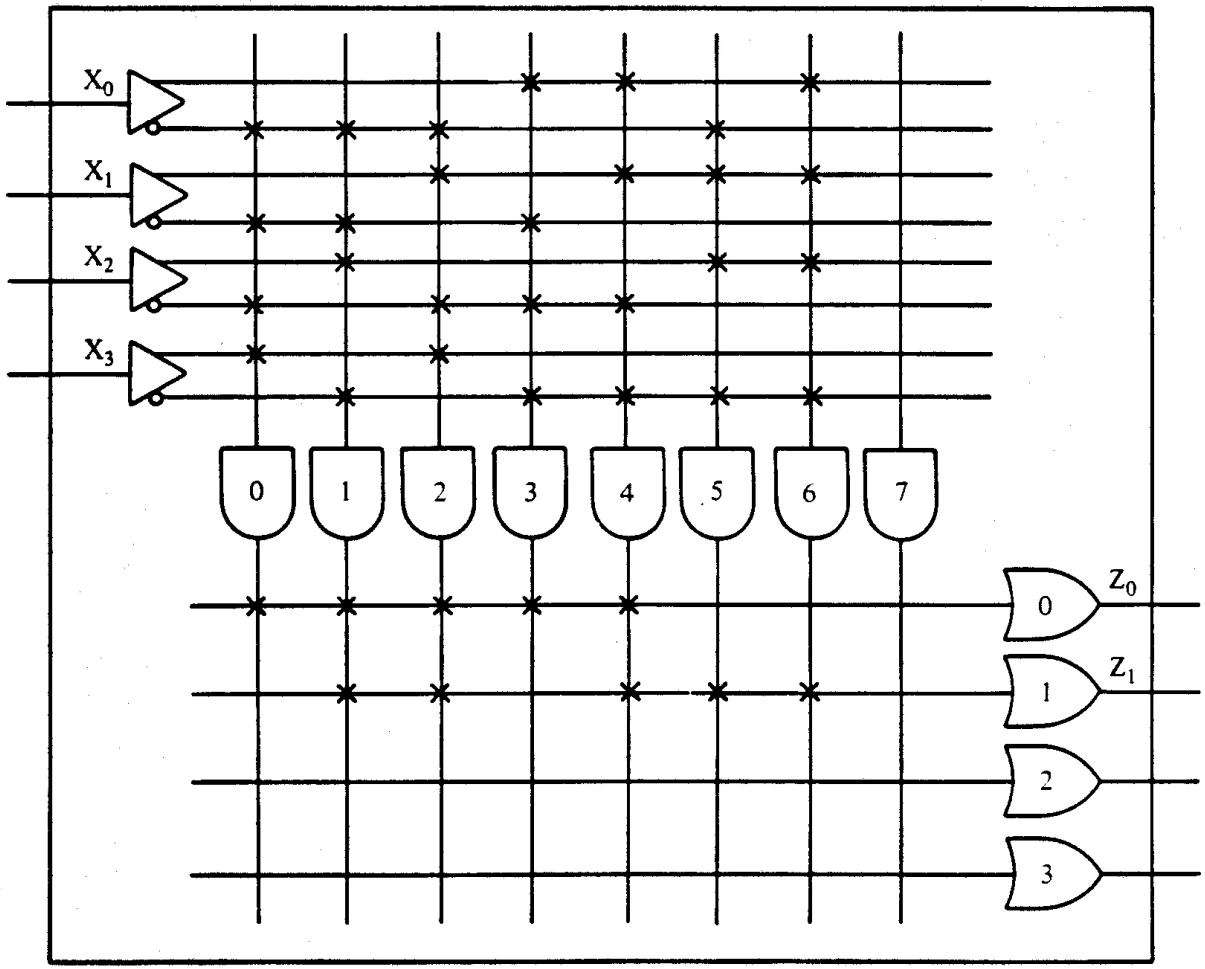
Figure 6.10 PLA circuit diagram for Example 6.1.



(a) Functional block diagram

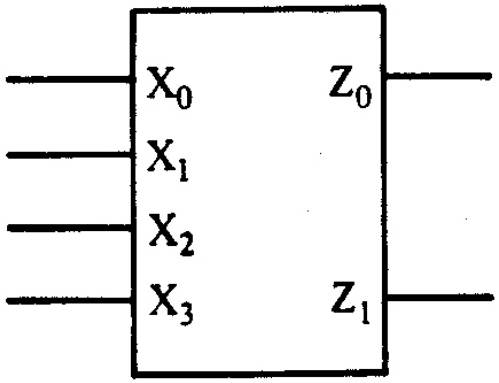
X_0	X_1	X_2	X_3	Z_0	Z_1
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	1	0	0	1
1	1	1	1	0	0

(b) Truth table



(c) PLA realization

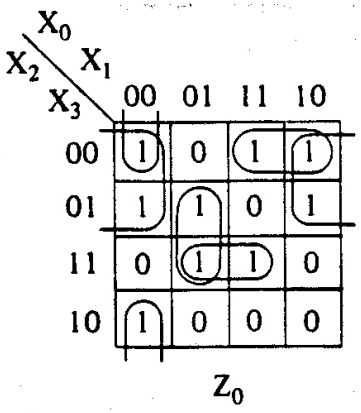
Figure 6.11 Illustration for Example 6.2.

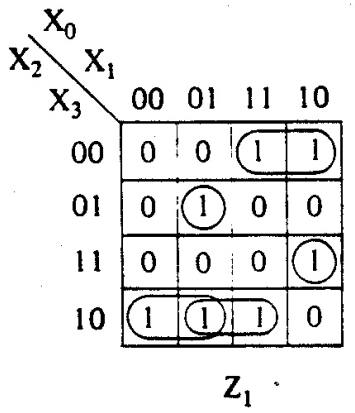


(a) Functional block diagram

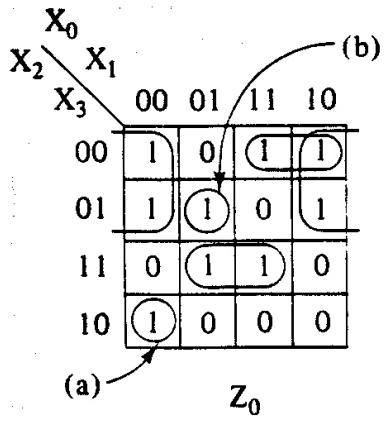
X_0	X_1	X_2	X_3	Z_0
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

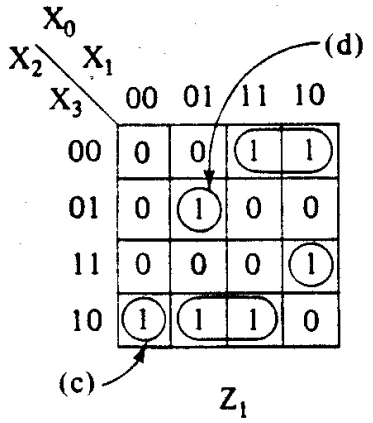
(b) Truth table





(c) Conventional minimization results in a total of nine distinct AND terms





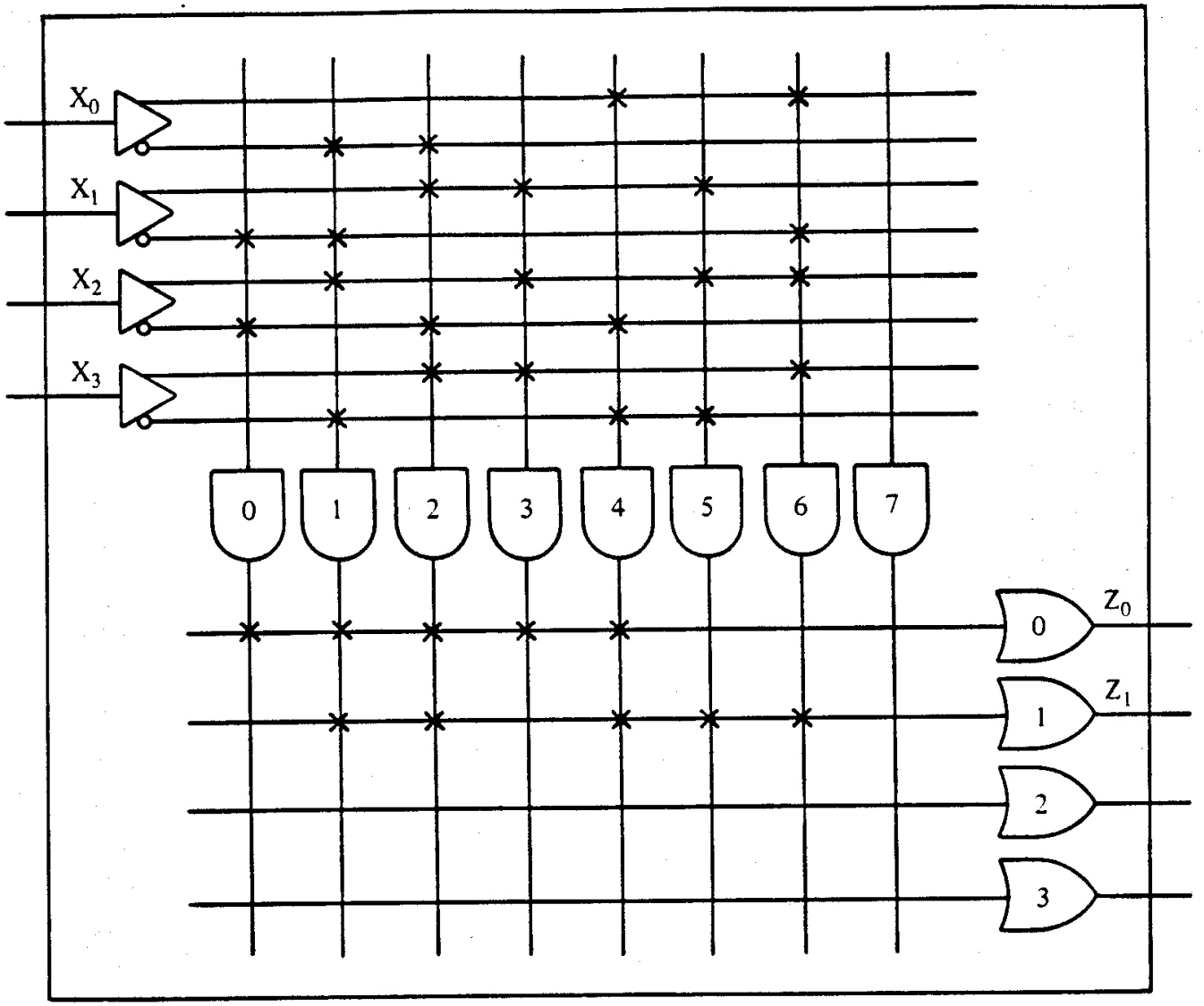
$$Z_0 = \bar{X}_1\bar{X}_2 + \bar{X}_0\bar{X}_1X_2\bar{X}_3 + \bar{X}_0X_1\bar{X}_2X_3 + X_1X_2X_3 + X_0\bar{X}_2\bar{X}_3$$
$$Z_1 = \bar{X}_0\bar{X}_1X_2\bar{X}_3 + \bar{X}_0X_1\bar{X}_2X_3 + X_0\bar{X}_2\bar{X}_3 + X_1X_2\bar{X}_3 + X_0\bar{X}_1X_2X_3$$

(d) Minimization for PLA realization – a total of seven distinct AND terms

Figure 6.12 Illustration for Example 6.3.

$$Z_0 = \bar{X}_1 \bar{X}_2 + \bar{X}_0 \bar{X}_1 X_2 \bar{X}_3 + \bar{X}_0 X_1 \bar{X}_2 X_3 + X_1 X_2 X_3 + X_0 \bar{X}_2 \bar{X}_3$$

$$Z_1 = \bar{X}_0 \bar{X}_1 X_2 \bar{X}_3 + \bar{X}_0 X_1 \bar{X}_2 X_3 + X_0 \bar{X}_2 \bar{X}_3 + X_1 X_2 \bar{X}_3 + X_0 \bar{X}_1 X_2 X_3$$



(e) PLA realization

Figure 6.12 *(cont.)*

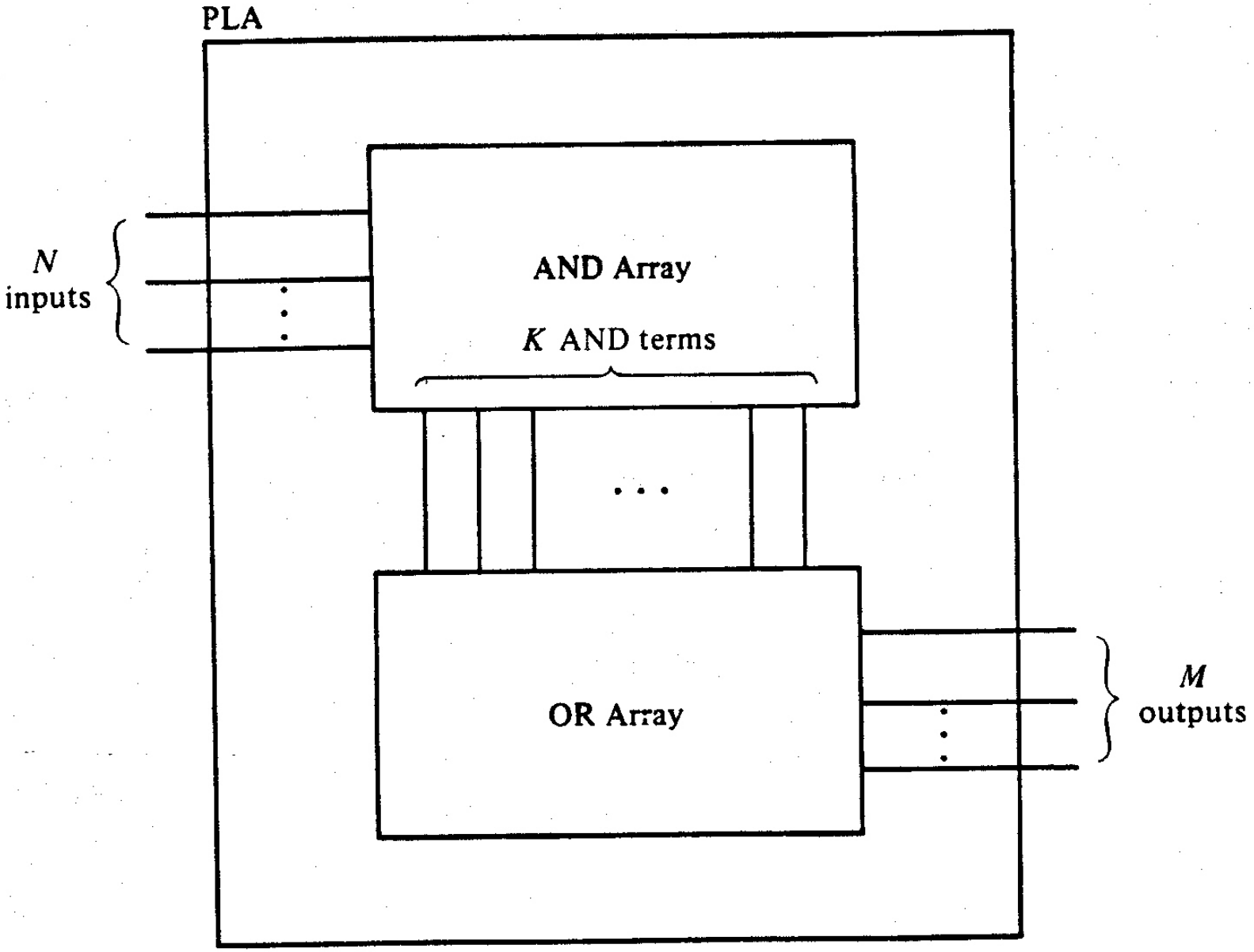
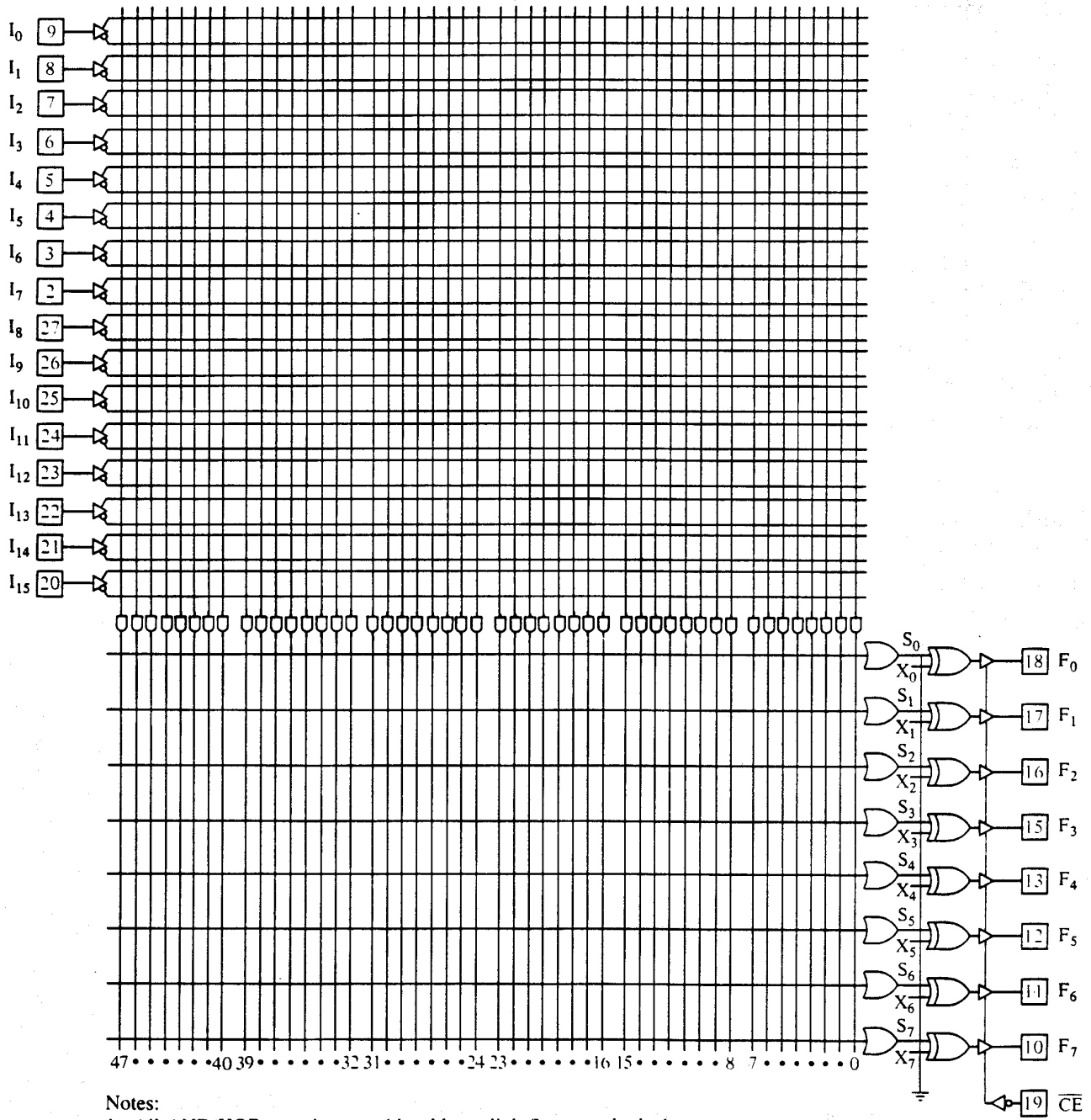
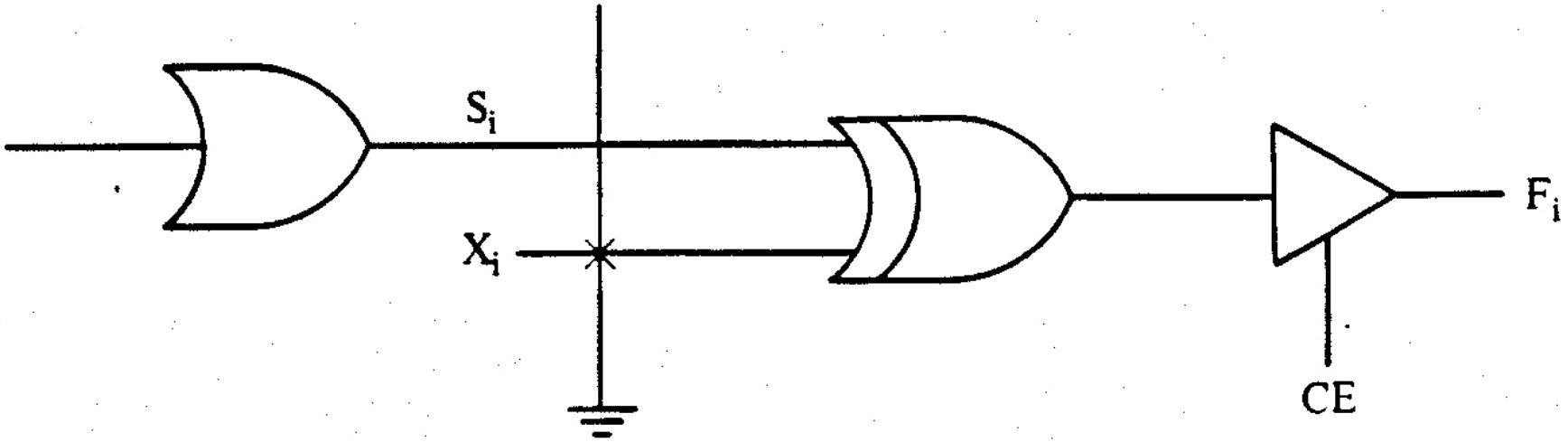


Figure 6.13 PLA with N inputs, M outputs, and K AND terms.

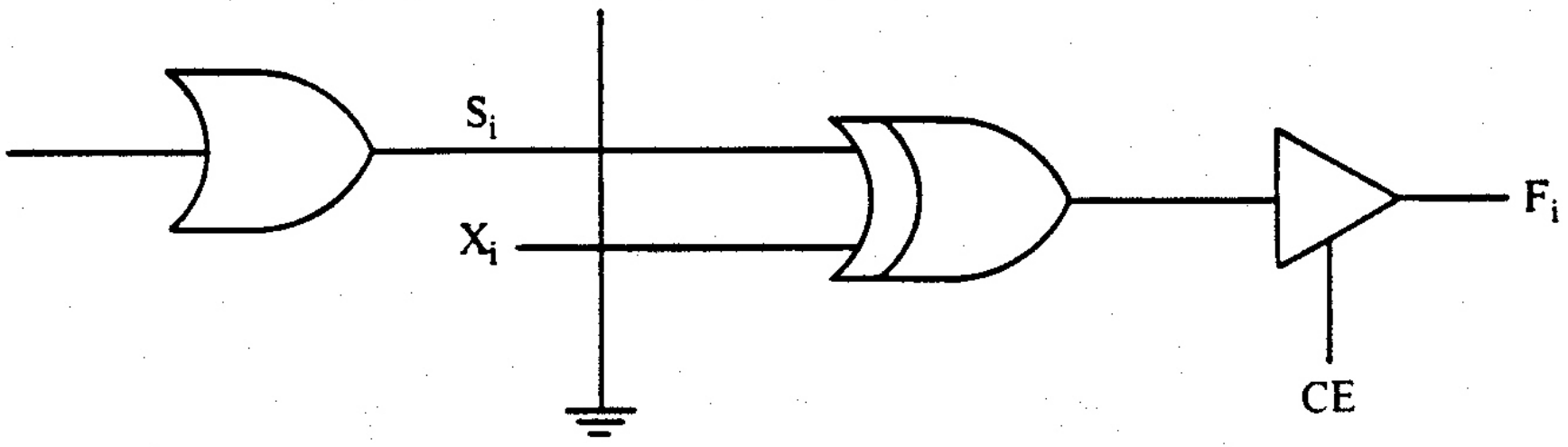


Notes:
1. All AND/XOR gate inputs with a blown link float to a logic 1
2. All OR gate inputs with a blown link float to a logic 0

Figure 6.14 82S100 FPLA. (Courtesy of Signetics Corporation.)



(a) Active-high



(b) Active-low

Figure 6.15 Programming the polarity of an FPLA output terminal.

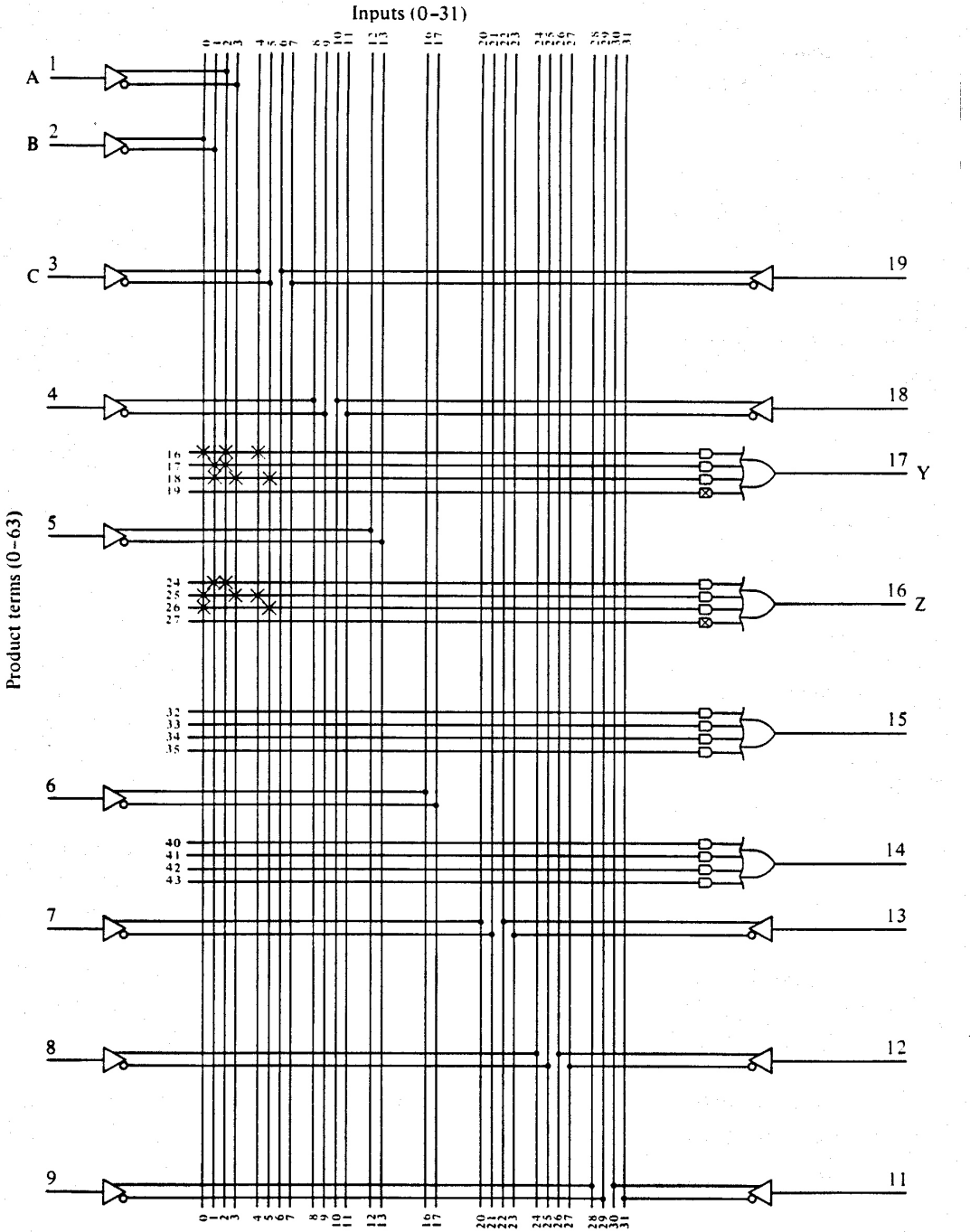
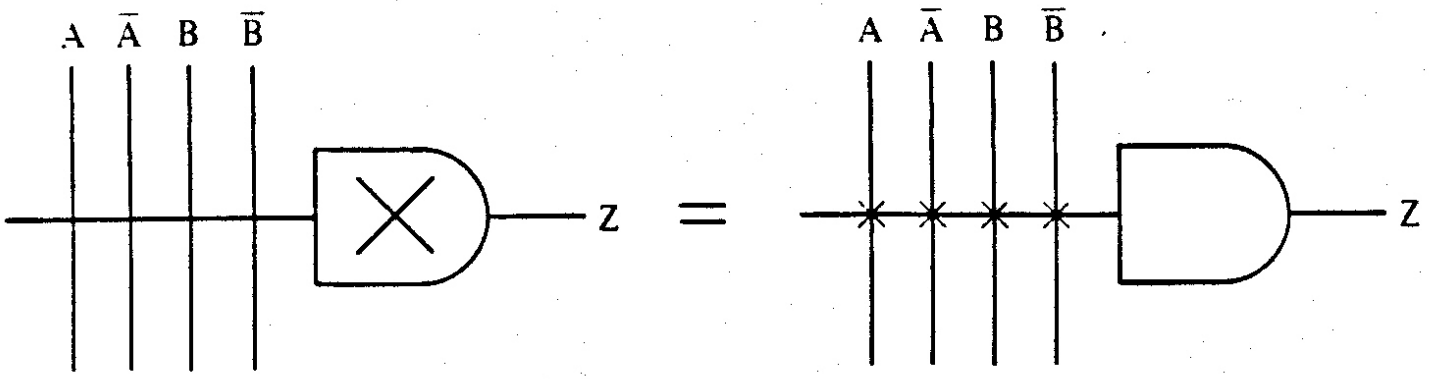
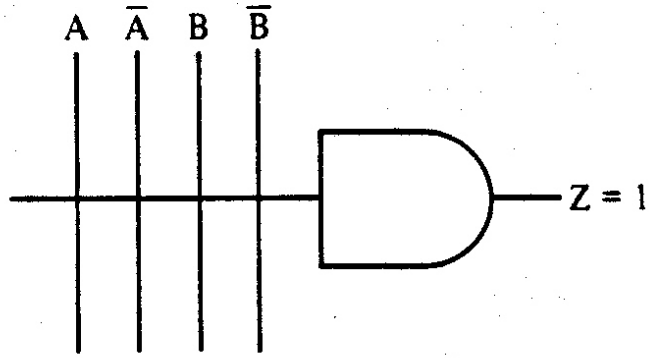


Figure 6.16 PAL14H4 realization of $Y = ABC + A\overline{B} + \overline{A}\overline{B}\overline{C}$ and $Z = A\overline{B} + \overline{A}BC + B\overline{C}$ from Fig. 6.10(a) of Example 6.1.



$$Z = A \cdot \overline{A} \cdot B \cdot \overline{B} = 0$$

(a) All inputs are connected



$$Z = 1$$

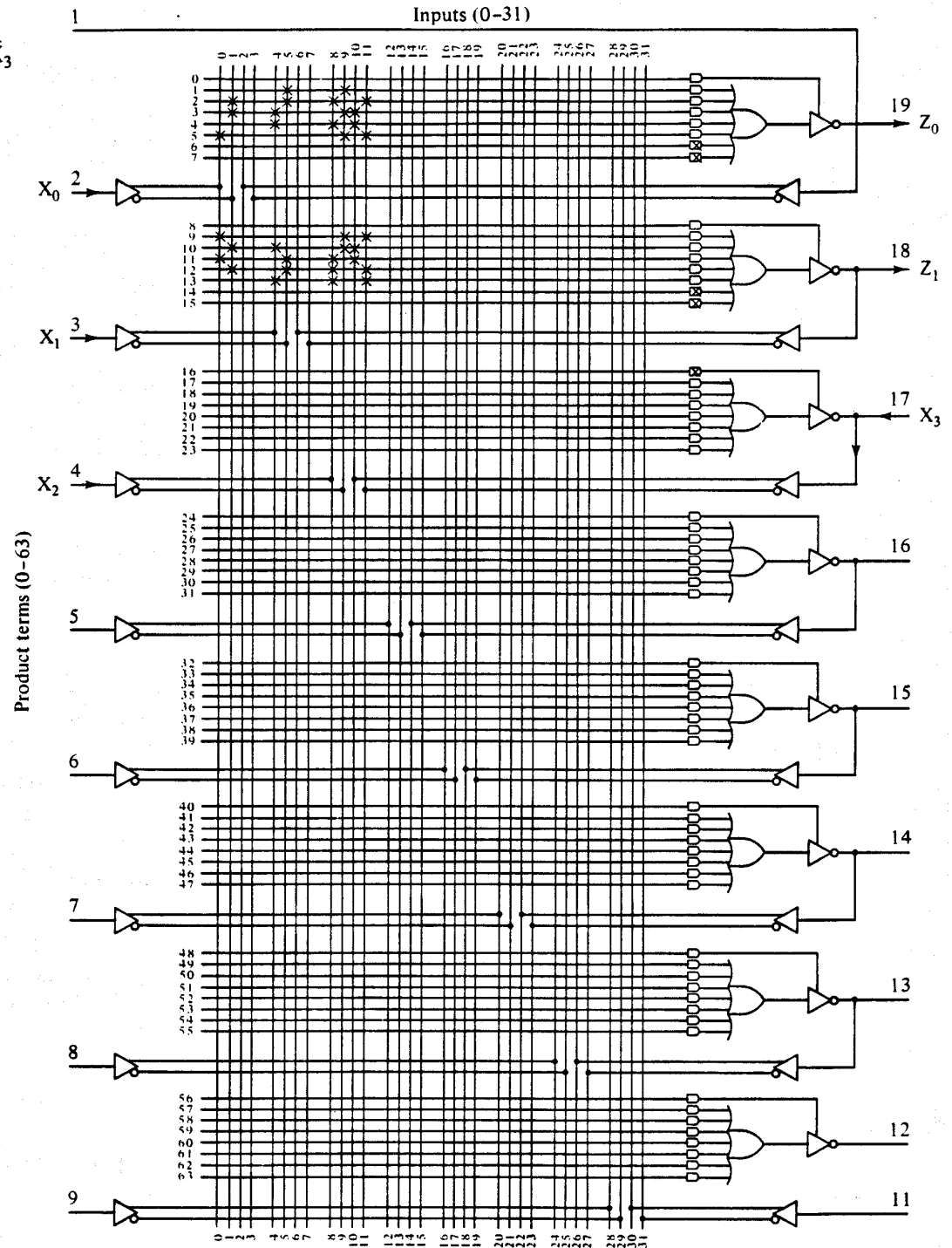
(b) All inputs are disconnected and left floating high

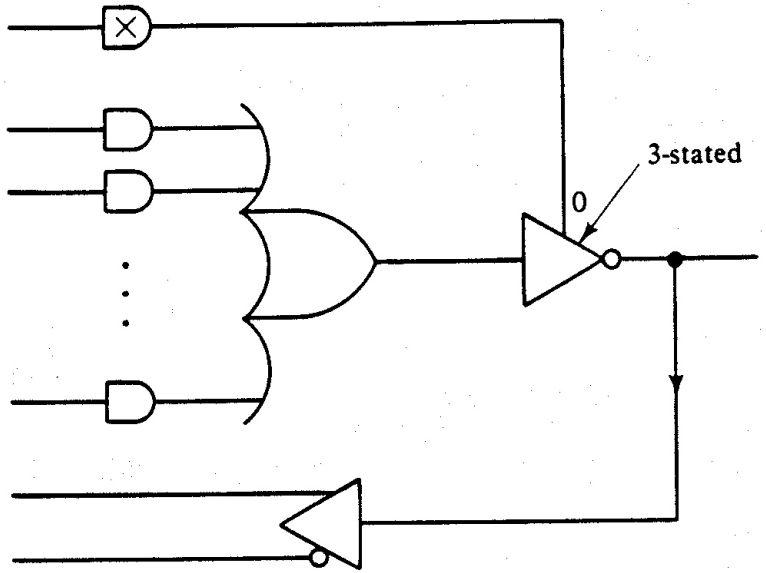
Figure 6.17 PAL shorthand notation.

$$Z_0 = \bar{X}_1\bar{X}_2 + \bar{X}_0\bar{X}_1X_2\bar{X}_3 + \bar{X}_0X_1\bar{X}_2X_3 + X_1X_2X_3 + X_0\bar{X}_2\bar{X}_3$$

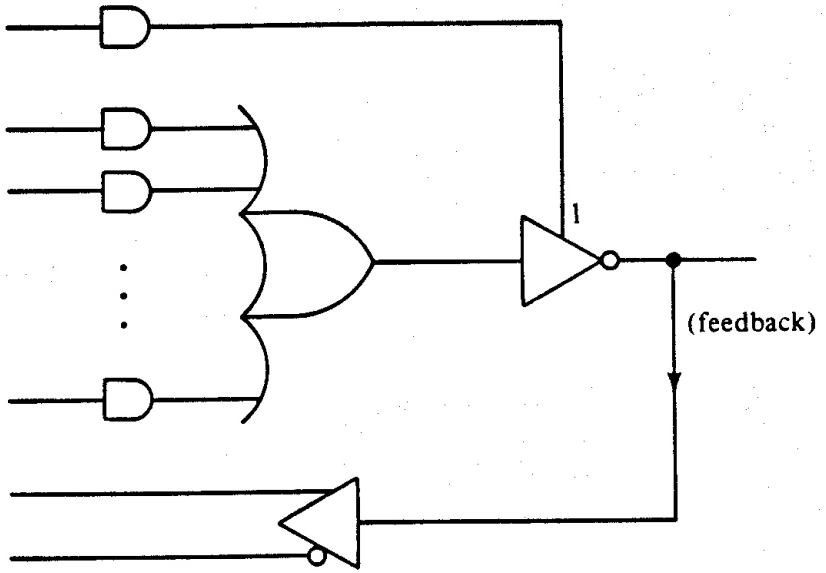
$$Z_1 = X_0\bar{X}_2\bar{X}_3 + \bar{X}_0X_1\bar{X}_2X_3 + X_0\bar{X}_1X_2X_3 + \bar{X}_0\bar{X}_1X_2\bar{X}_3 + X_1X_2\bar{X}_3$$

Figure 6.18 PAL16L8 realization of Example 6.3.





(a) PAL I/O terminal programmed as an input



(b) PAL I/O terminal programmed as an output

Figure 6.19 Programming of an I/O terminal of a PAL.

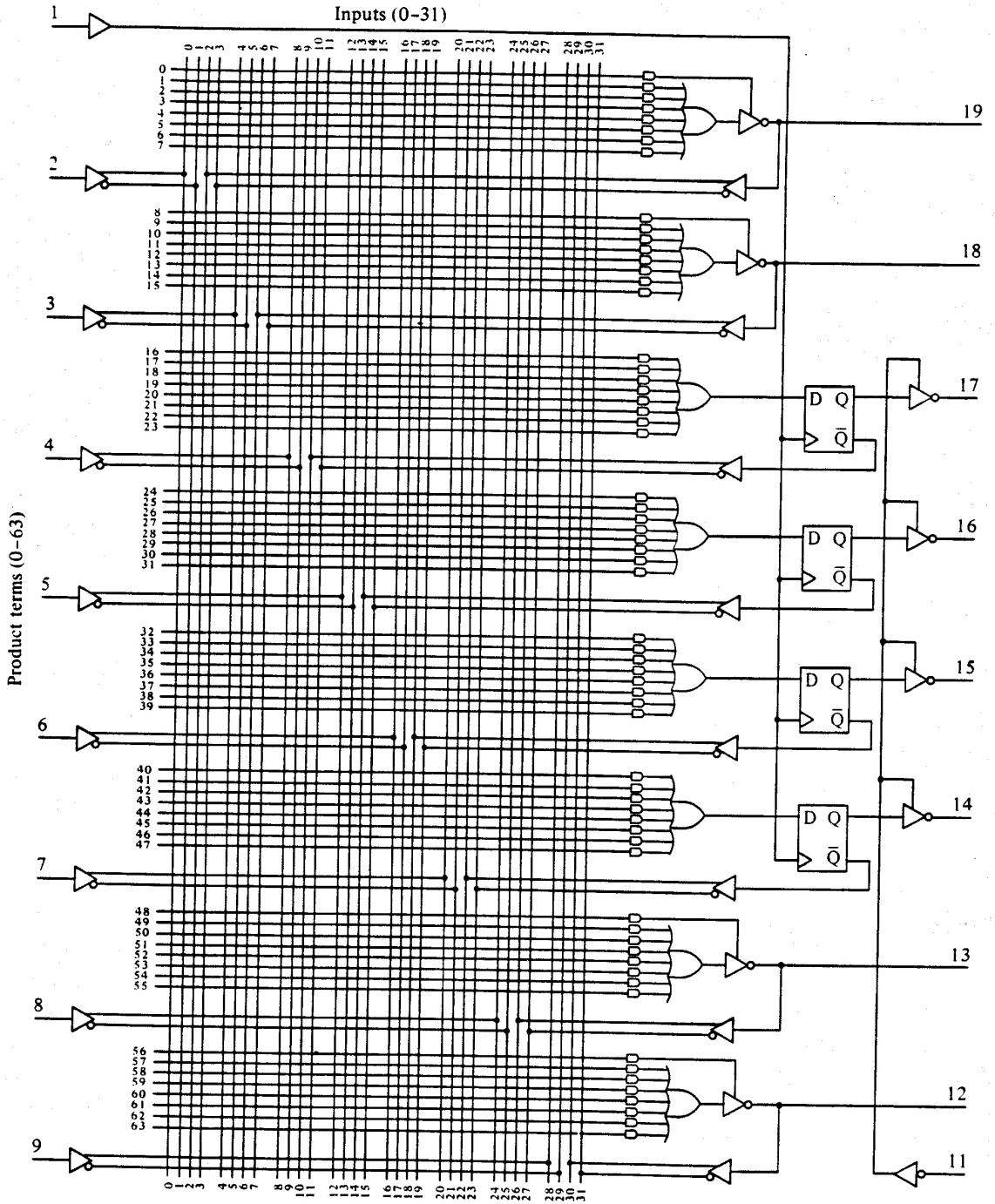


Figure 6.20 Logic diagram of the PAL16R4.