Component Creation: MaxPlusII Tool Tip

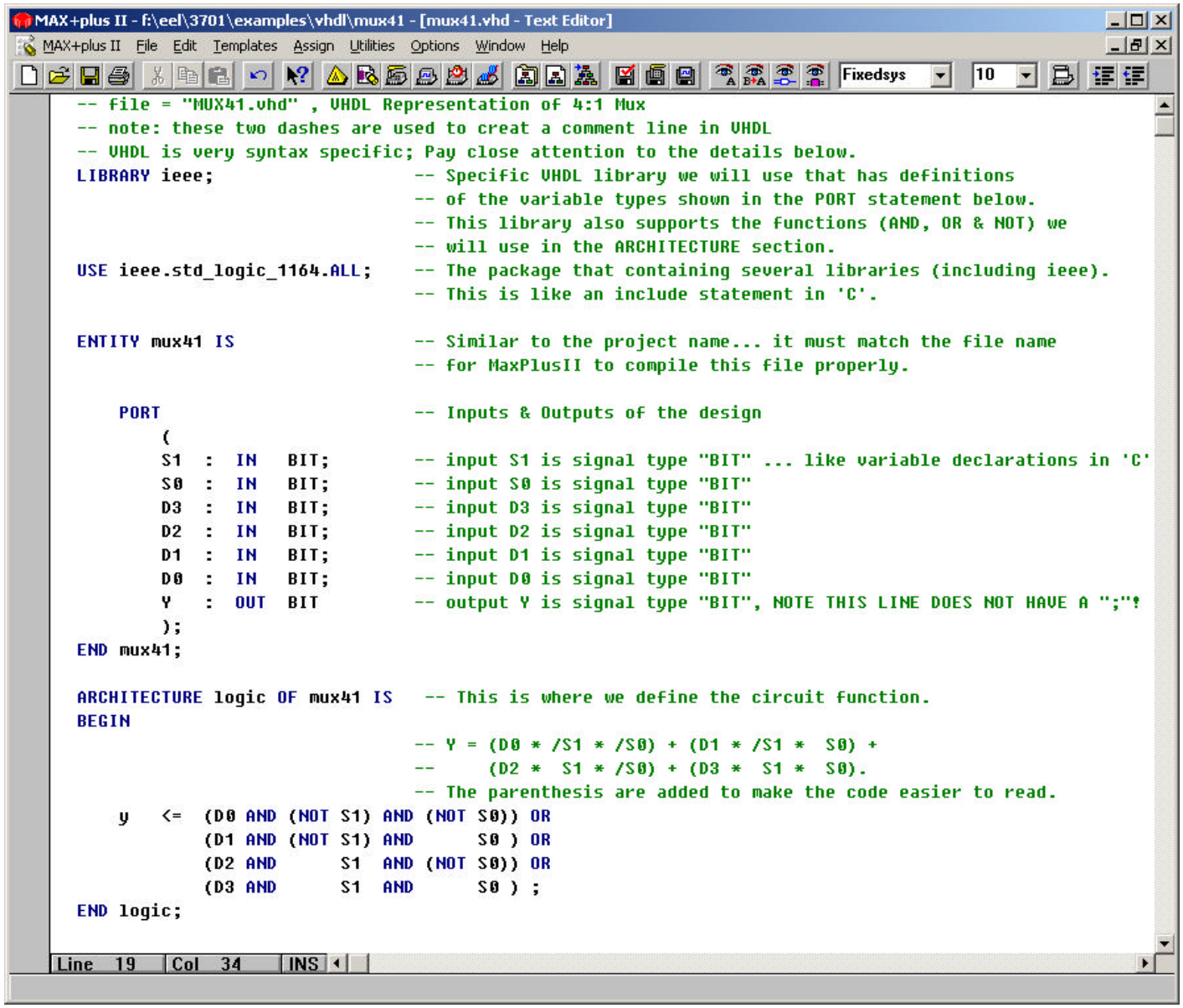
Question: How do I create a component from a previously designed schematic (GDF file), so that I can place in into a new schematic (GDF file)?

Answer: After successfully compiling the project, select the graphics editor window and choose *File | Create Default Symbol*. This will create a file with the extension *sym* in the same directory. This symbol can now be used in a new schematic.

Question: How do I create a component from previously designed VHDL code, so that I can place in into a new schematic (GDF file)?

Answer: The below example will demonstrate the technique.

We would like to create a graphical component out of the Mux41 VHDL code shown below (MUX41.vhd) and use it graphically in another design.



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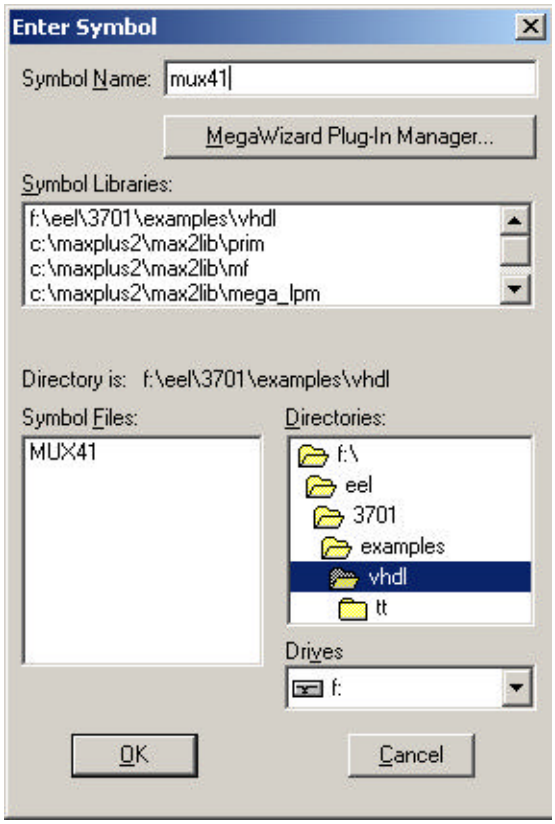
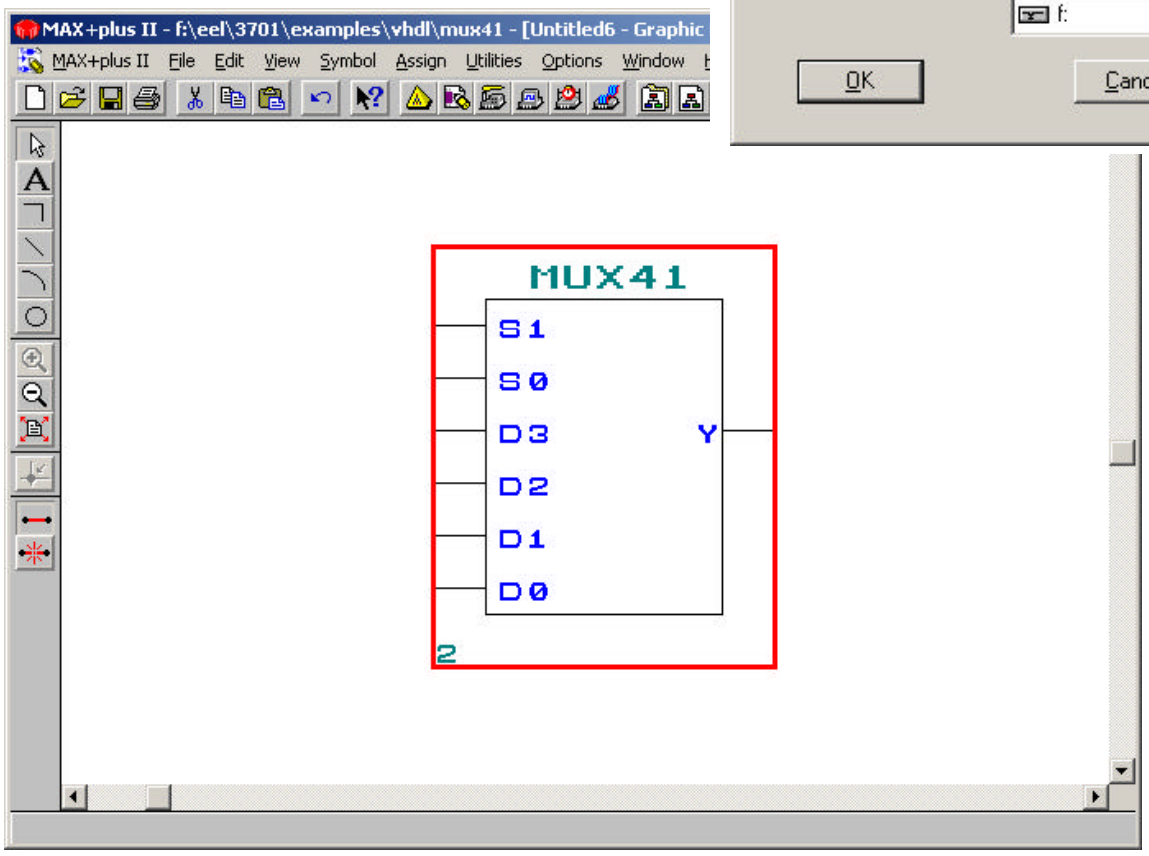
The steps to create a graphical component for this code are:

1. In MaxPlus2, open MUX41.vhd, set your project to this file, and compile it.
2. After compilation, a symbol file, mux41.sym, has been created in that same directory.
3. Create a new Labx.gdf file (*File|New|Graphic Editor Files*) or assume that the file already exists. Put this file in the same directory as MUX41.vhd.
4. Open your schematic (Labx.gdf) in the same directory as the symbol file and set your project to this file. This is the file in which you want to place your newly created VHDL component symbol. Now right click the mouse to enter a symbol and select your symbol you just created from the VHDL code (as shown in this figure).
5. You should see the symbol that you have created from your VHDL file now on your schematic. It is illustrated in the figure below.





6. You can now add wires & I/O to the input and output ports of the component as you would any other component grabbed out of Altera's libraries as shown on the following figure.

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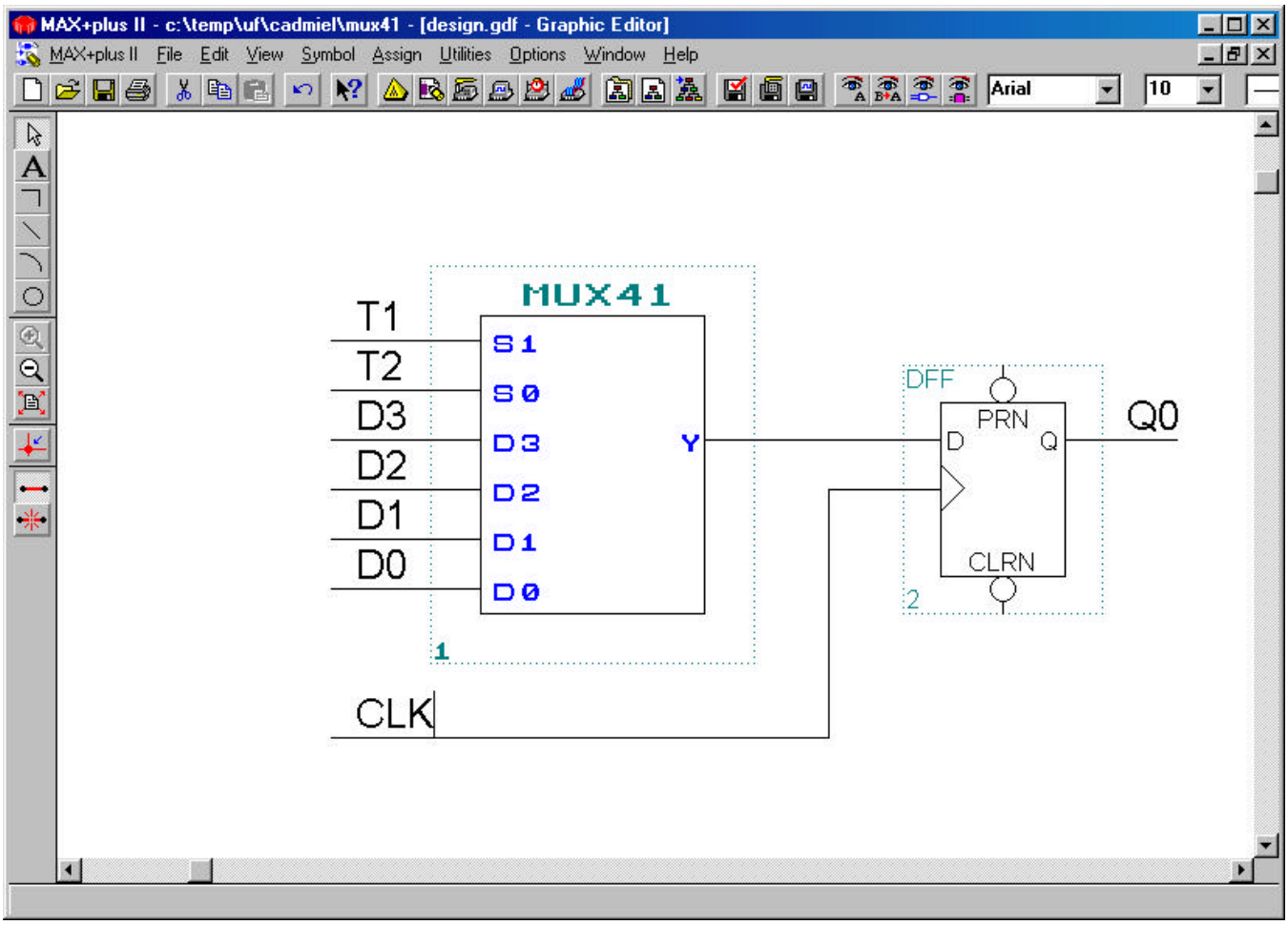

Special Note: It is best not to name the VHDL component and GDF file the same name. Use different names for each.

Example application:
The logic equations of the controller of an ASM can be easily specified using VHDL (much easier than graphically entering the gates). More importantly, they can be easily changed during the debugging phase without having to redraw and connect the gates every time. Using the graphical symbol, the equations can then be integrated with the rest of the ASM.