UF-3701 PLD Board Debugging Suggestions

You can verify the proper operation of your board by designing a circuit in Quartus, programming your PLD PCB and then testing your circuit. If you are suspicious about the proper functioning of a pin or two, just create a simple circuit with inputs, level-shifters (NOT gates) [or use "wire" elements], and outputs, selecting the pins that you are unsure of. Note that a pin could be functional as an input but not as an output (and perhaps vice-versa). A more comprehensive test can be performed by repeating the tests that were done on your board by your PI in one of our early labs. This test will verify most of your pin's output capabilities.

For DE10-Lite PCB

1. Be sure to tri-state all unused inputs.
2. Verify that your breadboard circuits are, in fact, powered (i.e., verify that both 3.3V and ground are connected).
3. Verify that your ribbon cable is properly connected to the DE10 and the breakout PCB on your breadboard. See the OOTB EEL3701 Connection Guide for more info.
4. The other most common problem (leading to overheating and other problems) is incorrectly connecting your PLD PCB to other circuits, i.e., switch circuits and LED circuits. If a PLD pin is chosen as an output and connected to a switch circuit, either the pin or the PLD can be damaged. Often the damage to the pin is permanent, but the PLD can still be used. Other times, the entire chip will be damaged to the point that it can no longer be used.
   - Check and double check that your input and output circuits and pin selection on your PLD match. If you think you may have damaged a pin, check it with a simple circuit. If the pin is damaged, mark it on your board as a warning not to use it again. If you lose a pin or two, don't worry; there are more than enough pins available for all our labs. (Note: It is possible that a pin can be damaged so that it can no longer be used as an output, but that it can still be used as an input.)
5. If you select the wrong device in Quartus, Quartus may indicate that it successfully program and verified the PLD programming, even when it is not programmed at all. You might also get a message similar to "Error: JTAG ID code specified in JEDEC STAPL Format File does not match any valid JTAG ID codes for device." In either of these two cases, a solution is to pick the correct device.
   - To use the DE10-lite in Quartus, do the following:
     - Select "**`Assignment`**"
     - - Select "**`Device`**" and then select the "**`Board`**" tab towards the top of the screen
     - - Change the family to "**`MAX 10`**", and select "**`MAX 10 DE10 - Lite`**".
   - The DE10-Lite uses a Max 10 FPGA Device, **`10M50DAF484C7G`**
6. Rarely, Quartus gets confused and either has an error message that does not make sense or incorrectly programs a device. This is caused when one or more files in a project folder gets corrupted. This error is **very rare**. We can't really complain, because we are getting Quartus for free; it costs $3000 for Quartus and almost $1000 for the simulator. When this problem occurs, it can be corrected by doing the following.
   - Make a new project folder and a new project. Copying your design file(s), bdf and/or vhd, (and your vwf file, if desired), but **nothing** else. Complete your design as usual.
7. If you check all of the above and you still have a problem, look at the Quartus FAQ. If you still cannot fix the problem, contact a PI or Dr. Schwartz.

UF-3701 PLD Board Debugging Suggestions

For OOTB PLD PCB from semesters prior to Fall 2023

If you have a problem with your PLD PCB (with the Altera **10M02SCU169C8G** PLD in the **MAX 10** family of parts), here are a few suggestions of things you can do to find/correct your problem. If your board is not working, it is your responsibility to get it working **BEFORE** your next lab. Failure to do so will cause you to earn no points for the required lab demonstrations.

1. If the PLD starts to get **hot**, **remove power from the circuit immediately**. This rule should be applied to all the circuits built in EEL 3701.
2. Be sure to tri-state all unused inputs.
3. Verify that your PLD PCB is, in fact, powered (i.e., verify that both 3.3V and ground are connected).
4. Verify that you USB Blaster cable is properly connected. Pin 1 is labeled on both the MAX 10 PLD Board and the USB Blaster cable.
5. One of the two most common problems (including overheating PLDs) are due to poor soldering. Even if the board worked when you first tested it, inferior soldering can cause errors including an overheating chip. If you board was bounced around in your tool box, even adequate soldering can be damaged. A good job of soldering should last for many years, probably longer that the IC's in the circuit. But a poor soldering job, even if untouched, can fail at any time.
   - Touch up all the solder joints and use the flux pin. Solder joints should look like a shiny Hershey's Kiss (but without the tag), i.e., shiny and bell-shaped.

Hershey's Kiss

6. The other most common problem (leading to overheating and other problems) is incorrectly connecting your PLD PCB to other circuits, i.e., switch circuits and LED circuits. If a PLD pin is chosen as an output and connected to a switch circuit, either the pin or the PLD can be damaged. Often the damage to the pin is permanent, but the PLD can still be used. Other times, the entire chip will be damaged to the point that it can no longer be used.
   - Check and double check that your input and output circuits and pin selection on your PLD match. If you think you may have damaged a pin, check it with a simple circuit. If the pin is damaged, mark it on your board as a warning not to use it again. If you lose a pin or two, don't worry; there are more than enough pins available for all our labs. (Note: It is possible that a pin can be damaged so that it can no longer be used as an output, but that it can still be used as an input.)
7. If you select the wrong device in Quartus, Quartus may indicate that it successfully program and verified the PLD programming, even when it is not programmed at all. You might also get a message similar to "Error: JTAG ID code specified in JEDEC STAPL Format File does not match any valid JTAG ID codes for device." In either of these two cases, a solution is to pick the correct device.
   - Select the **10M02SCU169C8G** PLD in the MAX 10 family.
8. If the wrong device is showing up in the programmer (because earlier you had selected a wrong or no device and then fixed it), in the programmer double click on a wrong device and then select the correct device (**10M02SCU169C8G**).
   - If the incorrect pof file is displayed in the programmer (under the file section), double click on the incorrect or absent file and then select the correct pof file, i.e., with your filename.

UF-3701 PLD Board Debugging Suggestions

9. Verify that the pins that you soldered on the JTAG header have no connections between them (known as solder bridges). You can detect this by measure the resistance between adjacent pins (when the board is unpowered). If necessary, remove the wayward solder. (Your TA can help.) You might also look for other solder bridges elsewhere on your board.
10. Rarely, Quartus gets confused and either has an error message that does not make sense or incorrectly programs a device. This is caused when one or more files in a project folder gets corrupted. This error is **very rare**. We can't really complain, because we are getting Quartus for free; it costs $3000 for Quartus and almost $1000 for the simulator. When this problem occurs, it can be corrected by doing the following.
    - Make a new project folder and a new project. Copying your design file(s), bdf and/or vhd, (and your vwf file, if desired), but **nothing** else. Complete your design as usual.
11. If you check all of the above and you still have a problem, look at the Quartus FAQ. If you still cannot fix the problem, contact a PI or Dr. Schwartz.