University of Florida   EEL 3701   Dr. Eric M. Schwartz
Department of Electrical & Computer Engineering   Revision **0**   2-Mar-10
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UF-3701 CPLD Board Information
(Altera 7064 PLCC CPLD Information)

The UF-3701 CPLD Board contains an Altera 7064 CPLD (EPM7064SLC44-10). This is a programmable 44-pin device in a PLCC package. The -10 at the end indicates that the device has a propagation delay of 10ns. This CPLD board can be plugged into your protoboard for programming and for a use as complex logic circuits. Once the device is properly programmed, input switch circuits and output LED circuits can be attached to the input and output pins, respectively of the CPLD board.

Table 1 shows the purpose of each of the CPLD pins on the UF-3701 Board. Table 2 shows the pins group by functions.

Table 2: Pinouts by function for Altera's EPM7064SLC44 CPLD. Note that the pins in ( ) are for the JTAG programming and should be avoided, if possible.

CPLD Pin(s)	Function(s)
1 (avoid using)	Input, Global Clear
43	**Input, Global Clock 1**
2 (avoid using)	Input, OE2, Global Clock 2 (alt to pin 43)
44 (avoid using)	Input, OE1
7,13,32,38 (do **not** use)	JTAG programming interface
10,22,30,42	Ground (GND)
3,15,23,35	+5V (VCC)
4,5,6,(7),8,9,11,12	Logic Array Block A I/O
(13),14,16,17,18,19,20,21	Logic Array Block B I/O
24,25,26,27,28,29,31,(32)	Logic Array Block C I/O
33,34,36,37,(38),39,40,41	Logic Array Block D I/O

The board layout is shown in Figure 1. Figure 2 shows the CPLD pin-out diagram. The two pins adjacent to the CPLD socket labeled G and 5V (circled below) are the power pins for this board and should be connected to ground and VCC, respectively.
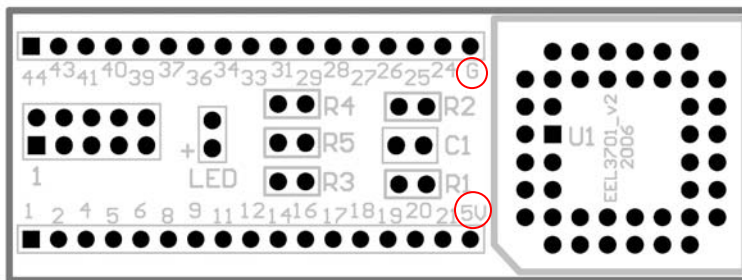

Figure 1: Board layout with pin numbers. The circled pins are used to power the board.

Make sure that you assign the EPM7064SLC44-10 device before compiling your design.

Table 1: Pinouts for Altera's EPM7064SLC44 CPLD.

CPLD Pin	Purpose
1	Input/GCLRn
2	Input/OE2/GCLK2
3	VCC
4	General I/O
5	General I/O
6	General I/O
7	TDI (prog)
8	General I/O
9	General I/O
10	GND
11	General I/O
12	General I/O
13	TMS (prog)
14	General I/O
15	VCC
16	General I/O
17	General I/O
18	General I/O
19	General I/O
20	General I/O
21	General I/O
22	GND
23	VCC
24	General I/O
25	General I/O
26	General I/O
27	General I/O
28	General I/O
29	General I/O
30	GND
31	General I/O
32	TCK (Prog)
33	General I/O
34	General I/O
35	VCC
36	General I/O
37	General I/O
38	TDO (Prog)
39	General I/O
40	General I/O
41	General I/O
42	GND
43	**Input/GCLK1**
44	Input/OE1

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Some key points to remember about programming your board:

1. The UF-3701 board brings out the above signals to the pins that plug into the protoboard.
2. The JTAG programming pins are used to program the device via the USB (or parallel port Byte-Blaster cable (attached to your PC) and thus can **not** generally be used as inputs. These pins can be monitored with an oscilloscope.
3. The **Global Clock 1** pin should be used as a clock signal input in your design. This means that the clock node in your circuit should be assigned to pin 43 on the 7064. The procedure to do this will be described shortly.
4. The available I/O pins are those listed in Table 2 as Logic Array Block A, B, C or D I/O. These pins can be used as either inputs or outputs.
5. All other signals (OE1, OE2, GCLK2) will be discussed at a future date and should **not** be used in your design.
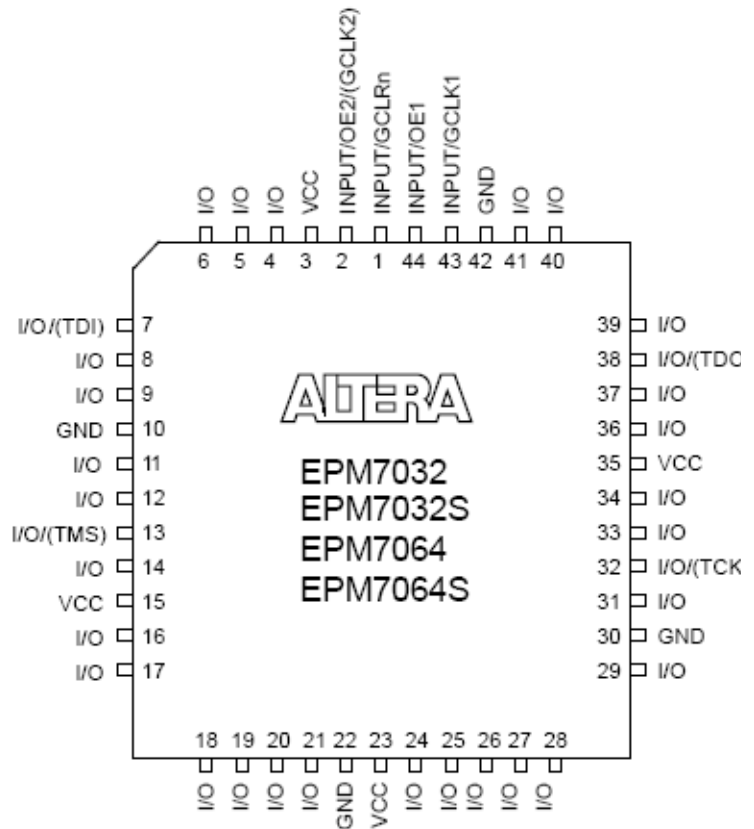

Figure 2: EPM7064 44-Pin Pin-Out Diagram.

There are two ways to have pins assigned to your schematic entry (or VHDL or Verilog) designs.

1. Let Quartus assign the pins automatically, and then modify them if necessary. (I recommend that you use this technique.)
2. Assign them yourself in the design.

These two methods are now described.

Quartus Automatic Pin Assignment

If you don't tell Quartus what pins to use on a CPLD or FPGA, it will automatically choose them for you. This is actually very good because the software will try to fit your design using all the available resources (gates) in the device. This is what you have been doing (without knowing it) in your designs thus far. You simply compile the design and pins are automatically selected. The question now becomes how do we look up the pins that Quartus has chosen for I/O in your design.

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When you compile a design, Quartus assigns the pins for your design. There are several ways to see the pins Quartus has assigned.

Figure 3: Part of Compiler Tool window.

1. If you used the "Compiler Tool" (available under Processing), you can select the third button under "Fitter" with the word "TEXT" under it (as shown in Figure 3). This will open the Fitter Report file (with file name extension .fit.rpt).
2. If you used the "Compiler Tool" (available under Processing), you can select the button labeled "Report." In the report window, select Fitter | Pin-Out File. All of the pins of this chip are listed with the associate signal names.
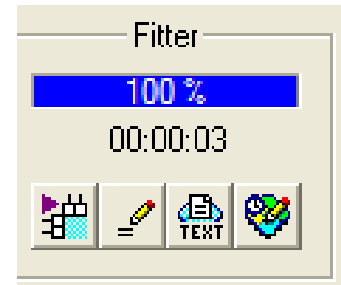
You can view all the pin locations presently assigned with the "Timing Closure Floorplan," which can be found at Assignments | Timing Closure Floorplan. Pins can be changed in the Timing Closure Floorplan simply by clicking on the input or output you would like to reassign, dragging it to the new pin assignment, and dropping it there. You must recompile after modifying pin assignments.

Manually configuring a Pin Assignment (or altering the Quartus Pin Assignments)
If you want to use the pinouts that Quartus has assigned for you and make them fixed as you edit your design, then under "Assignments" menu select "Back-Annotate Assignments…". Select "Pins & device assignments" and then select "OK". The pins should now appear on your bdf design.

To change the pin numbers, you can double click on a pin and individually change it or you can use the "Pin Planner" or "Assignment Editor" discussed below.

You can assign pins directly with the "Pin Planner," which can be found at Assignments | <u>P</u>ins. The green arrow in Figure 4 points to the Pin Planner button. The window that comes up will show a block diagram of the chip an allow you to select the pin number for each of your inputs and outputs.

Figure 4: Green arrow shows "Pin Planner" button.

You can assign pins directly with the "Assignment Editor," which can be found at Assignments | <u>A</u>ssignment Editor. The red arrow in Figure 4 points to the "Assignment Editor" button. A short cut keystroke is Ctrl-Shift-A.

To have any pin number changes take effect, you **<u>must</u>** recompile the design.

To display and hide (i.e., to toggle) the appearance of pin numbers in your bdf file, use the right mouse button and select Show | Show Location Assignments. The pin numbers that were next to your inputs and output pins will now disappear. If you do it again, the pin numbers will reappear.