

Component Creation: Quartus Tool Tip

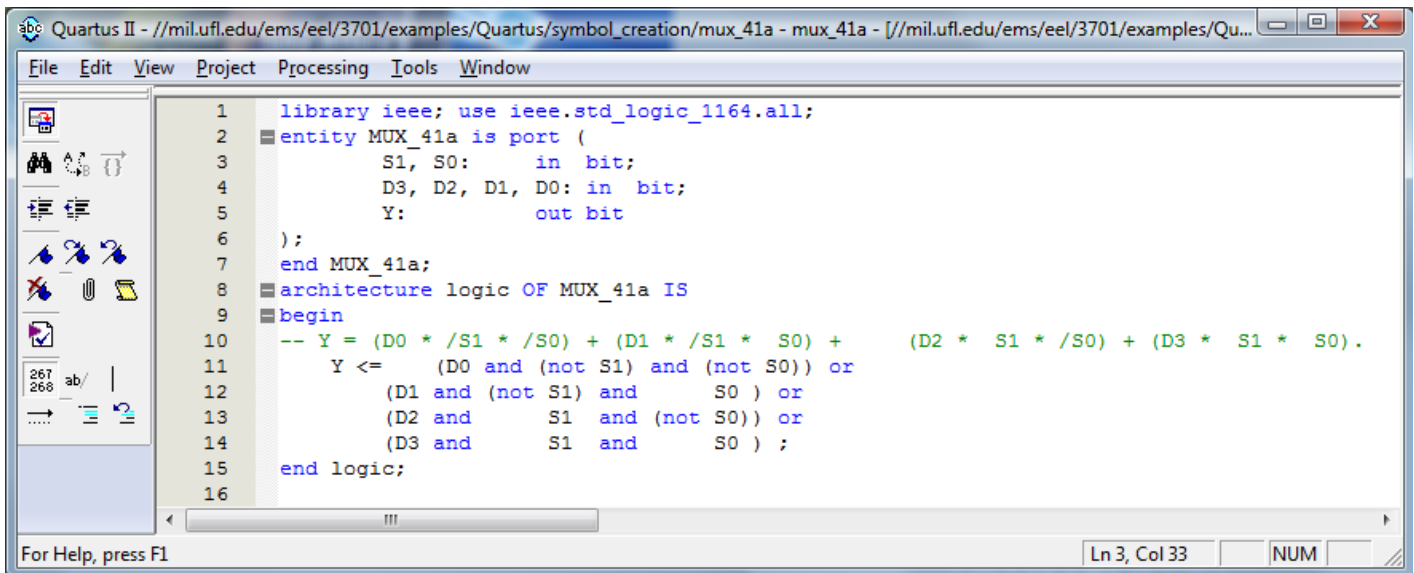
Question: How do I create a component from a previously designed schematic (BDF file), so that I can place it into a new schematic (BDF file)?

Answer: After successfully compiling the project, select the graphics editor window (BDF file) and then choose *File | Create / Update | Create Symbol Files for Current File*. This will create a file with the extension *bsf* in the same directory. This symbol can now be used in a new schematic.

Question: How do I create a component from previously designed VHDL code, so that I can place it into a new schematic (BDF file)?

Answer: After successfully compiling the project, select the VHDL file and then choose *File | Create / Update | Create Symbol Files for Current File*. This will create a file with the extension *bsf* in the same folder. This symbol can now be used in a new schematic. The below example will demonstrate the technique.

We would like to create a graphical component out of the MUX_41a VHDL code shown below (MUX41a.vhd) and use it graphically in another design. (Alternatively, you could create this same MUX with several ANDs, ORs and NOTs using schematic entry in a BDF file.)

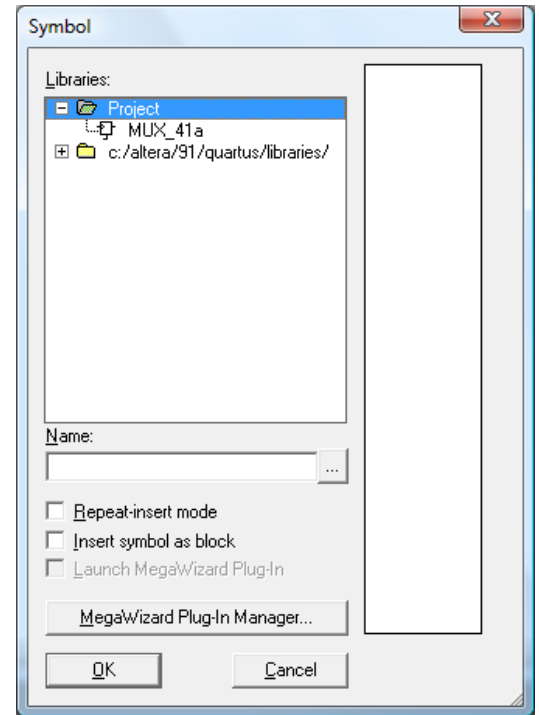


```
1  library ieee; use ieee.std_logic_1164.all;
2  entity MUX_41a is port (
3      S1, S0:    in bit;
4      D3, D2, D1, D0: in bit;
5      Y:        out bit
6  );
7  end MUX_41a;
8  architecture logic OF MUX_41a IS
9  begin
10     -- Y = (D0 * /S1 * /S0) + (D1 * /S1 * S0) + (D2 * S1 * /S0) + (D3 * S1 * S0).
11     Y <= (D0 and (not S1) and (not S0)) or
12         (D1 and (not S1) and S0) or
13         (D2 and S1 and (not S0)) or
14         (D3 and S1 and S0);
15 end logic;
16
```

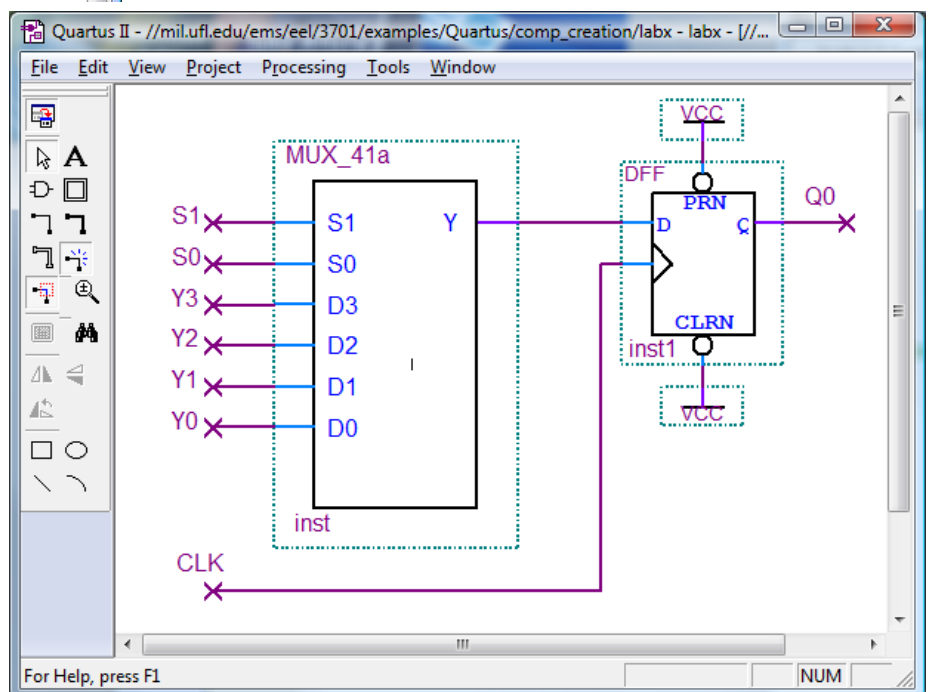
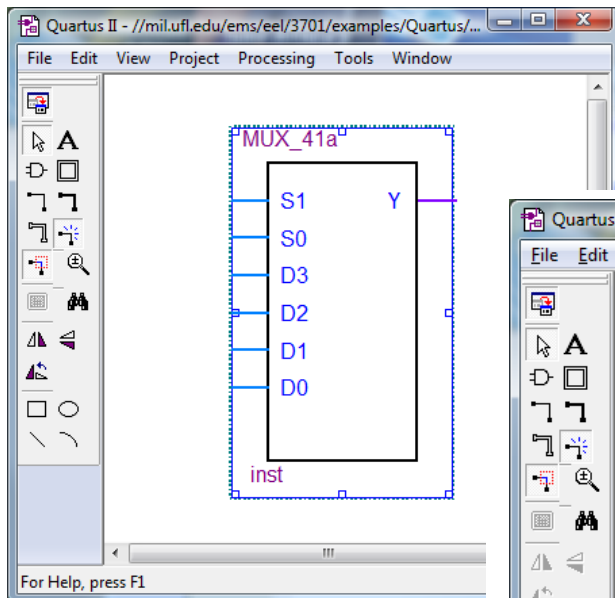
Component Creation: Quartus Tool Tip

The steps to create a graphical component for MUX_41a.vhd (or a bdf file):

1. In Quartus, create a new project called LabX. I made the project LabX in folder comp_creation (for component creation). Create a vhd (or bdf file) called MUX_41a.vhd. Set this file as your “Top-Level Entity”, i.e., *Project / Set as Top-Level Entity*) and then compile.
2. After compilation, select the design file (MUX_41a.vhd). Create a new symbol as by selecting *File / Create / Update / Create Symbol Files for Current File*. A symbol file (MUX_41a.bsf) has been created in that same folder.
3. Create a new schematic entry (bdf) file in the same folder. This is the file in which you want to place your newly created VHDL (or schematic entry) component symbol. Now double-click the left mouse button to enter a symbol and select the symbol you just created (MUX_41a), as shown in this figure. Save this schematic entry file as Labx.bdf.
4. You should see the symbol that you have created from your VHDL file now on your schematic. It is illustrated in the figure below.



5. You can now add wires & I/O to the input and output ports of the component as you would any other component selected out of Altera’s libraries, as shown in the figure below.



Component Creation: Quartus Tool Tip

Special Note: It is best not to name the VHDL component and BDF file the same name. Use different names for each.

Example application:

The logic equations for an ASM controller can be easily specified using VHDL (much easier than graphically entering the gates in a bdf schematic entry file). More importantly, they can be changed easily during the debugging phase without having to redraw and connect the gates every time. Using the graphical symbol, the equations can then be integrated with the rest of the ASM.