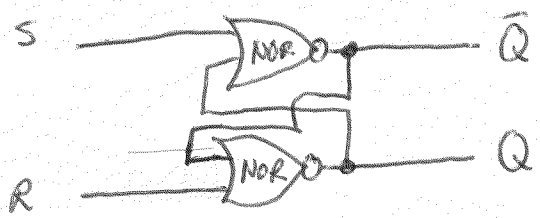
Flip-Flop Creation

Ungated SR



*Design Requirement: $Q \neq \bar{Q}$ always!

① Start w/initial condition
$Q=0, \bar{Q}=1$
$S=0, R=0$
- trace through circuit you'll notice there is no change in $Q \neq \bar{Q}$

(1A) change $S=1, R=0$
stabilizes to $Q=1, \bar{Q}=0$

(1B) change $R=1, S=0$
stabilizes to $Q=0, \bar{Q}=1$

(1C) change $S=1, R=1$
stabilizes to $Q=0, \bar{Q}=0$
* violates original design requirement

① Start initially w/conditions
$Q=1, \bar{Q}=0$
$S=0, R=0$
- trace and you find no change in $Q \neq \bar{Q}$

(1A) change $S=1, R=0$
stabilizes to $Q=1, \bar{Q}=0$

(1B) change $R=1, S=0$
stabilizes to $Q=0, \bar{Q}=1$

(1C) change $R=1, S=1$
get $Q=0, \bar{Q}=0$
* also violates original design requirement

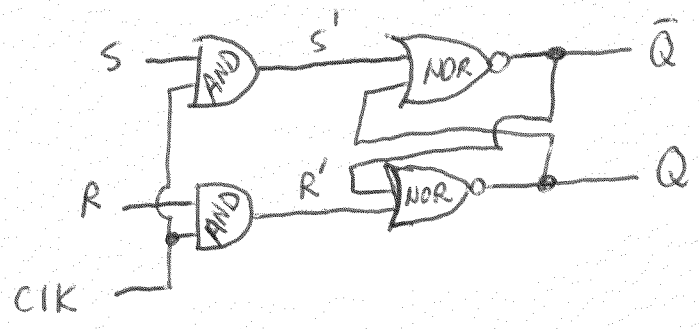
SR Characteristic Table

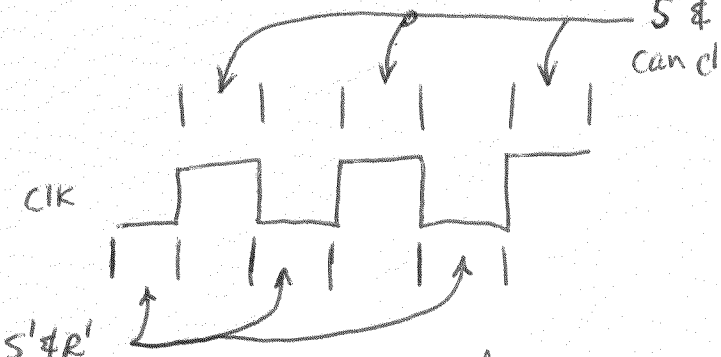
S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Not Allowed
1	1	1	Not Allowed

Condensed

S	R	Q^+
0	0	Q hold
0	1	0 reset
1	0	1 set
1	1	Not allowed

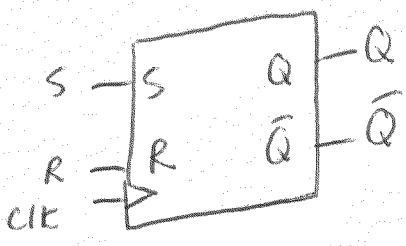
Gated SR Flip-Flop



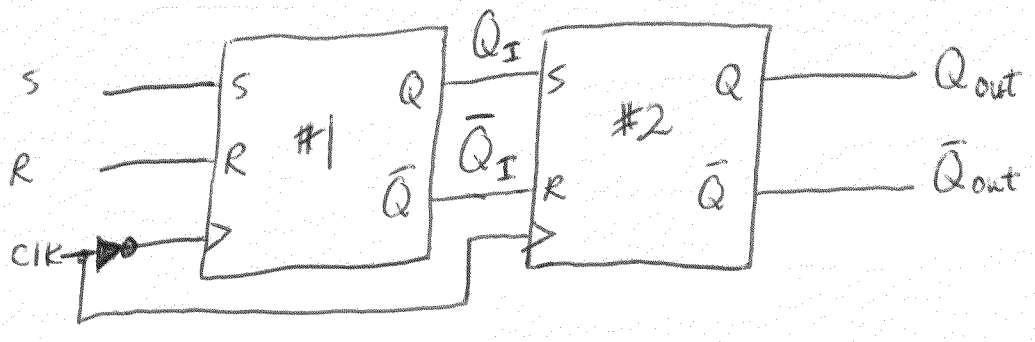


are always low ∴ hold mode

creat simple gated block



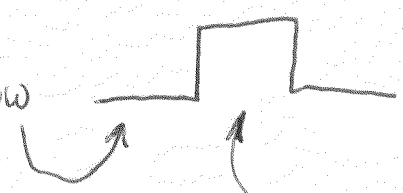
Edge Triggered SR F/F out of (2) SR Blocks & inverter on Clk to one of them



① Let $Q=0$, $\bar{Q}=1$ initially

② Let $S=1$ & $R=0$

- when CLK is low



$S=1$, $R=0$
passes through SR #1
and set intermediate $Q_I=1$ & $\bar{Q}_I=0$

- when clk goes high
SR #1 goes into "hold" mode
SR #2 passes Q_I & $\bar{Q}_I$
through such that $Q_{out}=1$
$\bar{Q}_{out}=0$

Device can only change output (Q_{out}, $\bar{Q}$
a short time after CLK goes high ∴ risin
edge triggered device.

EEL 3701 Flip Flop Notes

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2/98

F/F summary

"JK-F/F"

Abbreviated JK Next State Table (also called characteristic table)

J K	Q^+
0 0	Q (hold)
0 1	0 (Reset)
1 0	1 (set)
1 1	$\bar{Q}$ (toggle)

Abbreviated Excitation Table

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Abbreviated Excitat
"D-F/F"

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

Abbreviated Excitation T-F/F

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Abbreviated Excitation SR F/F

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

This table format is very useful in generating Next State Table for counters & ASM

→ *FUTURE PROBLEMS TO COME

"Creating Flip Flops from other Flip Flops"

T F/F from a JK F/F?

① Look at char. table for each

J K	Q^+
0 0	Q
0 1	0
1 0	1
1 1	$\bar{Q}$

→ ?

T	Q^+
0	Q
1	$\bar{Q}$

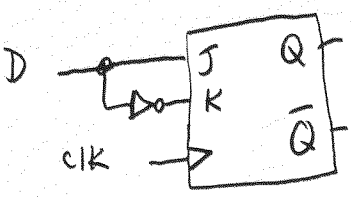
- Notice the cases when J=K=0 & J=K=1 match the T char. table....

∴

D F/F from JK F/F ?

J K	Q^+
0 0	Q
0 1	0 (clear)
1 0	1 (set)
1 1	$\bar{Q}$

D	Q^+	
0	0	← when J=0, K=1 (clear)
1	1	← when J=1, K=0 (set)

∴ 

D F/F from SR F/F ?

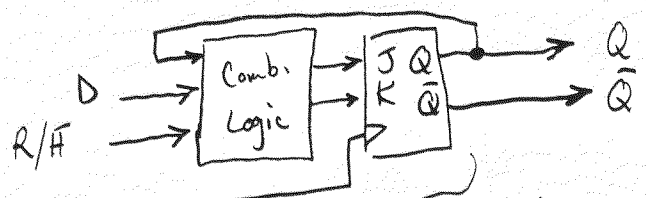
S R	Q^+
0 0	Q
0 1	0
1 0	1
1 1	N/a

D	Q^+
0	0
1	1

– you try this one...?

How do we create a D F/F with a Run/$\overline{\text{HOLD}}$ signal from a JK F/F?

① start w/ char table of new device & Draw block diagram



CLK	R/$\bar{H}$	D	Q	Q^+	
↑	0	0	0	0	Hold mode
↑	0	0	1	1	
↑	0	1	0	0	
↑	0	1	1	1	
↑	1	0	0	0	Run Mo
↑	1	0	1	0	"Typica
↑	1	1	0	1	D F/F
↑	1	1	1	1	

② Write Char. Table for target F/F

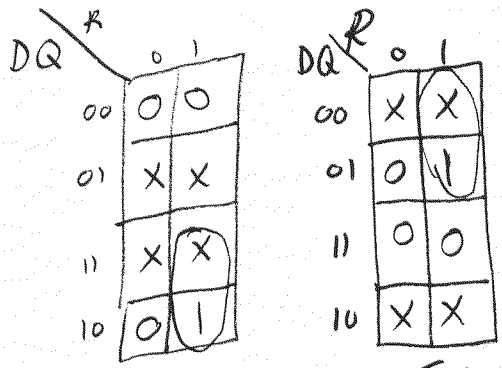
J K	Q^+
0 0	Q
0 1	0
1 0	1
1 1	$\bar{Q}$

③ Write next state using target F/F information

R/H	D	Q	J	K	Q^+
0	0	0	0	X	0
0	0	1	X	0	0
0	1	0	0	X	1
0	1	1	X	0	
1	0	0	0	X	0
1	0	1	X	1	0
1	1	0	1	X	1
1	1	1	X	0	1

what combinations produce the correct $Q \rightarrow Q^+$ transition?

④ Find Equations for J & K inputs (K-maps)



∴ Q is not needed!

⑤ Final Circuit