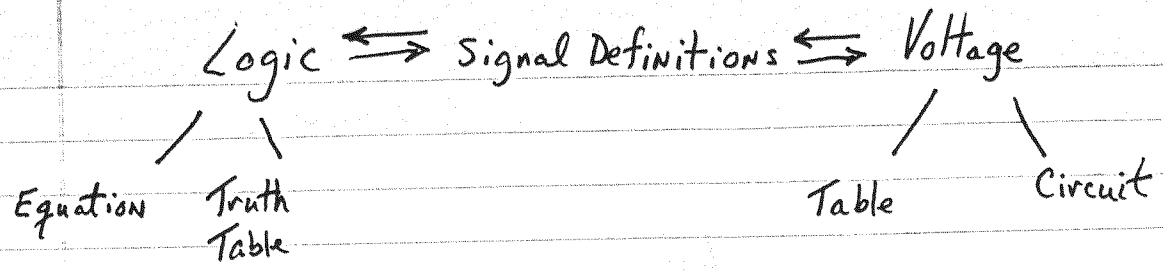
Dr. K. Gugel

*Note from **Dr. Schwartz:** Many things in this document are **NOT** the way that our class does mixed logic. Ask me if you are not sure.*

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Given: $Y = \overline{\overline{A}B + C}$ Logic Equation w/ A.L, B.H, C.H, Y.L signal definition

① Write the Logic Truth Table?

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

② Write the Voltage Table?

| A.L | B.H | C.H | Y.L |
|---|---|---|---|
| H | L | L | H |
| H | L | H | H |
| H | H | L | H |
| H | H | H | H |
| L | L | L | H |
| L | L | H | H |
| L | H | L | L |
| L | H | H | H |

(3) Implement the Circuit using NAND gates only?

(3a) Positive Logic Method

I. Draw the Logic Equation using ANDs & OR Gates.

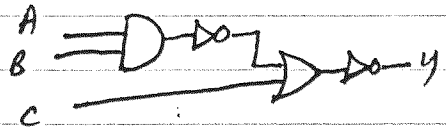
II. Add inverters for complements in the Logic Equation

III. Add inverters for low true input and output signals.

IV. Simplify using existing hardware.

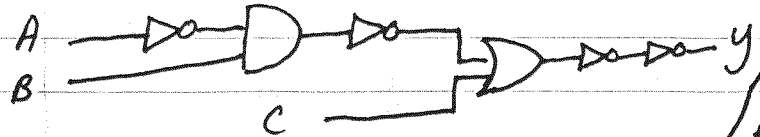
I. $\overline{Y = \bar{A}B + C}$


II.

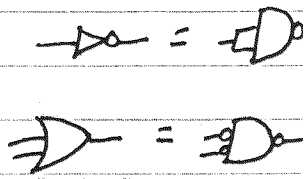


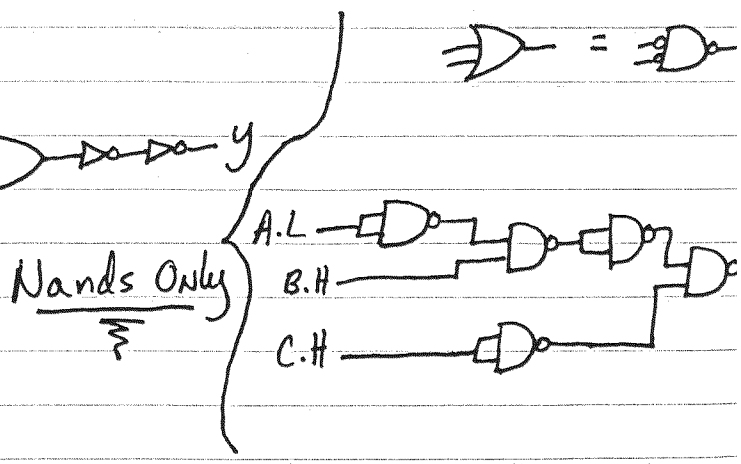

*Note from **Dr. Schwartz:** All inputs and outputs should have labeled activation levels.*

III. A.L, B.H, C.H, Y.L
* *




IV.

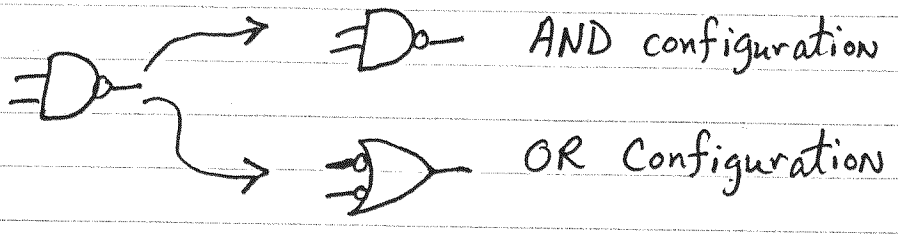




## (3b) Mixed Logic Method

I. Draw with selected gate in "AND" or "OR" configuration as needed.

i.e. selected gate = NAND




II. Look for mismatches in the circuit. Mismatches should correspond to complements in the logic equation.

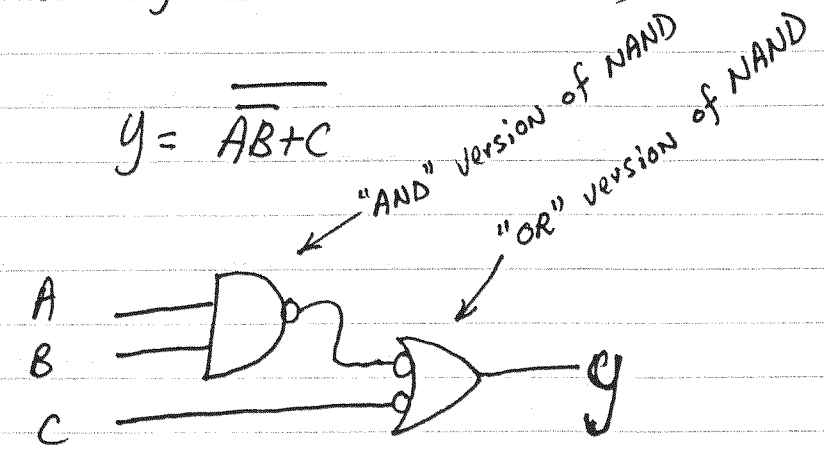
III. Add inverters to remove or add mismatches such that the existing mismatches all correspond to complements in the logic equation.

### List of Mismatches

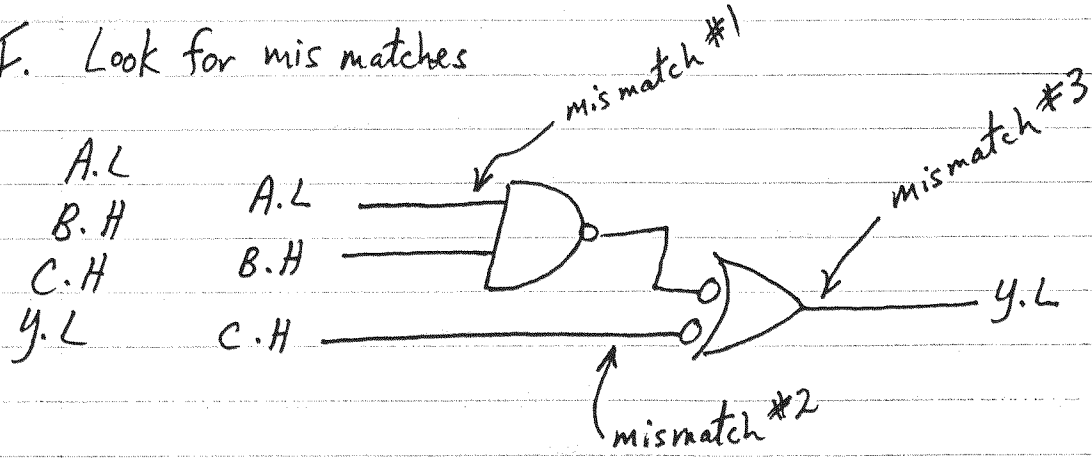
(a) active low input signal connected to active high input wire
(b) active high input signal connected to active low (bubble) wire
(c) active high output wire connected to an active low output signal
(d) active low output wire connected to an active high output signal

(36) Mixed Logic Method (continued)

I. $y = \overline{\overline{A}B + C}$




II. Look for mis matches



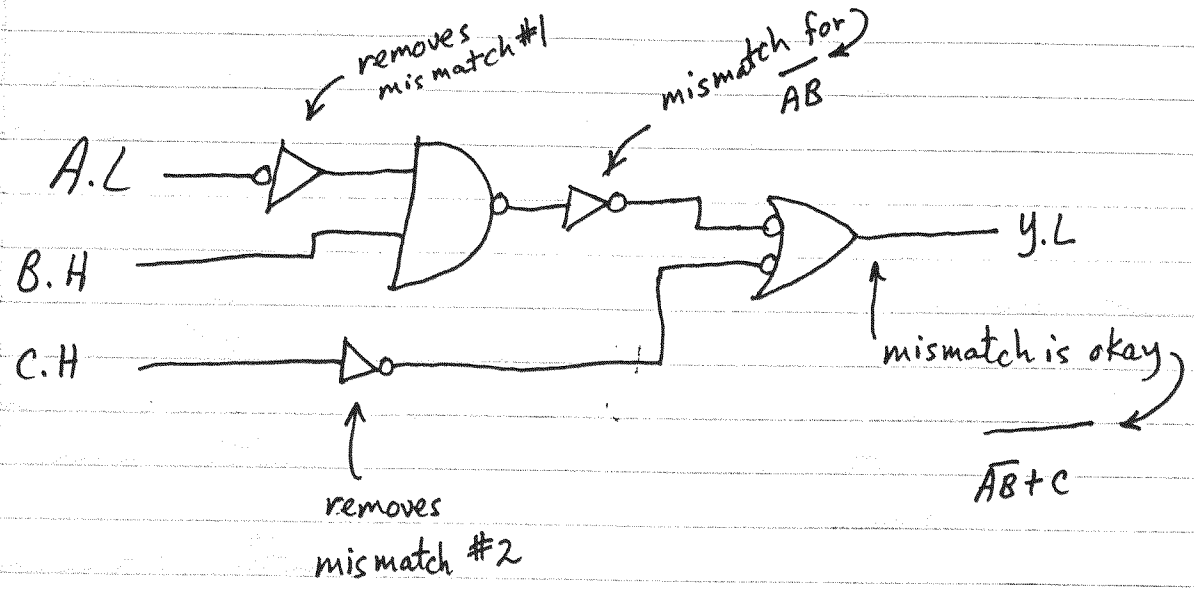

- we only want mismatches for $\overline{\overline{A}B + C}$

- mismatch #1 & #2 are not desired and should be remove with inverters

- mismatch #3 is $\overline{\overline{A}B + C}$ so this is okay

- also, need to create mismatch

## III. Fixing Bad Mismatches & Creating one needed mismatch




- above circuit is complete but you should show:

Extra Practice: Draw the circuit for L.E. $y = \overline{A\bar{B}C} + D$

using NORs w/ y.L, A.H, B.H, C.H, D.L signal definiti

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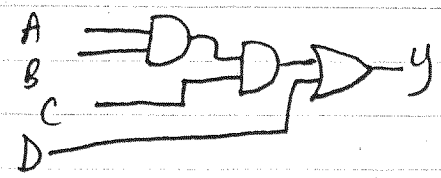
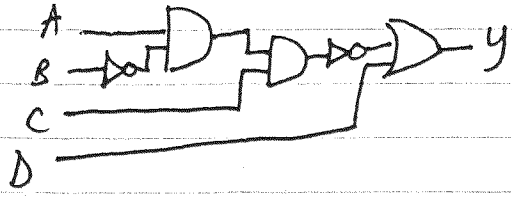
Positive Logic Method

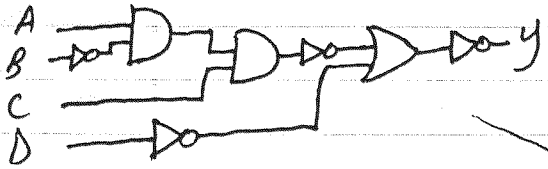
I.



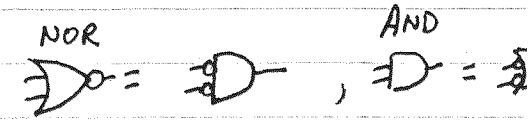

II.

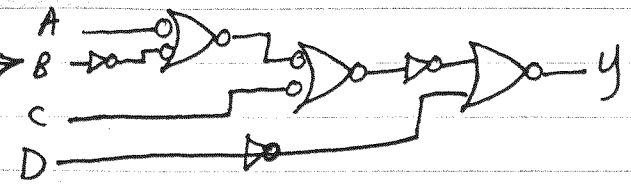



III. y.L, D.L



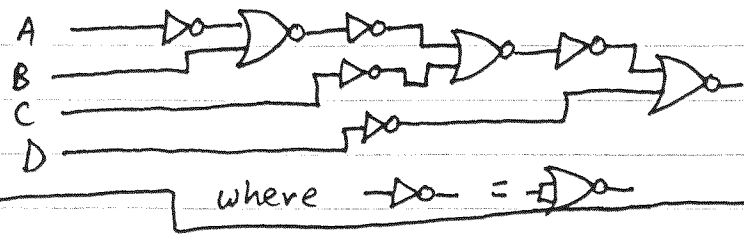

IV.




*Note from **Dr. Schwartz:** All inputs and outputs should have labeled activation levels.*

Final Circuit




Mixed Logic

"OR" style "AND" style

I.

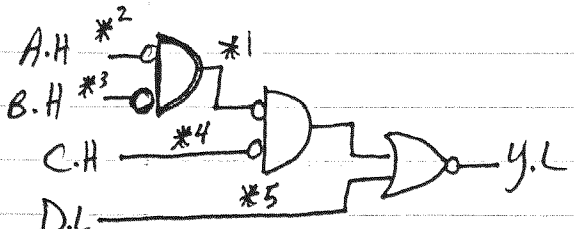
II. *1-5 are mismatches!

*1 = bad, must remove *4 = Bad, rem

*2 = bad, must remove *5 = Bad, rem

*3 = okay, $\bar{B}$

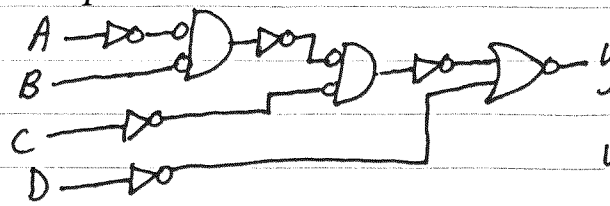
_ also, add mismatch for $\overline{A\bar{B}C}$




*Note from **Dr. Schwartz:** All inputs and outputs should have labeled activation levels.*

Final Circuit

III.




where,