University of Florida
Department of Electrical & Computer Engineering

EEL 3701 Fall 1996
2 October 1996

Exam #1

Dr. Eric M. Schwartz
Professor in ECE

24-Aug-99 1:28 PM

_______________ , ___________

Last Name , First Name

fpInstructions:

- ***Show all work*** *on the* ***front*** *of the test papers. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will not be graded without an indication on the front.*
- *You may* ***not*** *use any notes, HW, labs, other books, or calculators.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *This exam counts for at least 20%. of your total grade (13.3% if you fail to take one of the 3 exams).*
- *Put your name at the top of* ***each*** *test page and be sure your exam consists of 8 distinct pages.*
- ***Read*** *each question* ***carefully*** *and* ***follow the instructions****.*
- *Boolean expression answers must be in* ***lexical order****.*

Good luck!

PLEDGE:

On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_______________ _______________ _______________

PRINT YOUR NAME SIGN YOUR NAME DATE

COMMENTS, FEEDBACK, or any special instructions for the professor:

Page	Available	Points
1	0	0
2	7	
3	14	
4	10	
5	25	
6	15	
7	16	
8	12	
TOTAL	100	

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[7%] 1. Your beloved uncle's favorite number is 37. You therefore decide to make him a box to contain his birthday present for his 37th birthday. The important thing is not what is in the box, but the box itself. Since Uncle Henry is an eccentric math professor, you decide to use your new knowledge of number systems to create a box lock using only the number 37 in the combination. The trick is to use varying representations of this number.

2 min

(4%) a) Determine the hexadecimal, octal, binary, and BCD representations of the decimal number 37.37 . (Only two digits to the right of the point are required.)

3 min

Binary: ____________________

Octal: ____________________

Hex: ____________________

BCD: ____________________

(3%) b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -37.

2 min

Signed Mag: __________________

1's Comp: __________________

2's Comp: __________________

You can now design your lock using all the above numbers. Let's see how sharp Uncle Henry really is!

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[6%] 3 min 2. Your new boss, Mr. Cliff Claven, has a problem with truth (tables). Please determine the canonical SOP **or** POS (no minimization) for **each** of the outputs in below truth table.

S	A	M	D	I	N
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	0	0
1	1	1	0	0	1
1	1	1	1	1	1

I = ______________________________

____

____

____

N = ______________________________

____

____

____

[8%] 5 min 3. Simplify the below Boolean expression **using Boolean algebra**.

$$Z = A\overline{C}(B + D) + \overline{B}\ \overline{D} + C$$

Z = ______________________

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[10%] 4. Answer the following questions for the below equation:

$$W = (\overline{A} + \overline{B} + \overline{C}) * (A + \overline{B} + C) * (A + \overline{B} + \overline{C})$$

(6%) a) Determine the MSOP and MPOS. Use the below Karnaugh maps (K-maps) to solve this problem.

$\boxed{\text{4 min}}$

A

BC

W_{MSOP}

A

BC

W_{MPOS}

W_{MSOP} = ________________

W_{MPOS} = ________________

(4%) b) The only signals available for implementing the design are A, B, and C, i.e., no complement terms are available. Which solution costs less? Justify your answer by drawing a circuit for each of the above two designs.

$\boxed{\text{3 min}}$

Minimum cost (circle one): MSOP MPOS

____

____

____

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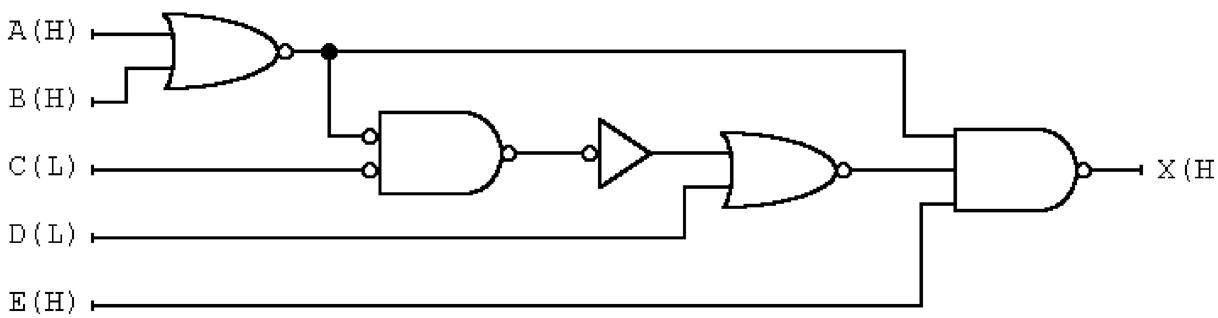
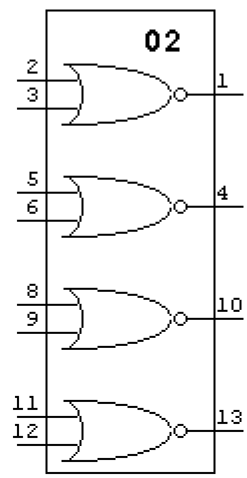
[10%] 5. Determine the equation implemented with this circuit. Do **not** minimize the equation. It is **not** necessary to put the equation in lexical order. Label the mixed-logic equation at **each** intermediate signal on this circuit.

3 min



X = ____



[15%] 6. Directly implement the below equation with a mixed-logic circuit diagram. Use only gates on 74'02 chips (shown to the right). Label all gates and **pin numbers** as you should be doing in lab. Pick whatever activation levels you want for the inputs, but make the output Y active-low.

5 min

$$Y = (A * B * \overline{C} + D) * \overline{\overline{E}\ F}$$

A( )__

B( )__

C( )__

D( )__

E( )__

F( )__

__Y(L)

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[15%] 7. You are trapped on an island with a couple of sailors, an actress, a wealthy elderly couple, and a farm girl. You have 1100 meters of wire, all the TTL chips you can possibly use, several power supplies, 37 binary switches, and several Prototype Boards.. (The electronic components washed up on shore along with a space capsule after a particularly bad storm.) You need to transmit seven binary signals (outputs of the seven binary switches shown below left) from the beach lookout point to the camp, 200 meters away. The camp has 7 active-low lights which should indicate which, if any, of the 7 switches were pressed. **Design a circuit** to accomplish this task. **Mark each long wire** with its length to be sure you don't need more than the available 1100 meters. Label each chip with its name (number not necessary), e.g., MUX, XOR, etc..

3 min

7 min

Beach side | Camp Side

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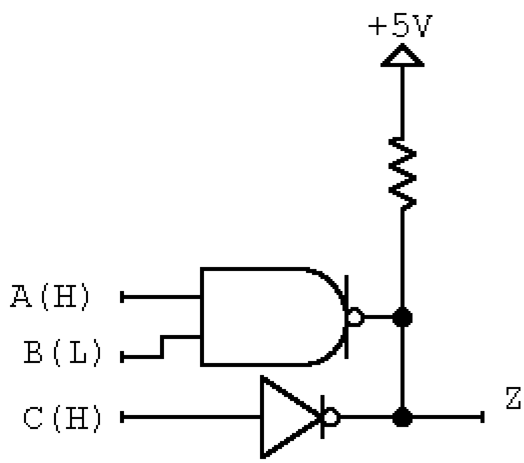
[10%] 8. Design a complete circuit to implement the below equation. You may use **only one single chip** (that has been discussed in this course). You do not need to know the chip number. Both active-high **and** active-low versions of all inputs are available. Label the activation level of all signals, e.g., A(L) or B(H). The output may be active-high or active-low. Do **not** simplify the equation.

4 min

$$T = \overline{A}B + \overline{B}\ \overline{C} + ABC$$

[6%] 9. Analyze this open-collector circuit.



(3%) a) Determine the equation for Z active-low.

1 min

Z(L) = ____________________________

(3%) b) What is the equation if you interpret Z as active-high?

1 min

Z(H) = ____________________________

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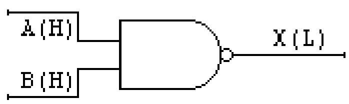
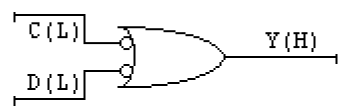
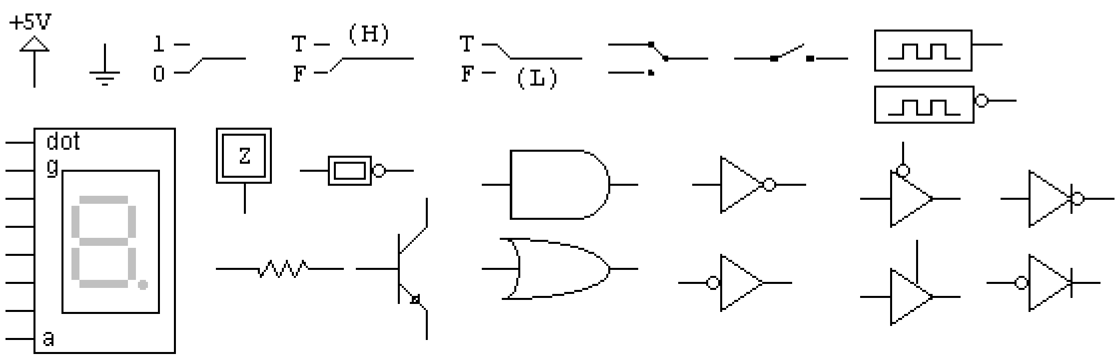
[6%]
2 min

10. Attach the appropriate input and output devices to the below two gates so that you can demonstrate each of their functions using **<u>purely</u> mixed-logic** in LogicWorks™.





These are the available library of parts you may use for the above problem:

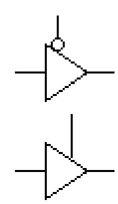


[6%]
2 min

11. Use as many of the gates **to the right** as necessary to implement the function:

$$H = EL + \overline{L}P$$

The inputs are all active-high and the output is active-high.



L(H)____

E(H)____ ____H(H)

P(H)____