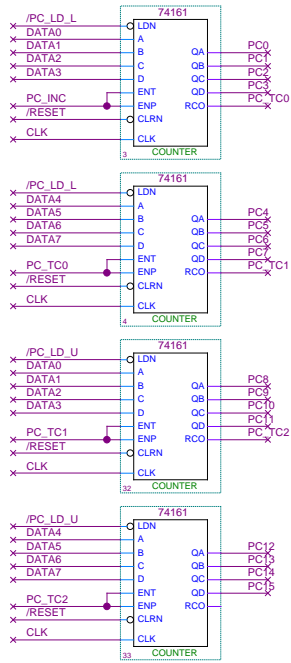


Date: November 10, 2010

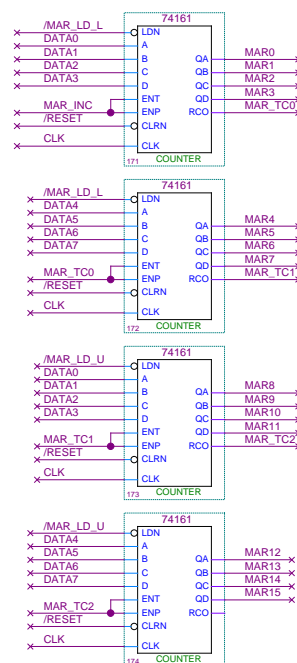
//mil.ufl.edu/ems/eel/3701/gcpu/gcpu-f10/pc\_mar\_ix/pc\_mar\_ix.bdf

Project: computer

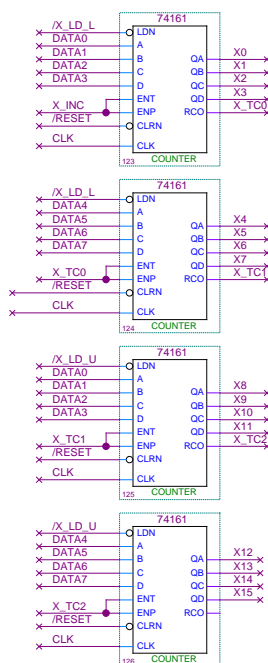
### Program Counter Register



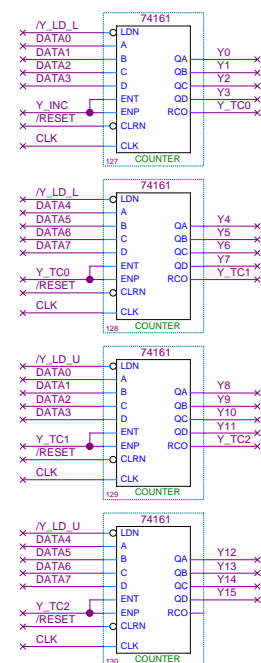
### Memory Address Register



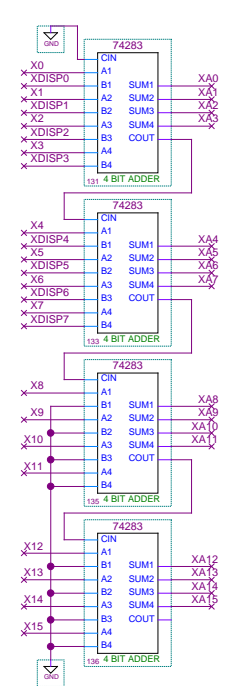
## X Index Register



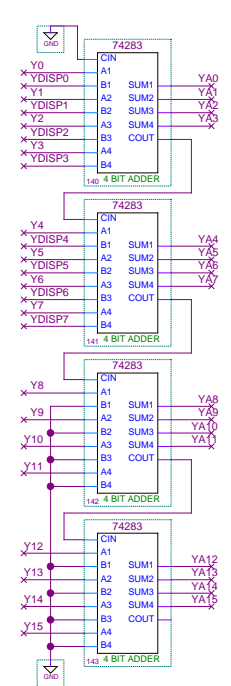
### Y Index Register



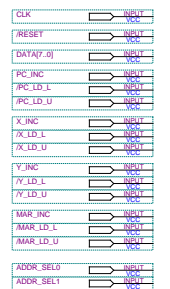
X Displ. Generation



## Y Displ. Generation

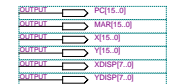


### Input / Output Signals



ADDR_SEL1:0	Addr Output
0 0	PC Register
0 1	MAR Register
1 0	X + Displ.
1 1	Y + Displ.

## Debug Signals



### Address Selection/Generation

