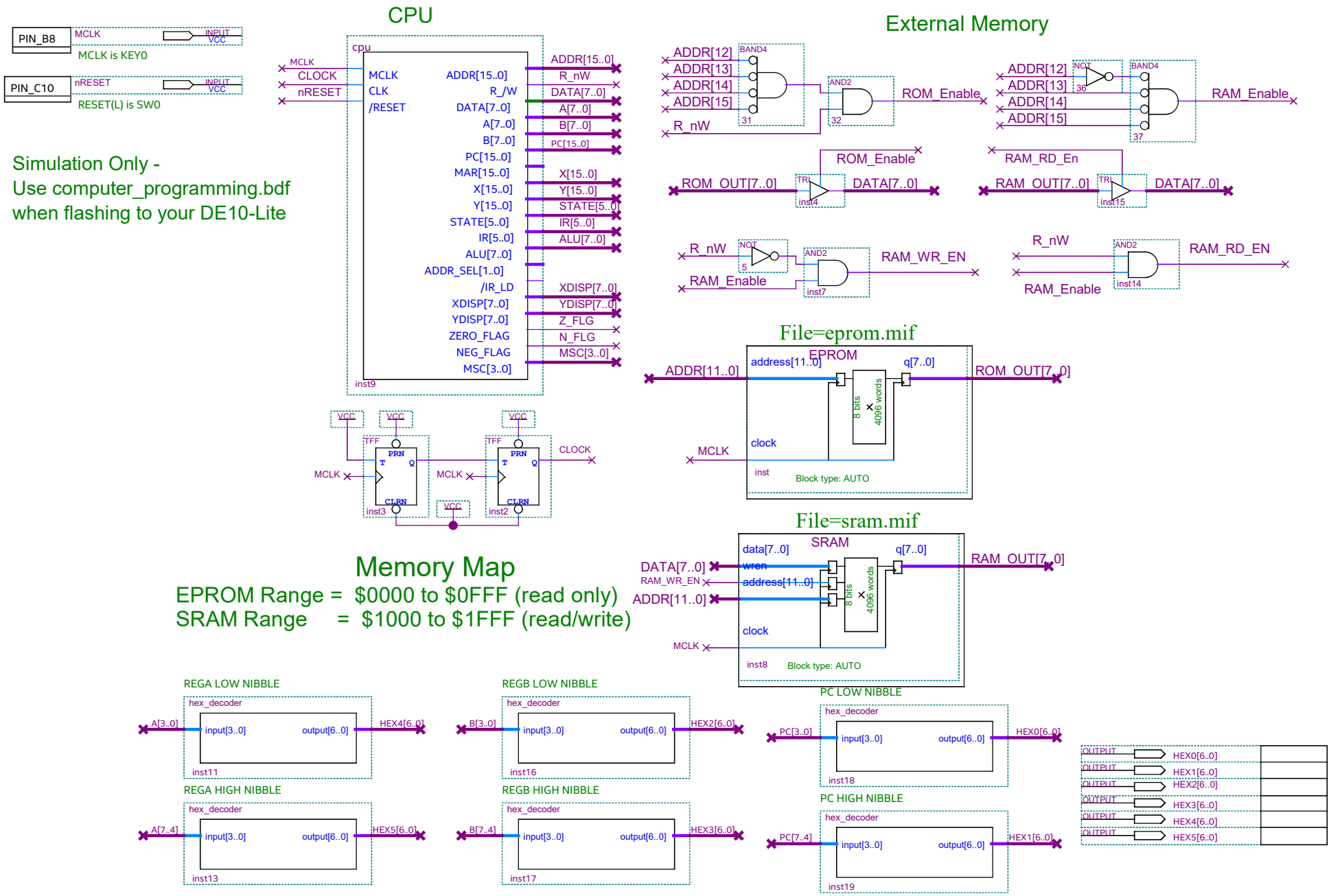
PIN_B8
MCLK
INPUT
VCC
MCLK is KEY0
PIN_C10
nRESET
INPUT
VCC
RESET(L) is SW0
Simulation Only -
Use computer_programming.bdf
when flashing to your DE10-Lite
CPU
cpu
MCLK
CLOCK
nRESET
MCLK
CLK
/RESET
ADDR[15..0]
R_/W
DATA[7..0]
A[7..0]
B[7..0]
PC[15..0]
MAR[15..0]
X[15..0]
Y[15..0]
STATE[5..0]
IR[5..0]
ALU[7..0]
ADDR_SEL[1..0]
/IR_LD
XDISP[7..0]
YDISP[7..0]
ZERO_FLAG
NEG_FLAG
MSC[3..0]
ADDR[15..0]
R_nW
DATA[7..0]
A[7..0]
B[7..0]
PC[15..0]
X[15..0]
Y[15..0]
STATE[5..0]
IR[5..0]
ALU[7..0]
XDISP[7..0]
YDISP[7..0]
Z_FLG
N_FLG
MSC[3..0]
inst9
VCC
TFF
PRN
T
Q
CLRN
MCLK
inst3
inst2
CLOCK
External Memory
ADDR[12]
ADDR[13]
ADDR[14]
ADDR[15]
R_nW
BAND4
31
AND2
32
ROM_Enable
NOT
36
37
RAM_Enable
ROM_OUT[7..0]
TRI
DATA[7..0]
inst4
RAM_RD_En
RAM_OUT[7..0]
inst15
5
RAM_WR_EN
inst7
inst14
File=eprom.mif
EPROM
ADDR[11..0]
address[11..0]
q[7..0]
ROM_OUT[7..0]
8 bits
4096 words
clock
inst
Block type: AUTO
File=sram.mif
SRAM
data[7..0]
wren
address[11..0]
DATA[7..0]
RAM_WR_EN
ADDR[11..0]
inst8
Memory Map
EPROM Range = $0000 to $0FFF (read only)
SRAM Range = $1000 to $1FFF (read/write)
REGA LOW NIBBLE
hex_decoder
A[3..0]
input[3..0]
output[6..0]
HEX4[6..0]
inst11
REGB LOW NIBBLE
B[3..0]
HEX2[6..0]
inst16
PC LOW NIBBLE
PC[3..0]
HEX0[6..0]
inst18
REGA HIGH NIBBLE
A[7..4]
HEX5[6..0]
inst13
REGB HIGH NIBBLE
B[7..4]
HEX3[6..0]
inst17
PC HIGH NIBBLE
PC[7..4]
HEX1[6..0]
inst19
OUTPUT
HEX0[6..0]
HEX1[6..0]
HEX2[6..0]
HEX3[6..0]
HEX4[6..0]
HEX5[6..0]