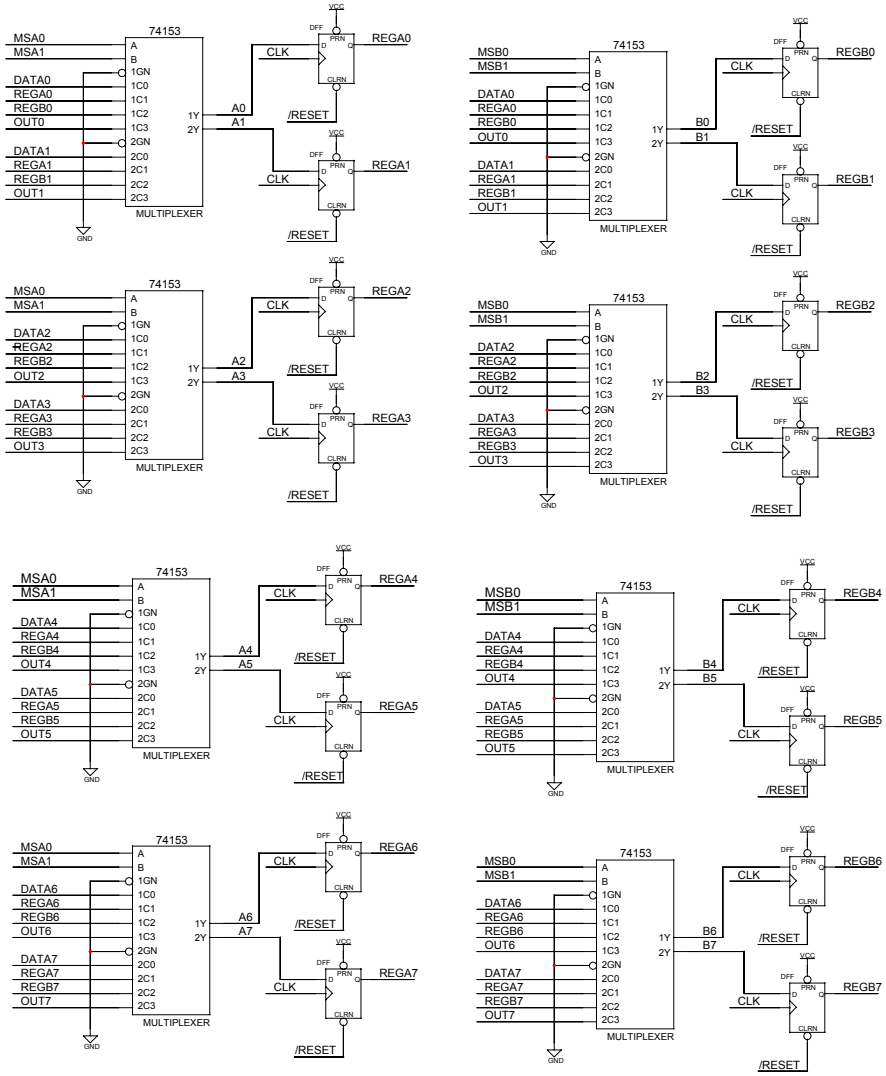
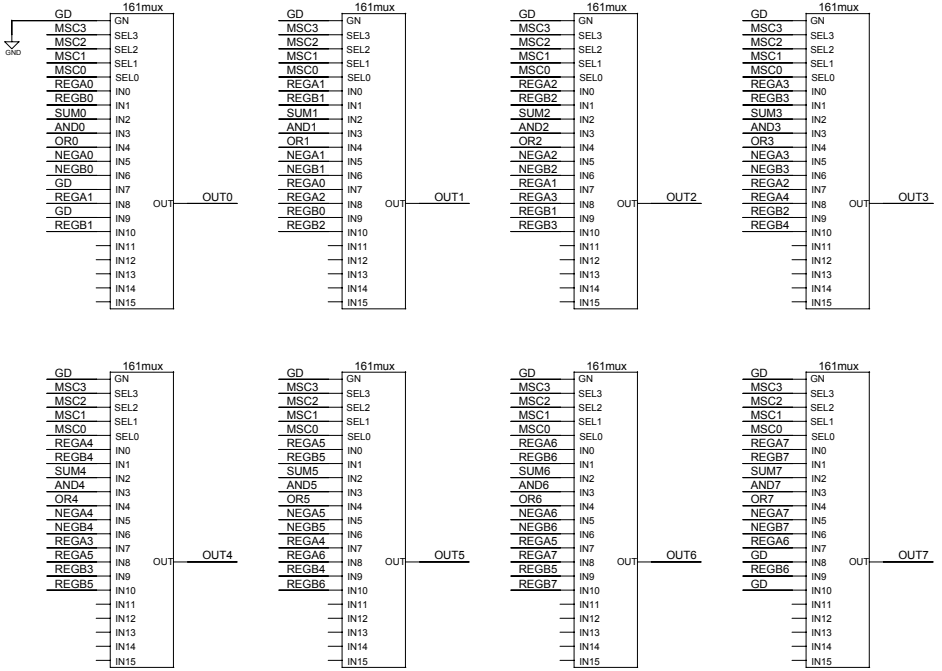
Mux A, Mux B, Reg A, Reg B Block

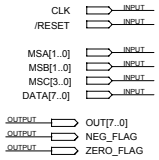


Mux C Block

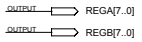


MSC3:0	Selection
0 0 0 0	REGA
0 0 0 1	REGB
0 0 1 0	Sum(A,B)
0 0 1 1	AND(A,B)
0 1 0 0	OR(A,B)
0 1 0 1	COMA
0 1 1 0	COMB
0 1 1 1	SHFA_Left
1 0 0 0	SHFA_Right
1 0 0 1	SHFB_Left
1 0 1 0	SHFB_Right

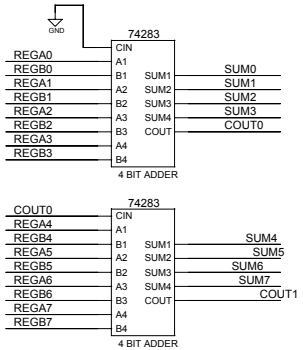
Input & Output Signals



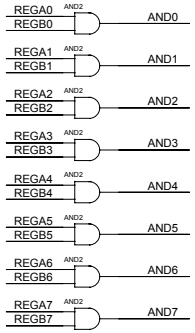
Debug Signals



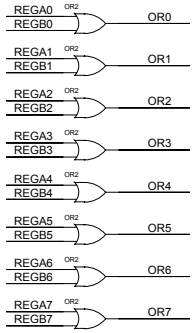
Sum & Carry Flag Generation



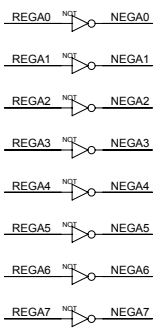
AND Generation



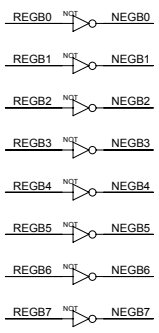
OR Generation



Negate A



Negate B



Z & N Flag Generation