

EEL 4712: DIGITAL DESIGN

<http://mil.ufl.edu/4712/>

INSTRUCTOR Dr. Eric M. Schwartz Office: MAEB 321 Phone: 392-2541 Email: ems@mil.ufl.edu
 Office Hours: Mon period 8 (3-3:50pm), Wed period 6 (12:50-1:40pm)

LECTURES Tues, 8th-9th periods (3pm) in MAEB 229, Thur, 9th period (4:05pm) in WEIM 1094

LAB SECTIONS (NEB 281)

1361 M 9-11 (Rishi)	1527 W 9-11 (Carlo)	1528 W E1-E3 (Carlo)	1525 Th 6-8 F 10-E1 (Rishi)
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CATALOG DESCRIPTION (ABET Design Content 50%) [Lab fee: \$40.98]
 Advanced modular logic, design languages, finite state machines and binary logic.

PREREQUISITES

EEL 3701 (and CGS 3422 is a prerequisite for EEL 3701). Basic digital design and a working knowledge of one high level programming language (such as FORTRAN, BASIC, PASCAL or C) and an acquaintance with assembler language are assumed.

TEXTBOOK AND SOFTWARE

Brown, S. D. and Vranesic, Z. G., "Fundamentals of Digital Logic with VHDL Design with CD-ROM, 2nd Edition", McGraw-Hill, 2005. (ISBN: 0072499389) (I have not seen the new 3rd edition [ISBN: 13 9780077221430], so I do not know if it is equivalent.)

Previous edition: Brown, S. D. and Vranesic, Z. G., "Fundamentals of Digital Logic with VHDL Design", McGraw-Hill, 2000 (ISBN: 0072460857)

- Textbook web site: <http://catalogs.mhhe.com/mhhe/viewProductDetails.do?isbn=0072499389>.
- E-book version web site: <http://www.zinio.com/offer?issn=0072460857&of=MHHE01>. \$78.89

Altera's *Quartus*. A very old version is available in the textbook. The most recent version is free and available on Altera's web site (<http://www.altera.com/>). As of today, the latest version is Quartus II Web Edition v8.0, Service Pack 1.

HARDWARE REQUIREMENTS

A custom board designed at UF is required. **The price is rolled into your course fees.** Over the last several years, students purchased their boards from an independent company for approximately \$120. You will also need your *Byte Blaster* that you used in EEL 3701. If you don't have a Byte Blaster or would like a USB Byte Blaster, the UF Bookstore has them for \$50. You will also need your **own laptop PC** for use in lab and possibly during the exams.

REFERENCES See <http://mil.ufl.edu/4712/references.html> for references.

OFFICE HOURS

You may see any TA for consultation (in NEB 281), not just the one teaching your lab section. I will hold office hours (as shown above) or by appointment. If you come by at any other time, I reserve the right to say, "I'm busy," although I rarely say this (even though it's invariably true). You are encouraged to use e-mail to communicate with the instructor and the TAs.

TA Office hours in NEB 281

TA name	Carlo Pascoe	Rishi Panjwani
office hours	Mon, per 6-7	Fri, per 8-9
open hours	Wed, per 7	Mon, per 5
e-mail	poppyc@ufl.edu	rrishi@ufl.edu

HANDOUTS: Most handouts are supplied on-line and can be downloaded from the class web site: <http://mil.ufl.edu/4712/>. If you miss a class in which a paper handout is given, you may pick it in our Lab (in NEB 213-A). Please **do not** ask the instructor or a TA for handouts. Old assignments not picked up during class will also be placed on this table.

EXAM SCHEDULE

There will be 3 exams and a comprehensive final exam. Changes to these dates, if necessary, will be announced as soon as possible.

EXAM	DATE	TIME	LOCATION
Exam 1	Tues, 7 Oct	In Class	In Class
Exam 2	Tues, 4 Nov	In Class	In Class
Exam 3	Tues, 2 Dec	In Class	In Class
Final Exam	Sat, 13 Dec	12:30 pm*	—

*Tentatively scheduled time

MULTIMEDIA CLASS/AUDIENCE HANDOUTS

Audience notes are normally from the class web site every week or so for the subsequent week or more of classes. The notes consist of copies of the class PowerPoint slides with some space for note taking. These notes are not required but are **highly** recommended. Check the class web site for information on exactly when the notes are available. **For optimal performance**, read the notes and examples for a class **before** that class (when available) and bring the **printed class notes and examples** to class to augment the printed material with your own notes. Notes will be removed shortly after they are covered in class.

COURSE REQUIREMENTS

1. Perform all laboratory experiments. A grade of 65% or better in Lab is **required** in order to obtain a passing grade. Your lowest lab will be dropped. But use this drop wisely, i.e., do **not** just skip a lab since all labs are important and your next missed lab may be unavoidable. If you need to miss a single lab, it's ok; you can **not** make up the missed lab. (You should do this lab on your own.) **If you have a valid reason for missing this lab, get documentation for your first missed lab and hold on to it.** If you miss a **second** lab, you must show the **professor** (not the TA) **written documentation for BOTH your first and your second missed labs.** This documentation should be official and from a doctor, judge, etc., so that a make-up can be arranged. You must notify the professor **prior** to your scheduled second missed lab or **as soon as possible after** your second missed lab. **There is no excuse that will allow you to reschedule your first missed lab other than an assembly exam in another course.**
 - Labs **must** be done at scheduled times.
 - An average lab grade of **65% or higher** is required to be **eligible** to **pass** the class!
2. Do all homework assignments. Late homework is **not** accepted. Do all scheduled and unscheduled quizzes.
3. Take 3 during-term exams and a comprehensive final exam. No makeup exams will be given except for medically documented incapacity or family emergency.

HOMEWORK AND EXAM SOLUTIONS: Solutions to some of the homework may be made available on our class web-site. Exam solutions will not be posted, but will be discussed in class on the day the graded exams are returned to the class.

HOMEWORK GRADING: Homework (if any) are due at the **start** of the class period. Late homework is **not** be accepted.

LABORATORY GRADING: See the *Laboratory Guidelines* given below.

EXAM RE-GRADE POLICY: If you believe an error has been made on an exam score you must make a **written** request to me explaining where the misgrading or error occurred. This request must be submitted **at the end of the class in which the exam is returned.** If you do resubmit an exam, however, I reserve the right to scrutinize and grade the entire exam more closely. This definitely places your current score at risk. Consequently, it is not advisable to resubmit an exam for correction unless a blatant error, such as a miscalculation of total points, has been made.

All grades are **non-negotiable one week** after the grade is posted. Please don't come to me after the final grades have been posted with a hard-luck story.

COURSE GRADE DETERMINATION

- | | | |
|-------------------------------|--------|--|
| • Exams @ (13.3-15%) x 3 | 40-45% | |
| • Laboratory | 30%* | (not all labs are weighted equally; grade of 65% required to pass) |
| • (Pop) Quizzes | 0-5% | (0-10 scheduled and unscheduled quizzes) |
| • Homework | 0% | (there will be between 0 and 12 homework assignments) |
| • <u>Comprehensive Final*</u> | 25% | (If $Final \geq 90$, then $Grade \leftarrow Grade + \frac{1}{2} Letter$. For some, final optional) |
| • Total | 100% | |

* A grade of 65% or better in Lab is **required** in order to obtain a passing grade. Your lowest lab will be dropped. But use this drop wisely, i.e., do **not** just skip a lab since all labs are important and your next missed lab may be unavoidable. If you need to miss a single lab, it's ok; you can **not** make up the missed lab. (You should do this lab on your own.) **If you have a valid reason for missing this lab, get documentation for your first missed lab and hold on to it.** If you miss a **second** lab, you must show the **professor** (not the TA) **written documentation for BOTH your first and your second missed labs.** This documentation should be official and from a doctor, judge, etc., so that a make-up can be arranged. You must notify the professor **prior** to your scheduled second missed lab or **as soon as possible after** your second missed lab.

Note: All grading percentages are subject to change at professor's discretion. Students will be notified of any changes.

Part of your grade on tests, quizzes, labs, etc. is based not only on solving the problem you are presented with, but the manner in which you solve it. For example, there is a difference between two programs that meet the given specifications, but one is an elegant, extensible 20-line solution, while the other is an obfuscated 100-line program that also meets the specifications but would be difficult to extend later. Just as your future employer would value the latter program less than the first, so will I in grading your exams.

CHEATING: CHEATING WILL NOT BE TOLERATED. We will actively search for cheaters. If you are caught, there will be no negotiations. You will fail the course and get reported to the honor court. There are **no excuses and no exceptions.** You may talk to other students about homework assignments and labs, but the final work **must** be your own. If you are caught cheating on **any** assignment (homework, lab, quiz or exam), the **smallest** penalty possible is failure of the course. During a 2004 semester many students were caught with partly copied lab assignments. If this happens this semester, the students will earn an "E" in the course. A meeting with the instructor will determine **additional penalties**, none of which are desirable or pleasant (i.e., cheating in this course will result in a failing grade in the course, initiation of honor court charges, and possibly expulsion from the university). If you know some one is cheating, **it is your responsibility to report it.** We have and will continue to prosecute cheaters by turning them over to the office of Student Judicial Affairs. For more information about cheating, see the URLs: <http://www.dso.ufl.edu/judicial/>.

WORKING TOGETHER

You are encouraged to work with other students on homework assignments (**absolutely forbidden on labs**) in a professional manner. Each person in the group should attempt to solve all problems **independently** and **only** then discuss the results with

one's partner(s) to correct errors and resolve differences. Copying your partner's work without a serious attempt on your part constitutes cheating and should not be permitted by your partner(s). Matching your solution to your partner's, however, is acceptable, if, after independent study and work you are convinced your partner's solution is correct. All solutions should reflect your style of problem solving, even those you have changed to match your partner's solution. In other words, **verbatim copying or simple paraphrasing of your partner's solution is not an acceptable form of cooperative study.** Your name and your partner's name(s) must be on your homework. You must do independent work on labs. See *Laboratory Guidelines* below.

MAJOR COURSE TOPICS (not necessarily in the order in which they are discussed):

1. Introduction
 - a) Review of combinational network design
 - i) Boolean Algebra (plus SOP, POS, Truth Tables)
 - ii) Minimization (K-Maps, other techniques)
 - iii) Mixed-logic representation (Direct Polarity Indication)
 - b) Digital Logic Elements as Electronic Devices (Circuit Fabrication Considerations)
 - c) Introduction to Programmable (Array) Logic Devices
 - i) Device architectures for PALs, PLAs and PROMs
 - ii) Design software for combinatorial networks – Behavioral VHDL
 - iii) Altera's Quartus (VHDL, Simulation, Signal Tap LSA
 - iv) Structural VHDL
2. Study of commonly-used combinational networks
 - a) Design equations for MUXes, Encoders, Decoders, 7-Segment Displays, Adders (HA and FA), ALUs, etc.
 - b) Address Decoding
 - c) ROMs for logic
 - d) The Look-Ahead Carry and the Multi-Bit Full Adder
 - e) Multi-bit Combinatorial Multiplier and the Carry-Save Adder
 - f) Physical implementations of these networks
3. Chip specifications and timing diagrams
 - a) TTL, CMOS and ECL Specs
 - b) Interfacing TTL, CMOS, and ECL
 - c) Propagation Delays
4. Computer assisted network design
 - a) Generation of truth tables by computer
 - b) Design software - logic assemblers and simulators
 - c) Testing the design and the implementation - test vectors
 - d) Logic State Analyzers
5. Review of clocked networks
 - a) Flip-Flops - in particular edge-triggered D flip-flops
 - b) Counters and Shift registers
 - c) Sequencers
 - d) Memories - RWM (RAM) and ROM (EPROM, EEPROM)
6. Design Methods for Synchronous Finite (Algorithmic) State Machines (FSM or ASM)
 - a) The ASM diagram (Mealy and Moore machines)
 - b) State assignment or no state assignment?
 - c) The VHDL State Machine design tools
 - d) Implementation methods - traditional, MUX, ROM/Latch
 - e) Implementation method – PALs, CPLDs, FPGA's
 - f) Using Altera's Quartus
7. Finite State Machine Design Examples
 - a) Successive-approximation Analog-to-Digital Converter (and D/A converters)
 - b) 8-bit Parallel-to-Serial and Serial-to-Parallel Converter (Asynchronous Serial Input/Output)
 - i) Serial Communication
 - ii) ASCII
 - iii) RS-232 (EIA-232D) standard (with DB-25 and DB-9 connectors)
 - c) Scanned Keypad Controller
 - d) Waveform Generator
 - e) Dynamic RAM Controller
 - f) Keyboard Controller
 - g) VGA Monitor Controller
 - h) Small computer
8. Time permitting
 - a) Pulse Width Modulation
 - b) Output and Input Timing (OC/IC)
 - c) Timing and Hazards (function and logic)
 - d) Asynchronous Design

Day of First Labs (see Schedule on next page)

Monday	Wednesday	Thursday Friday
3, 6	0, 1, 2, 7	4, 5, 8

POSSIBLE LAB TOPICS

- Lab 0: Intro to equipment & Cascading Synchronous Counters
- Lab 1: Intro to equipment & Cascading Synchronous Counters
- Lab 2: 7-Segment Display and Adders
- Lab 3: Look-Ahead Carry Adders and Structural VHDL
- Lab 4: ALU and Accumulator Register
- Lab 5: Counters and VGA Display
- Lab 6: Switch Debouncing and Serial Keyboard
- Lab 7: Video Memory and VGA
- Lab 8: Simple computer

EEL 4712C SCHEDULE

WEEK/DAY	DATE	Class	Lab / Notes
1 M	25-Aug		(Classes Begin)
1 Tu	26-Aug	1-2	
1 W	27-Aug		
1 Th	28-Aug	3	
1 F	29-Aug		
2 M	1-Sep	No class	Holiday: Labor Day
2 Tu	2-Sep	4-5	
2 W	3-Sep		0
2 Th	4-Sep	6	0
2 F	5-Sep		0
3 M	8-Sep		0
3 Tu	9-Sep	7-8	
3 W	10-Sep		1
3 Th	11-Sep	9	+
3 F	12-Sep		1
4 M	15-Sep		1
4 Tu	16-Sep	10-11	
4 W	17-Sep		2
4 Th	18-Sep	12	2
4 F	19-Sep		2
5 M	22-Sep		2
5 Tu	23-Sep	13-14	
5 W	24-Sep		
5 Th	25-Sep	15	
5 F	26-Sep		
6 M	29-Sep		3
6 Tu	30-Sep	16-17	
6 W	1-Oct		3
6 Th	2-Oct	18	3
6 F	3-Oct		3
7 M	6-Oct		
7 Tu	7-Oct	19-20	Exam 1 (in class)
7 W	8-Oct		
7 Th	9-Oct	21	4
7 F	10-Oct		4
8 M	13-Oct		4
8 Tu	14-Oct	22-23	
8 W	15-Oct		4
8 Th	16-Oct	24	5
8 F	17-Oct		5

WEEK/DAY	DATE	Class	Lab / Notes
9 M	20-Oct		5
9 Tu	21-Oct	25-26	
9 W	22-Oct		5
9 Th	23-Oct	27	
9 F	24-Oct	No Class	Holiday: Homecoming
10 M	27-Oct		6
10 Tu	28-Oct	28-29	
10 W	29-Oct		6
10 Th	30-Oct	30	6
10 F	31-Oct		6
11 M	3-Nov		
11 Tu	4-Nov	31-32	Exam 2 (in class) Election Day
11 W	5-Nov		
11 Th	6-Nov	33	
11 F	7-Nov		
12 M	10-Nov		
12 Tu	11-Nov	No class	Holiday: Veteran's Day (Election Day)
12 W	12-Nov		
12 Th	13-Nov	34	
12 F	14-Nov		
13 M	17-Nov		
13 Tu	18-Nov	35-36	
13 W	19-Nov		7
13 Th	20-Nov	37	7
13 F	21-Nov		7
14 M	24-Nov		7 Drop Deadline (Mon, 5pm)
14 Tu	25-Nov	38-39	
14 W	26-Nov		
14 Th	27-Nov	No Class	Thanksgiving Day
14 F	28-Nov	No Class	Thanksgiving Break
14 M	1-Dec		
14 Tu	2-Dec	40-41	Exam 3 (in class)
14 W	3-Dec		
14 Th	4-Dec	42	8
14 F	5-Dec		8
15 M	8-Dec		8
15 Tu	9-Dec	43-44	
15 W	10-Dec		8 (Classes End)
16 Sat	13-Dec		FINAL EXAM: (not as scheduled in course guide) Time: 12:30-2:30pm, Room_____.

LABORATORY GUIDELINES

Laboratory Introduction: At the beginning of each lab, the TA will give you any special instructions for that particular lab. Then you are to construct the digital circuit (or bring in your circuit already constructed) based on your prelab, debug the circuit, and demonstrate its correct performance to the TA. All circuits must be designed using Altera's *Quartus* or equivalent software and should include pin numbers on the schematics. You must bring a *Quartus* (or equivalent) printout of your circuit to lab and include the printout (or a corrected circuit drawn again with *Quartus* or equivalent) in your lab report.

Laboratory Preparation: All of the lab experiments require advanced preparation in the form of circuit designs, VHDL programs, computations and of course reading and understanding the lab handout itself. You must complete your prelab **before coming to lab to be admitted into the lab**. The prelab consists of the final wiring diagrams, truth tables, ASM charts and VHD files. If you are comfortable working with VHDL files on-line, you need only bring your flash (thumb) drive to lab, along with your *Quartus* (or equivalent) circuit and wiring diagrams printouts, etc. A well-prepared prelab is the key to finishing on time. **You must use your own laptop in EEL 4712; we do not have PCs available for student use except (possibly) in exceptional circumstances!!!**

1. *Bring your working VHDL code on media flash (thumb) drive to the lab. Simulate your design using the Quartus software before lab. Your source file(s) must be commented.*
 - Always compose, edit, test, and then save your VHDL source-code on to your media before your scheduled lab. This will save you considerable time and frustration and will improve your performance. You **must** also have a legible working printout of your commented VHDL source code.
 - Do not work from your flash drive. Use your laptop hard drive instead.
2. *Bring printed copies of the wiring diagram (mixed logic diagram), truth tables, ASM charts, spec sheets, and any other necessary documents. The wiring diagram must be created with Quartus or an equivalent package.*
3. *Simulate as much of the circuit as possible with Quartus (or equivalent) before coming to lab.*
4. *Structure your design into functional modules and comment the VHDL code while programming.*
 - Devise means for testing each part of the design separately so that problem isolation (debugging) is easily accomplished.
5. *Arrive at the lab on time to give yourself adequate time.*

Summary: Your **must** have the following at the **start** of each lab, i.e., upon entering. This will be submitted to the TA as part of your pre-lab

- Set of printouts for the TA and one for you (if relevant): Circuit diagram(s), ASM chart(s), VHDL source-code
- A flash (thumb) drive with the following: Quartus circuit diagram, VHDL source-code

Working Together:

You must do independent work on labs. Although you may *consult* with other students, TAs, or Instructors, you **must** do independent work. Consulting means "**seeking opinions or advice**" **not** getting working programs or designs, understanding them, and then modifying them to make them your own. The latter constitutes cheating (see above section). Working side-by-side to construct a program or design in a group constitutes cheating. (Solving labs are good practice for solving quizzes and exams, which are also **not** group activities.)

Laboratory Rules:

1. No food, drinks, or smoking in the Lab!
2. No student will be allowed into a lab section if they are more than 30 minutes late.
3. Keep your work area neat and clean it before you leave.
4. Students must attend labs during their assigned time.
5. No extra time will be given for those who cannot finish the experiment in the stipulated time.
6. After demonstrating your circuits to the TA, thoroughly clean up your area.

Laboratory Attendance: Laboratory attendance **during scheduled times** is mandatory. Documented personal or family emergency will be accepted as an excuse for absence for a **second** missed lab. In such cases, consult your **course instructor** (**not** your TA) about a make-up lab **as soon as possible**. You will not officially make-up your first missed lab. You should do this missed lab at home (or during TA office hours) to be sure you understand the required material.

If you cannot finish the laboratory during the allotted time, you will lose at least 10% to 30% off your final score. In general, you are expected to finish the labs on time.

Laboratory Grading: Grading emphasis will be placed upon your producing well documented, well structured designs that realize the functional requirements specified by the lab handout and the lab instructor. The remaining portion of your

grade will result from observations by your lab instructor on such matters as your understanding of the lab, your lab techniques, your prelab preparation and your cooperation and compliance with the rules. **Lab reports** are due at the start of your subsequent regularly scheduled lab. Late lab reports will **not** be accepted. You may **not** enter the lab without the necessary prelab preparations. Approximate grade guidelines (that may be changed without notification for various labs) are: **40% for pre-lab and 60% for in lab. Lab reports are graded separately. A lab report will generally count the same as a lab.** There may also be quizzes at the beginning of a lab period. Arriving late for a lab may result in a lab quiz grade of zero.

Although your lowest lab grade will be dropped, you **must** do all lab reports, i.e., lab reports can **not** be dropped.

All grades are **non-negotiable one week** after the grade is posted. Please don't come to me after the final grades have been posted with a hard-luck story.

Laboratory Reports: Most lab requires a formal written report (generated with your favorite word processor). These reports must be handed-in at the next lab period (even if you did not complete the lab), i.e., lab reports can **not** be dropped. If you miss a lab, you can still do a lab report if the lab is accomplished later. If you missed a lab but want to write a lab report for this lab, you must demonstrate the finished lab to one of the TAs who will then **sign a paper** that you will have ready for him/her at the time of your lab completion. This paper must include your name, a statement that you missed your regularly scheduled lab and that you demonstrated your **completed lab**, and the time that you demonstrated your completed lab. This paper must be included after the title page of your lab report.

The main objectives of the lab report are to document your design approach, solution technique, testing procedures, and results. The report will also demonstrate to the TA your understanding of the problem and the final solution. Please be concise. Your report should consist of the following sections:

- Purpose: Statement of the problem.
- Design: How you approached and solved the problem. Include your commented VHD file. What you did in lab. Include wiring diagrams, etc.
- Simulation: For some labs this may be included in the Design section. You **must annotate** key features of your simulation discuss them in the next section.
- Test & Verification: Experimental data collected, corresponding truth tables and state machines from your prelab, and a discussion of the results. You **must annotate** key features of your collected data and mention them in this section.
- Conclusions: Answers to questions in lab that haven't been answered yet and any additional conclusions or remarks.
 - Answering questions in the "Questions" section of the lab: Please copy the questions and answer them in this section. Clearly number them as they are numbered in the lab handout.

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Last Name: _____ First Name: _____

E-mail: _____ (please print clearly)

10-digit Password: _____ (used to retrieve grade information; please print clearly)

Your password must be 10 alphanumeric digits or less. Please save this password somewhere.