PRELIMINARY

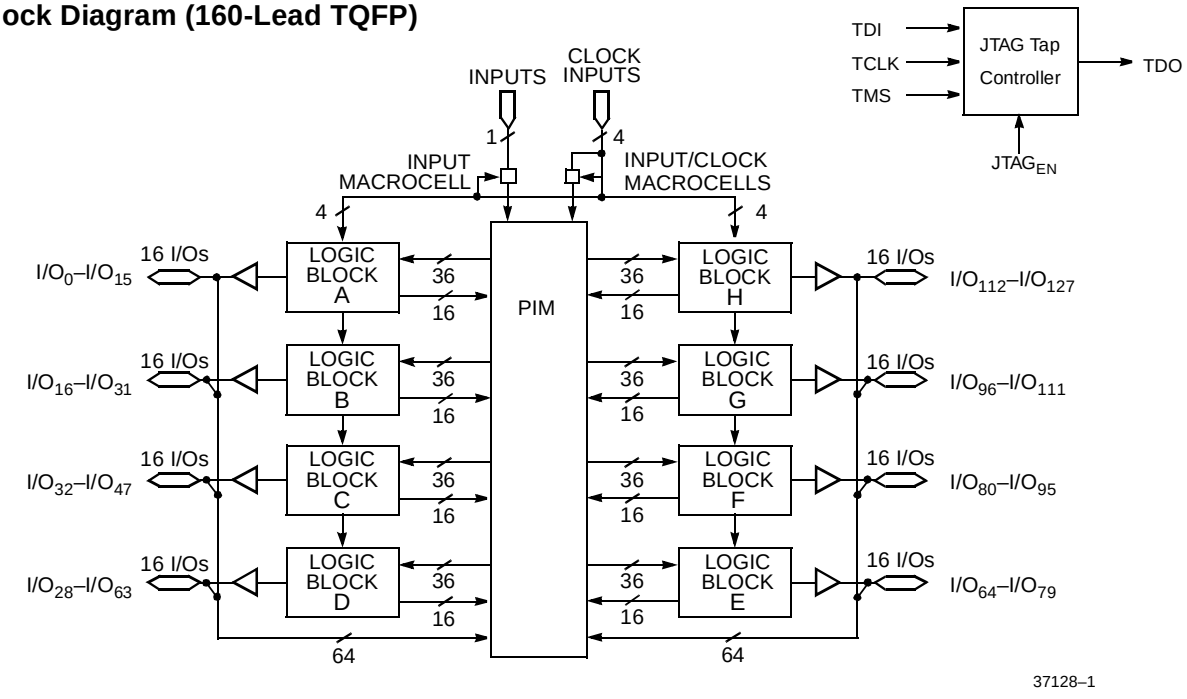
CY37128

UltraLogic™ 128-Macrocell ISR™ CPLD

Features

- 128 macrocells in eight logic blocks
- In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- Up to 128 I/Os
  - Plus 5 dedicated inputs including 4 clock inputs
- High speed
  - f_{MAX} = 167 MHz
  - t_{PD} = 6.5 ns
  - t_S = 4.0 ns
  - t_{CO} = 4.0 ns
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- 5V and 3.3V I/O capability
- User-Programmable Bus-Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant
- Available in 84-Lead PLCC and CLCC, 100-Lead TQFP and 160-Lead TQFP packages
- Pinout compatible with the CY37064/37064V, CY37128V, CY37192/37192V, CY37256/37256V, CY7C373i, CY7C374i, CY7C375i

Logic Block Diagram (160-Lead TQFP)



Selection Guide

	CY37128-167	CY37128-125	CY37128-100
Maximum Propagation Delay, t_{PD} (ns)	6.5	10	12
Minimum Set-Up, t_S (ns)	4	5.5	7.0
Maximum Clock to Output, t_{CO} (ns)	4	6.5	6.5
Typical Supply Current, I_{CC} (mA) in Low Power Mode	60	60	60

Functional Description

The CY37128 is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37128 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

# of Leads	# Buried Macrocells	# I/O Macrocells	Package Types
84	64	64	PLCC/CLCC
100	64	64	TQFP
160	0	128	TQFP

For a more detailed description of the architecture and features of the CY37128, see the Ultra37000 Family data sheet.

Fully Routable with 100% Logic Utilization

The CY37128 is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

Simple Timing Model

The CY37128 features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low Power Operation

Each Logic Block of the CY37128 can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes approximately 50% less power and slows down by t_{LP}.

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

3.3V or 5V I/O Operation

The CY37128 operates with a 5V supply, and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. A nominal timing delay is incurred on output buffers when V_{CCO} is set to 3.3V. This device requires 5V ISR programming.

In-System Reprogramming

The CY37128 can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37128 can also be programmed on a number of traditional parallel programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to the Ultra37000 Programming Kit data sheet (CY3700i).

User-Programmable Bus-Hold

All outputs of the CY37128 can either be configured into bus-hold mode or left floating. When in bus-hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

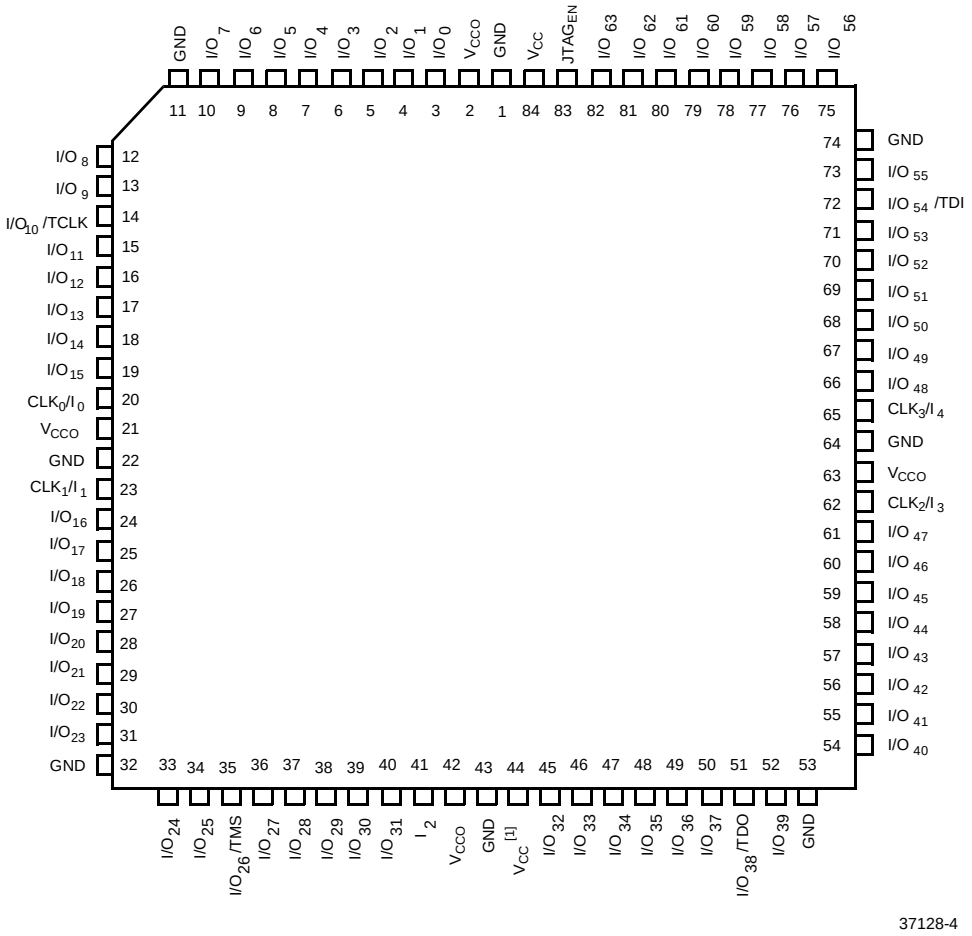
Design Tools

Development software for the CY37128 is available from Cypress's *Warp*™ or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

Pin Configurations

84-Lead PLCC (J83) / CLCC (Y84)

Top View



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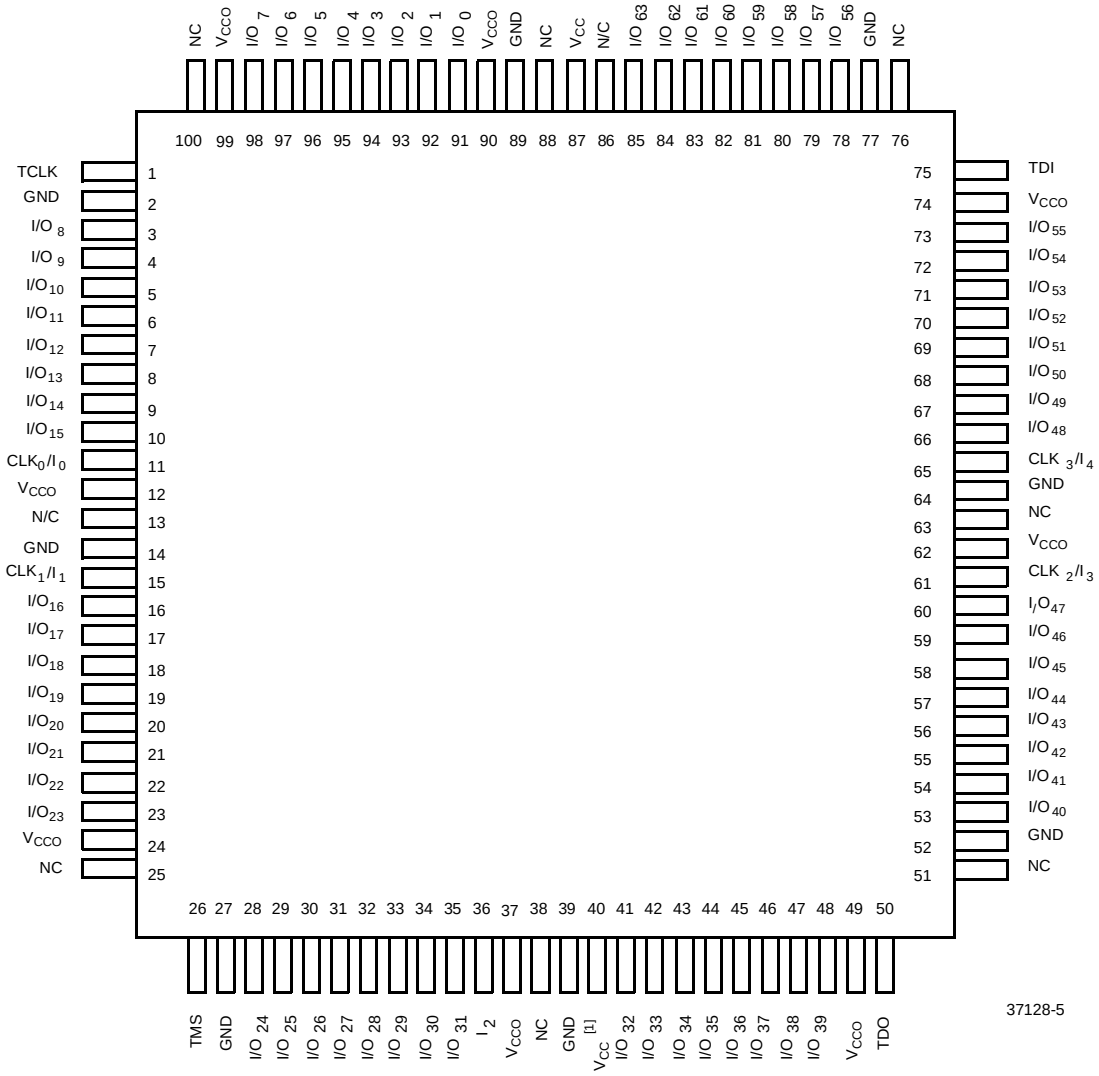
Note:

1. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

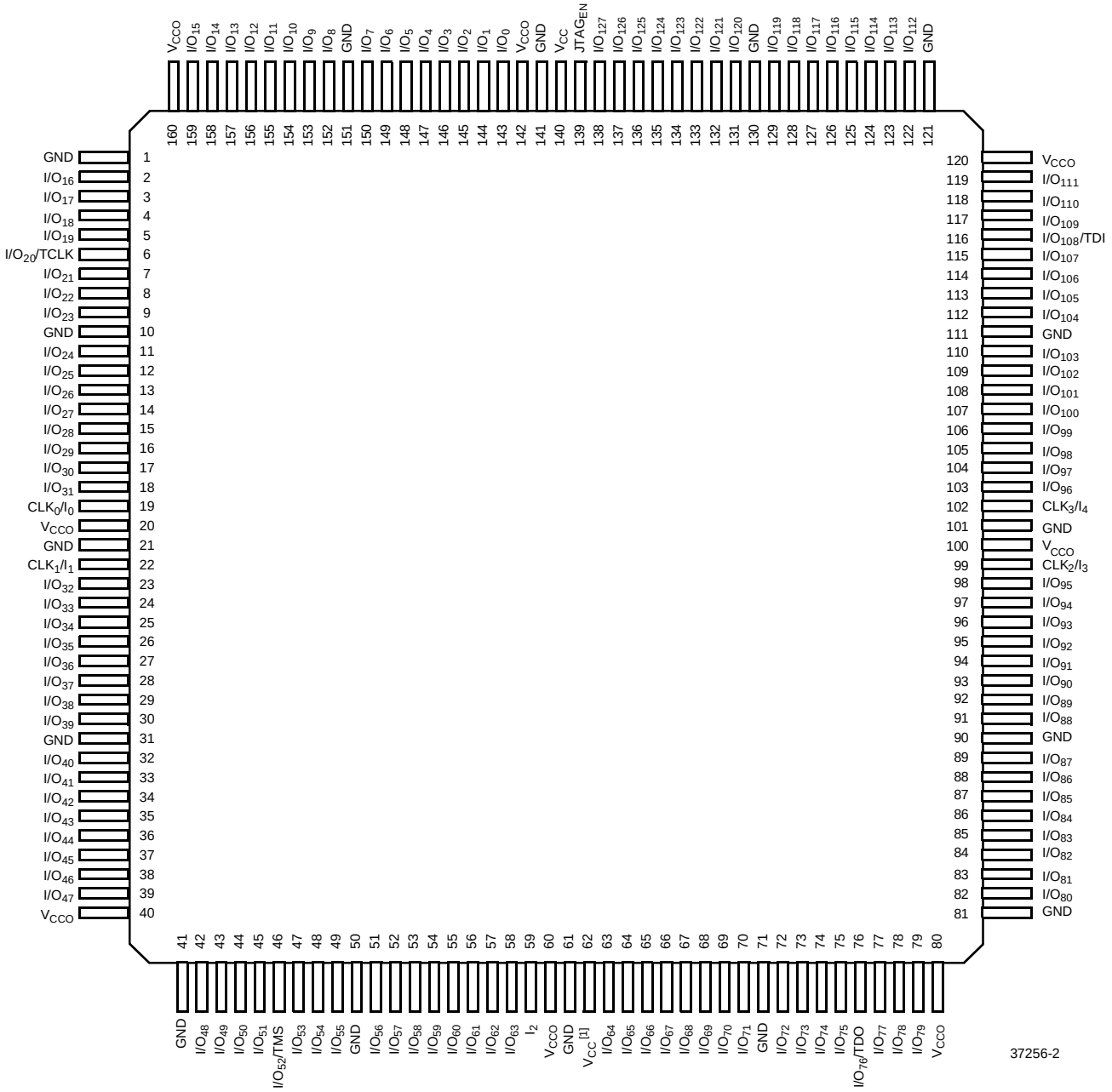
Pin Configurations (continued)

100-Lead TQFP (A100)
Top View



Pin Configurations (continued)

160-Lead TQFP (A160)
Top View



37256-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +125°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices see the Ultra37000 family data sheet.
3. T_A is the "Instant On" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[8]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[5]			4.0	V
			I_{OH} = 0 µA (Ind/Mil)[5]			4.3	V
			I_{OH} = –50 µA (Com'l)[5]			3.6	V
			I_{OH} = –100 µA (Ind/Mil)[5]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[6]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[6]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OZBH}	Output Leakage Current	V_{CC} = Max., V_O = 3.3V, Output Disabled[5], Bus-Hold Enabled		0	–70	–125	µA
I_{OS}	Output Short Circuit Current[7, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Inductance[8]

Parameter	Description	Test Conditions	160-Lead TQFP	84-Lead CLCC	84-Lead PLCC	100-Lead TQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	9	5	8	8	nH

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF

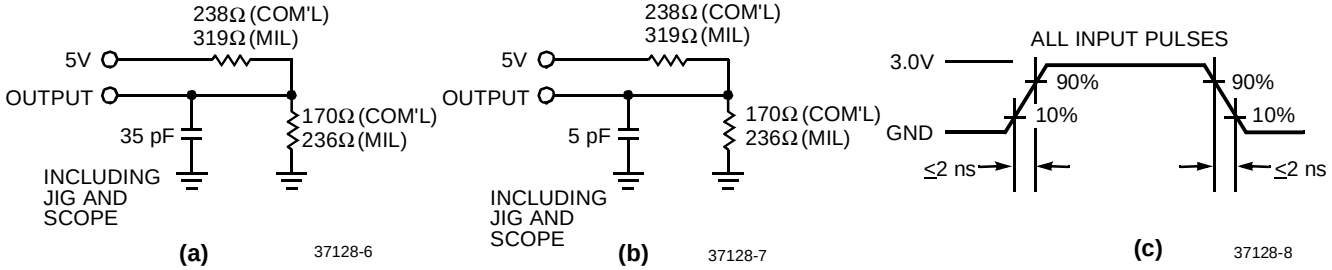
Endurance Characteristics[8]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

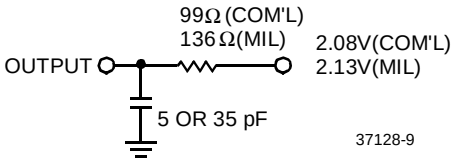
Notes:

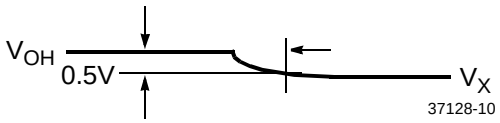
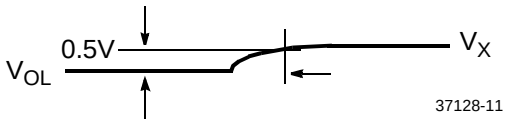
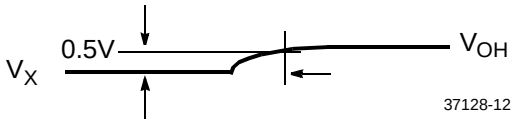
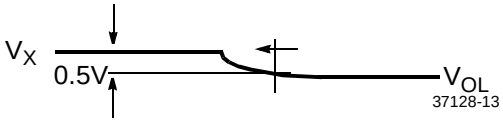
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
6. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
7. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
8. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[9]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Note:

9. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[10]

Parameter	Description	37128-167		37128-125		37128-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}[11, 12, 13]	Input to Combinatorial Output		6.5		10		12	ns
t_{PDL}[11, 12, 13]	Input to Output Through Transparent Input or Output Latch		10		13		16.5	ns
t_{PDLL}[11, 12, 13]	Input to Output Through Transparent Input and Output Latches		12		15		17	ns
t_{EA}[11, 12, 13]	Input to Output Enable		8.5		14		16	ns
t_{ER}[11]	Input to Output Disable		8.5		14		16	ns
Input Register Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time[8]	2.5		3		3		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	2.5		3		3		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		2.5		ns
t_{IH}	Input Register or Latch Hold Time	2		2		2.5		ns
t_{ICO}[11, 12, 13]	Input Register Clock or Latch Enable to Combinatorial Output		11		12.5		16	ns
t_{ICOL}[11, 12, 13]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		12		16		18	ns
Synchronous Clocking Parameters								
t_{CO}[12, 13]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output		4		6.5		6.5	ns
t_S[11]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	4		5.5		7		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}[11, 12, 13]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		10		14		16	ns
t_{SCS}[11]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	6		8.0		10		ns
t_{SL}[11]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	7.5		10		12		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	0		0		0		ns
Product Term Clocking Parameters								
t_{COPT}[11, 12, 13]	Product Term Clock or Latch Enable (PTCLK) to Output		10		13		13	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	2.5		3		3		ns
t_{HPT}	Register or Latch Data Hold Time	2.5		3		3		ns
t_{ISPT}[11]	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		-2		-2		-2	ns

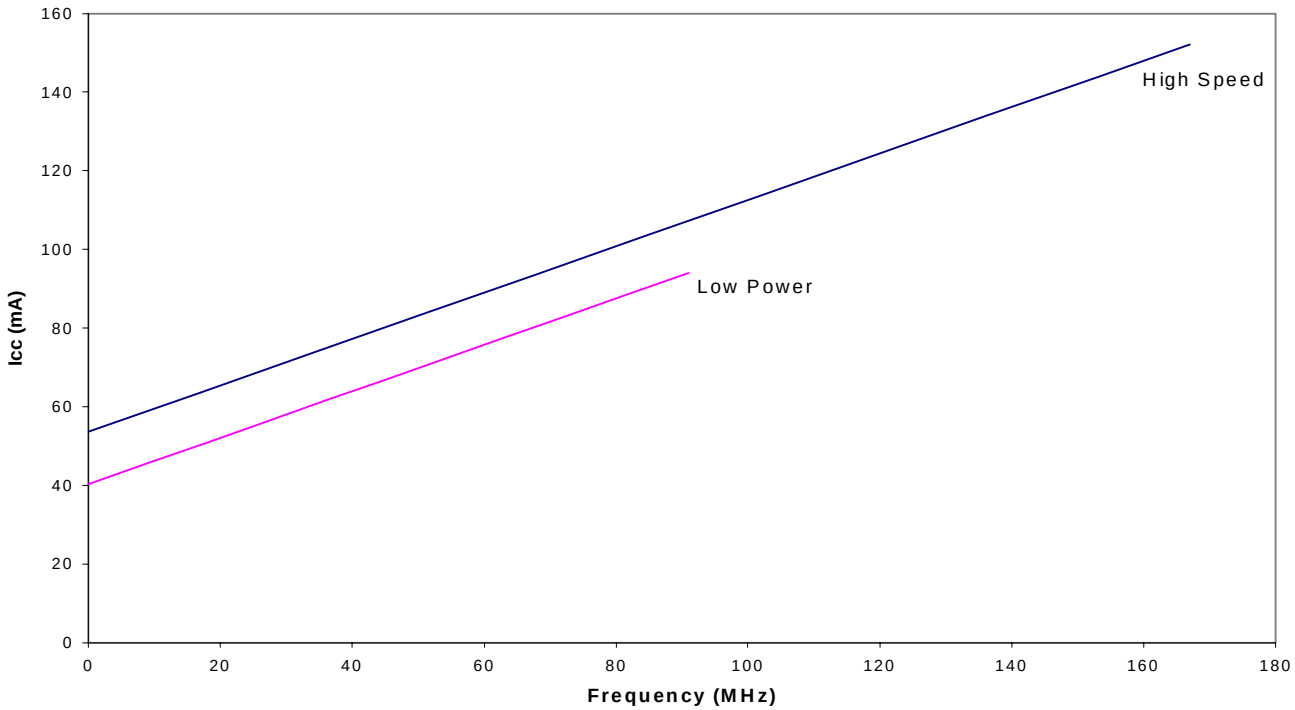
Notes:

10. All AC parameters are measured with 2 outputs switching and 35-pF AC Test Load.
11. Logic Blocks operating in low power mode, add t_{LP} to this spec.
12. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
13. When V_{CCO}= 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range[10] (continued)

Parameter	Description	37128-167		37128-125		37128-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time		6.5		9		11	ns
t_{CO2PT}[11, 12, 13]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		14		19		21	ns
Pipelined Mode Parameters								
t_{ICS}[11]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	6		8		10		ns
Operating Frequency Parameters								
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[8]	167		125		100		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[8]	200		158		153.8		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)[8]	105		83		76.9		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[8]	143		125		100		MHz
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width[8]	8		10		12		ns
t_{RR}[11]	Asynchronous Reset Recovery Time[8]	10		12		14		ns
t_{RO}[11, 12, 13]	Asynchronous Reset to Output		13		15		18	ns
t_{PW}	Asynchronous Preset Width[8]	8		10		12		ns
t_{PR}[11]	Asynchronous Preset Recovery Time[8]	10		12		14		ns
t_{PO}[11, 12, 13]	Asynchronous Preset to Output		13		15		18	ns
User Option Parameters								
t_{LP}	Low Power Adder		2.5		2.5		2.5	ns
t_{SLEW}	Slow Output Slew Rate Adder		2.5		2.5		2.5	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder[8]		0.3		0.3		0.3	ns
JTAG Timing Parameters								
$t_{S\ JTAG}$	Set-Up Time from TDI and TMS to TCK[8]	0		0		0		ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS[8]	20		20		20		ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO[8]		20		20		20	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency[8]		20		20		20	MHz

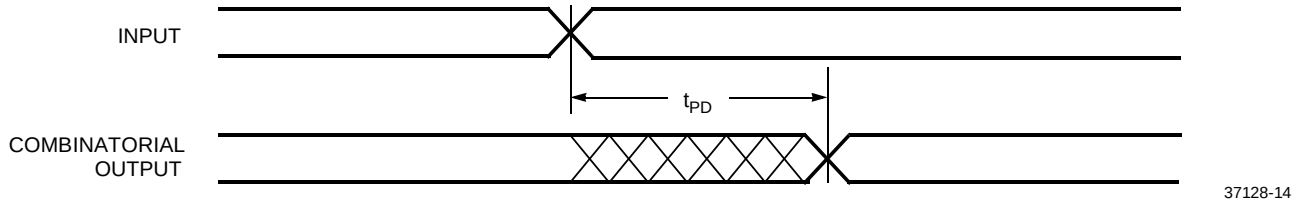
Typical I_{cc} Characteristics



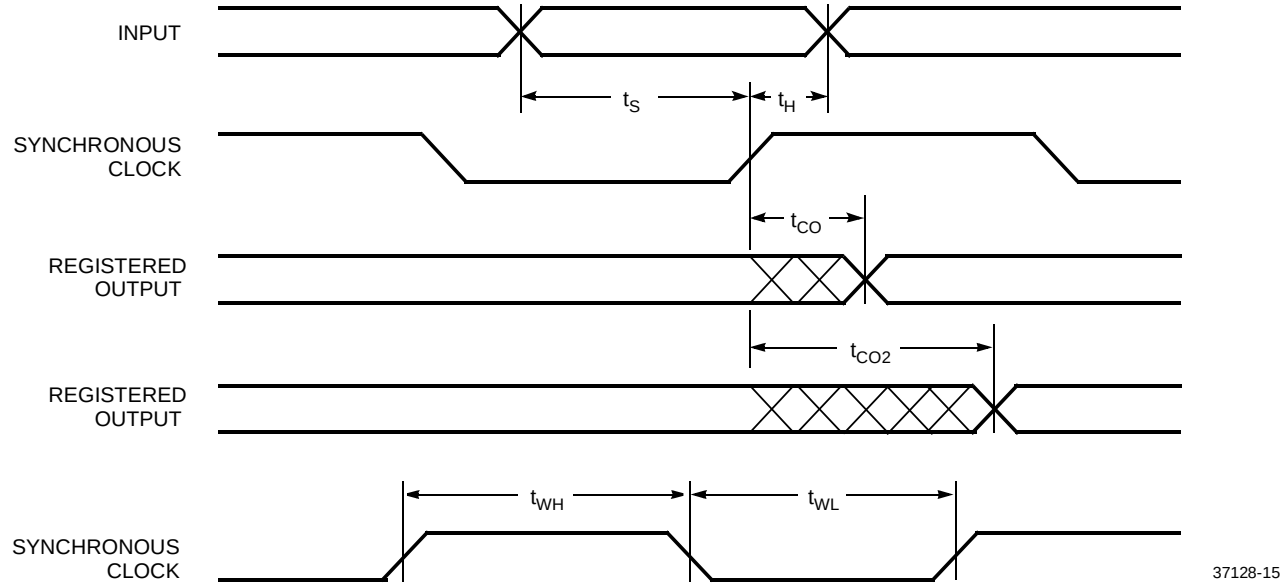
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{cc} = 5.0V, T_A = Room Temperature

Switching Waveforms

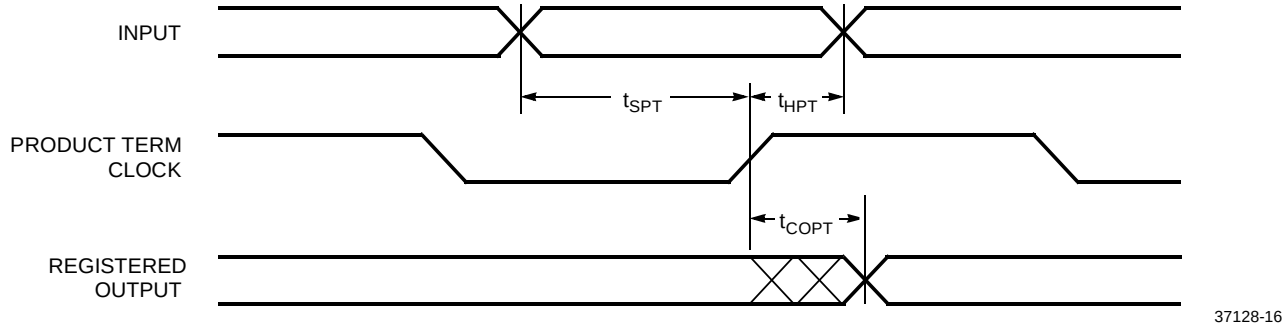
Combinatorial Output



Registered Output with Synchronous Clocking

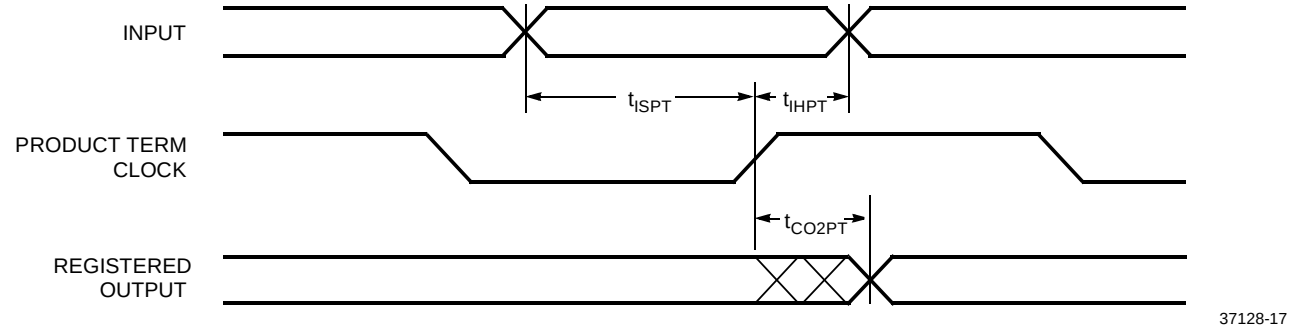


Registered Output with Product Term Clocking Input Going Through the Array



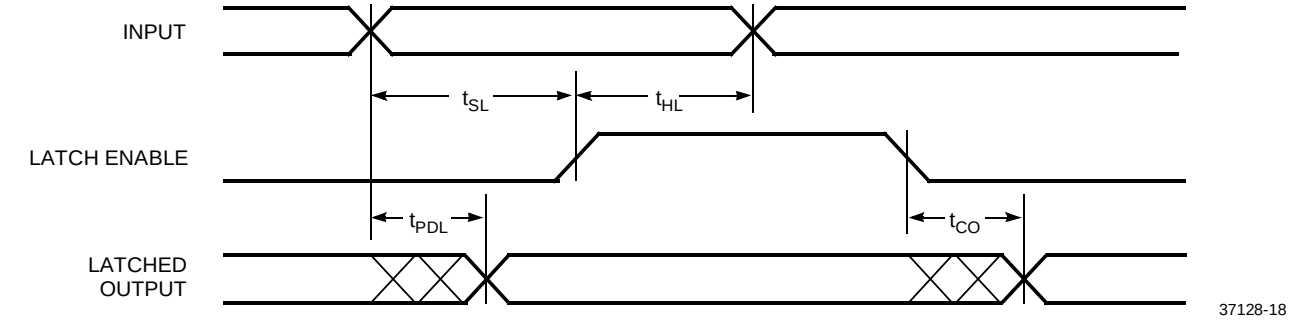
Switching Waveforms (continued)

Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



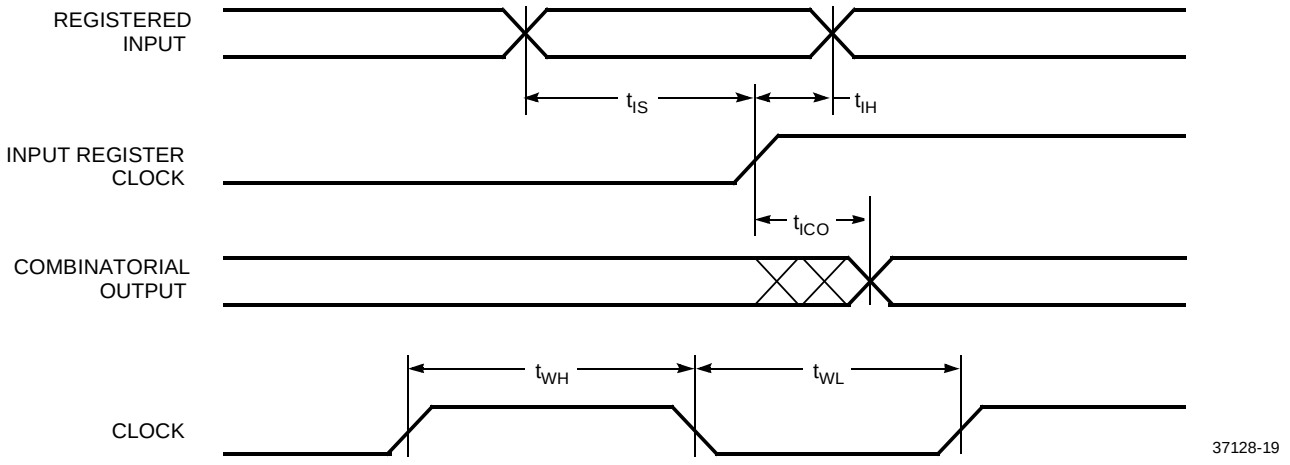
37128-17

Latched Output



37128-18

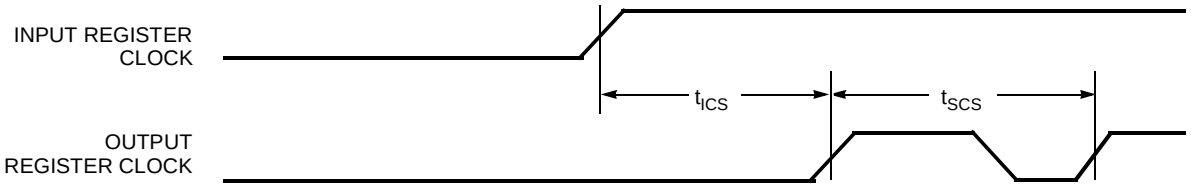
Registered Input



37128-19

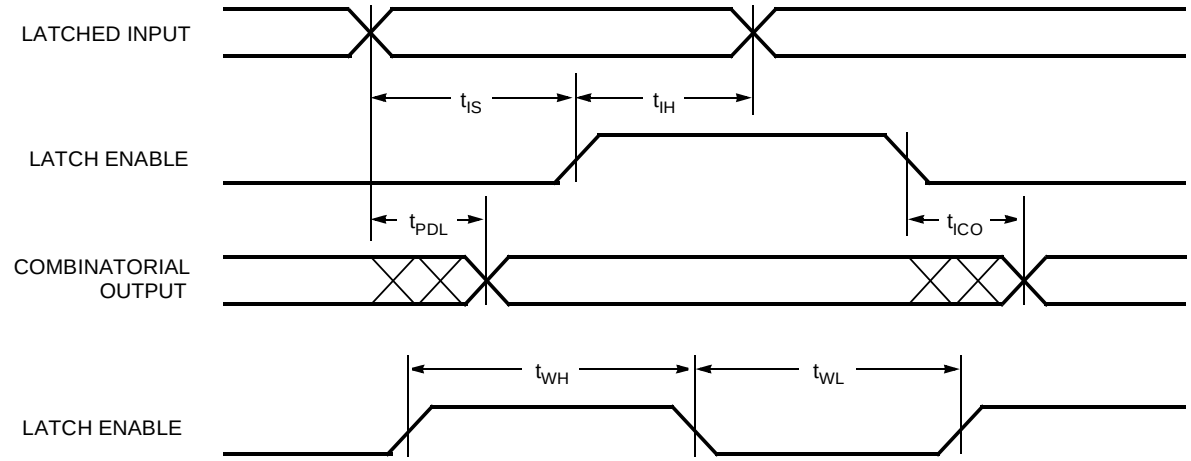
Switching Waveforms (continued)

Clock to Clock



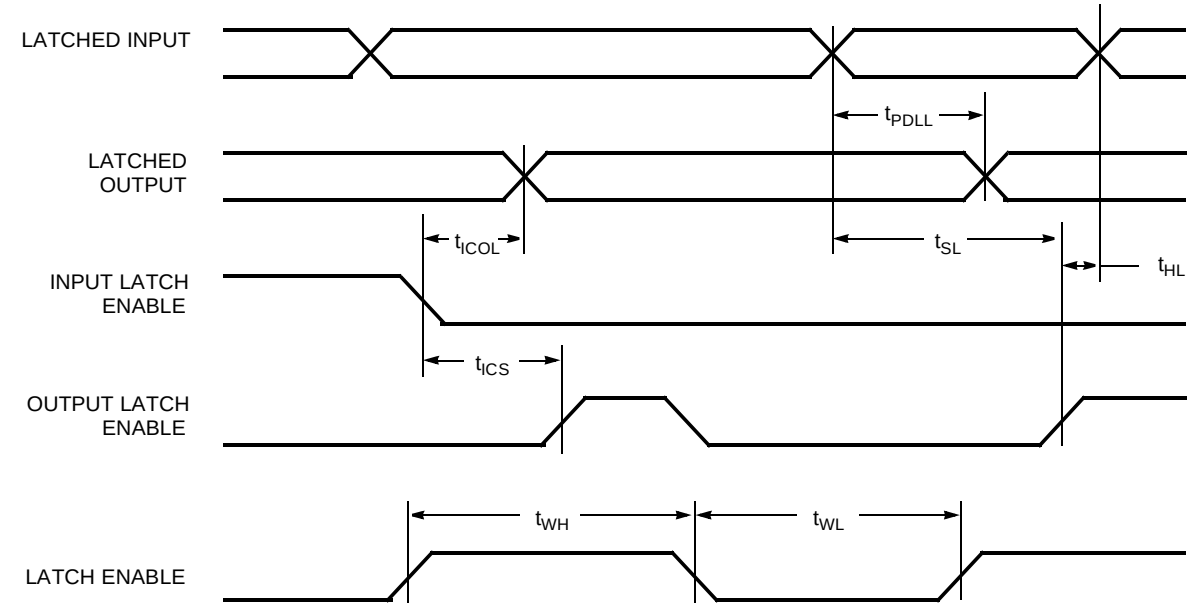
37128-20

Latched Input



37128-21

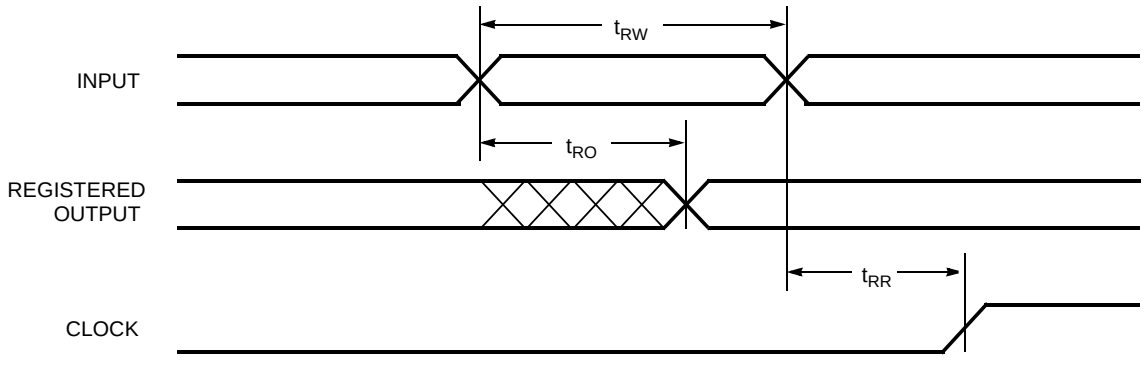
Latched Input and Output



37128-22

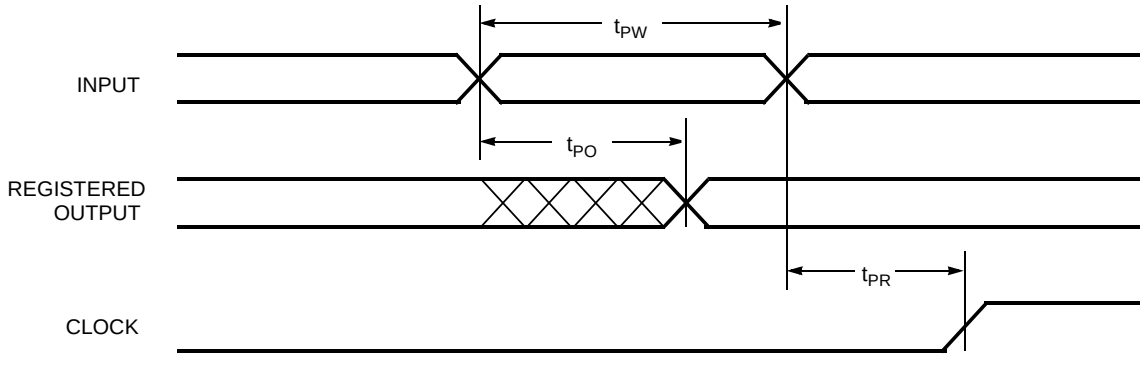
Switching Waveforms (continued)

Asynchronous Reset



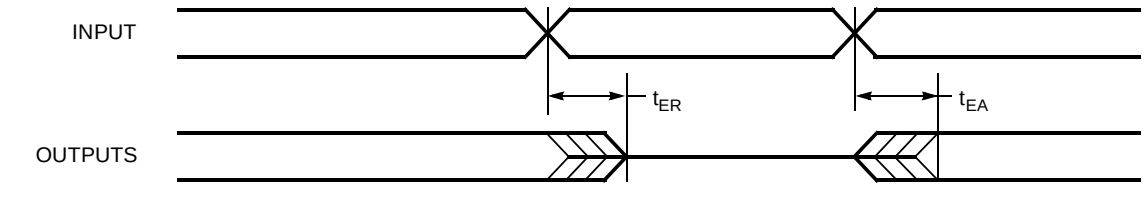
37128-23

Asynchronous Preset



37128-24

Output Enable/Disable



37128–25

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CY37128P84–167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–167AC	A100	100-Lead Thin Quad Flat Pack	
	CY37128P160–167AC	A160	160-Lead Thin Quad Flat Pack	
125	CY37128P84–125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–125AC	A100	100-Lead Thin Quad Flat Pack	
	CY37128P160–125AC	A160	160-Lead Thin Quad Flat Pack	
	CY37128P84–125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
	CY37128P100–125AI	A100	100-Lead Thin Quad Flat Pack	
	CY37128P160–125AI	A160	160-Lead Thin Quad Flat Pack	
	CY37128P84–125YMB	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
100	CY37128P84–100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–100AC	A100	100-Lead Thin Quad Flat Pack	
	CY37128P160–100AC	A160	160-Lead Thin Quad Flat Pack	
	CY37128P84–100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
	CY37128P100–100AI	A100	100-Lead Thin Quad Flat Pack	
	CY37128P160–100AI	A160	160-Lead Thin Quad Flat Pack	
	CY37128P84–100YMB	Y84	84-Lead Ceramic Leaded Chip Carrier	Military

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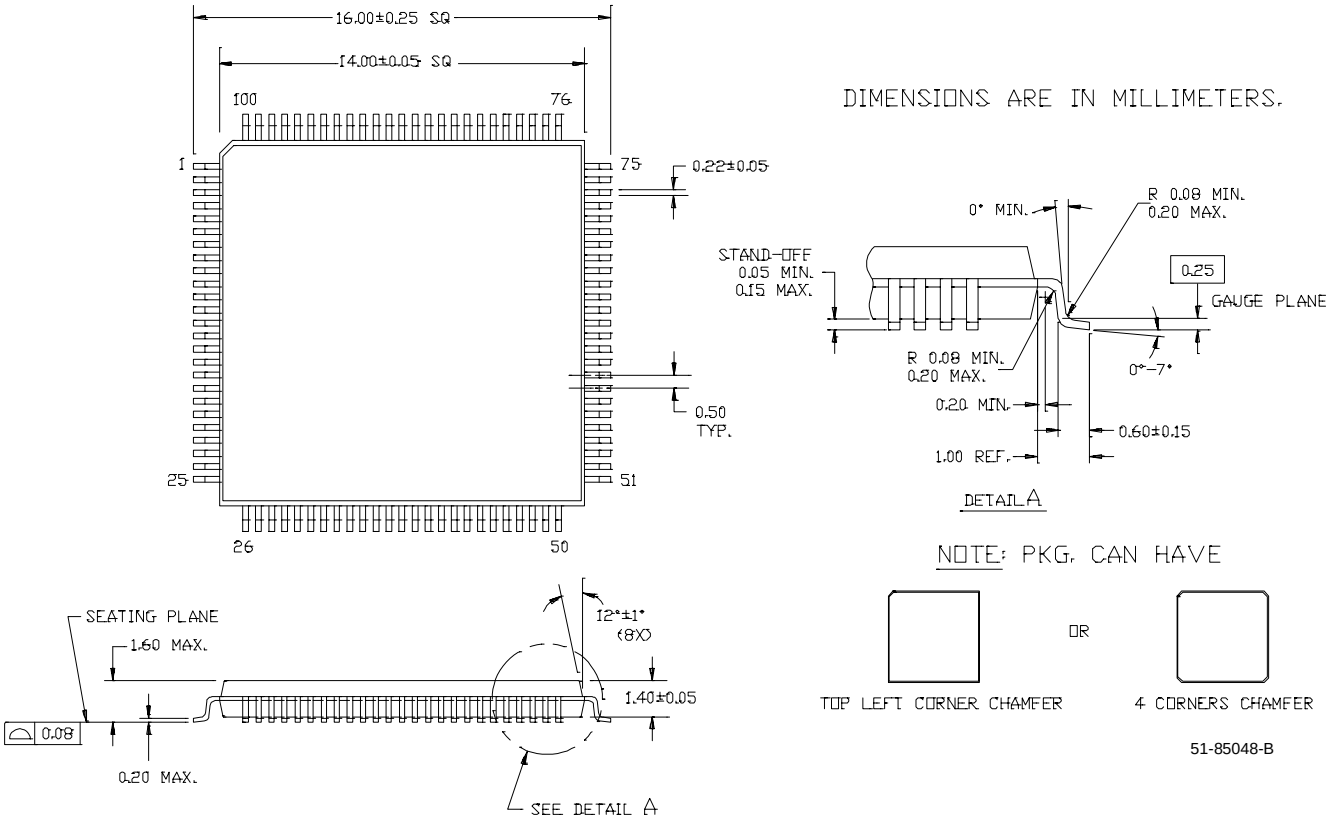
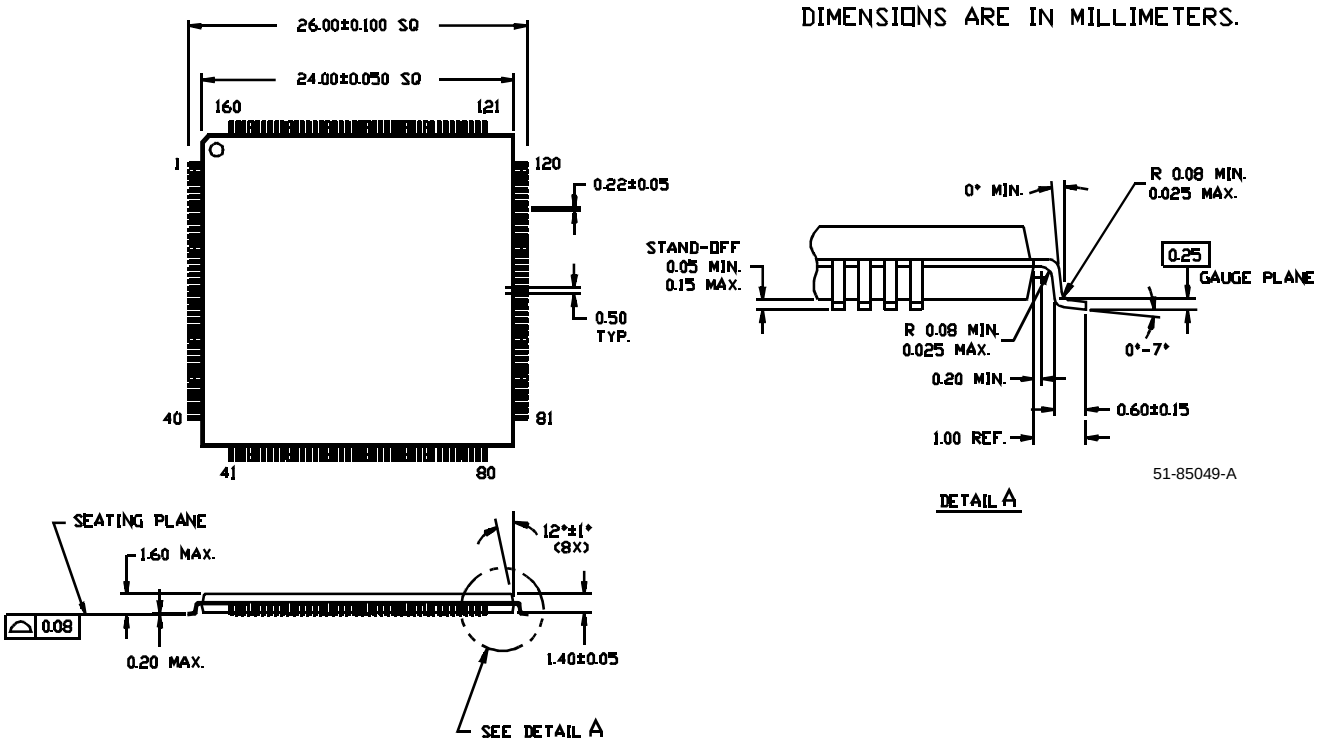
Package Diagrams

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100

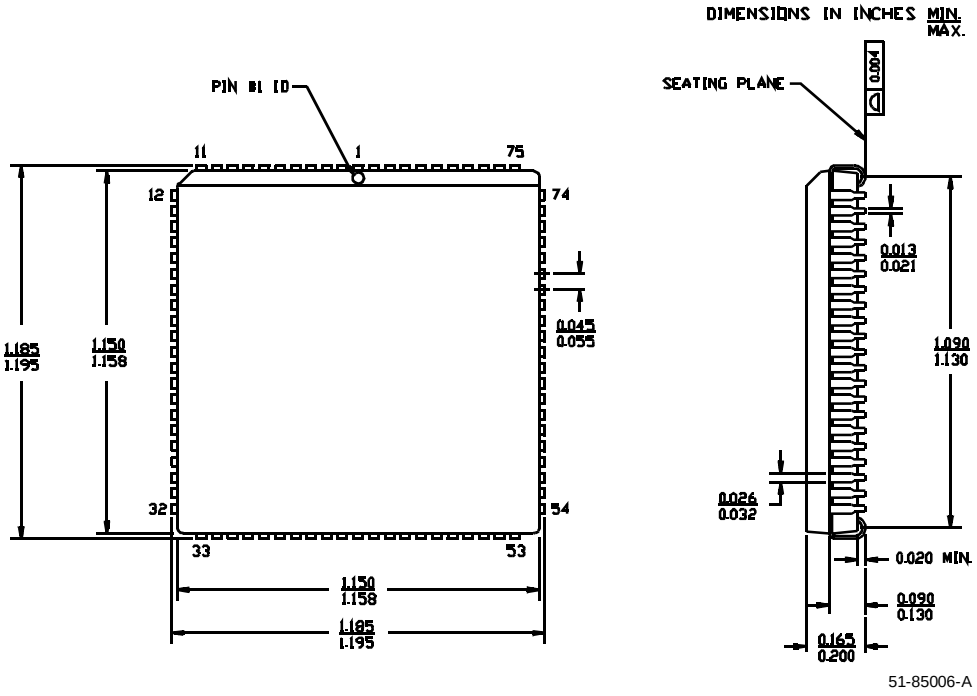


Package Diagrams (continued)

160-Pin Thin Plastic Quad Flat Pack (TQFP) A160

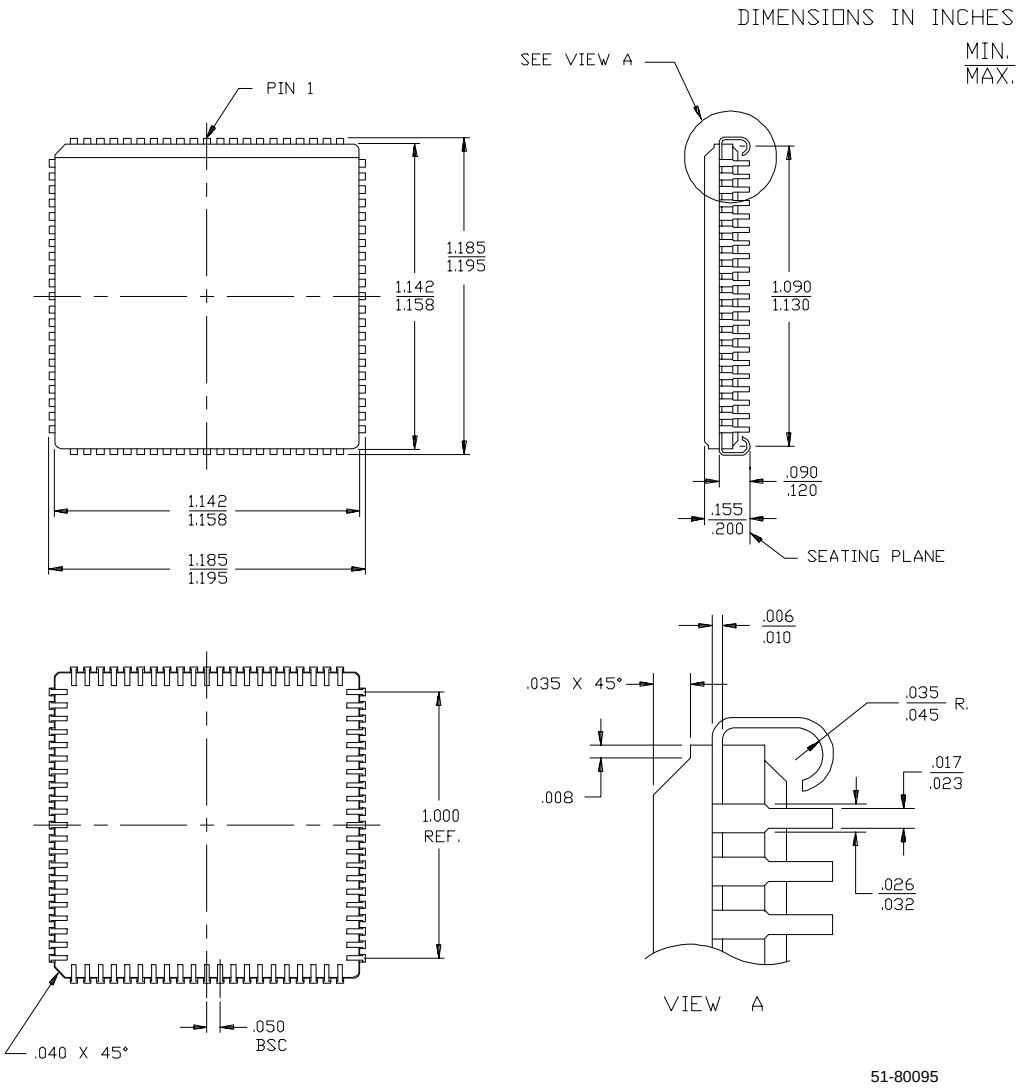


84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



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