VGA Information

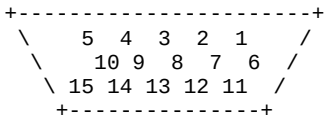


Figure 1: DB-15 Connector Pin Layout

Table 1: VGA pinout. Only pins 1, 2, 3, 13, and 14 are used on the UF-board.

VGA Pin #	Signal Name	UF-4712 Pin #
1	**Red**	**P115**
2	**Green**	**P118**
3	**Blue**	**P119**
4	No Connect (NC)	
5	(Analog) Ground (Self Test)	
6	Ground (Red Return)	
7	Ground (Green Return)	
8	Ground (Blue Return)	
9	No Connect (+5V)	
10	(Digital) Ground (Sync Return)	
11	(Digital) Ground	
12	DDC DAT, SDA, I2C data	
13	**Horizontal Synchronization**	**P121**
14	**Vertical Synchronization**	**P120**
15	DDC Clock, SLC, I2C clock	

DDC= Display Data Channel

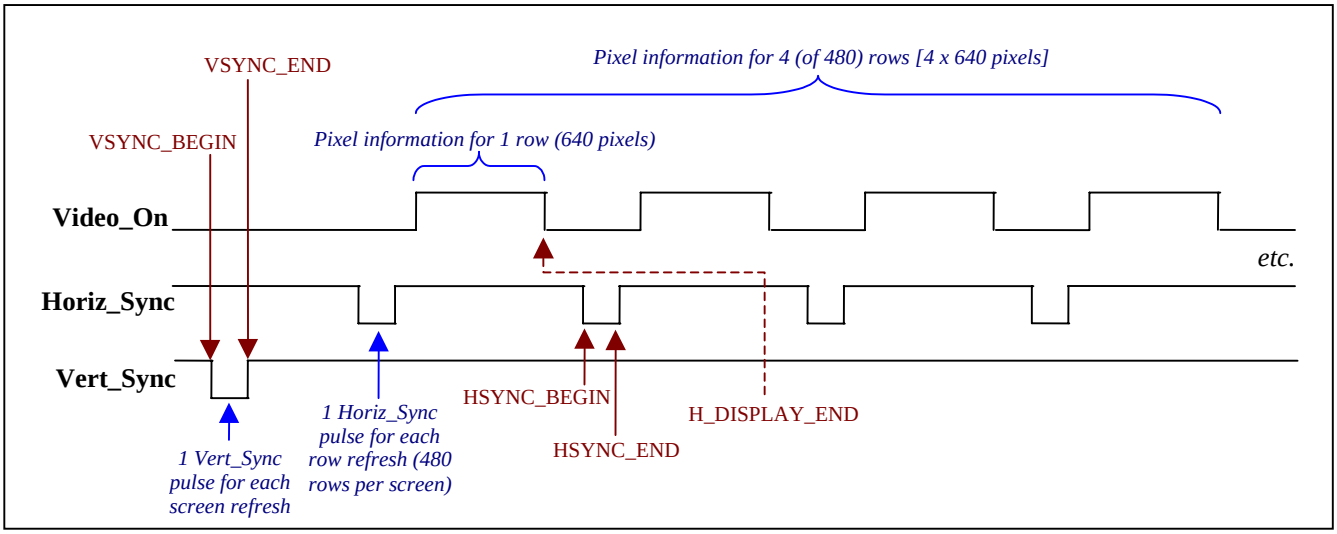
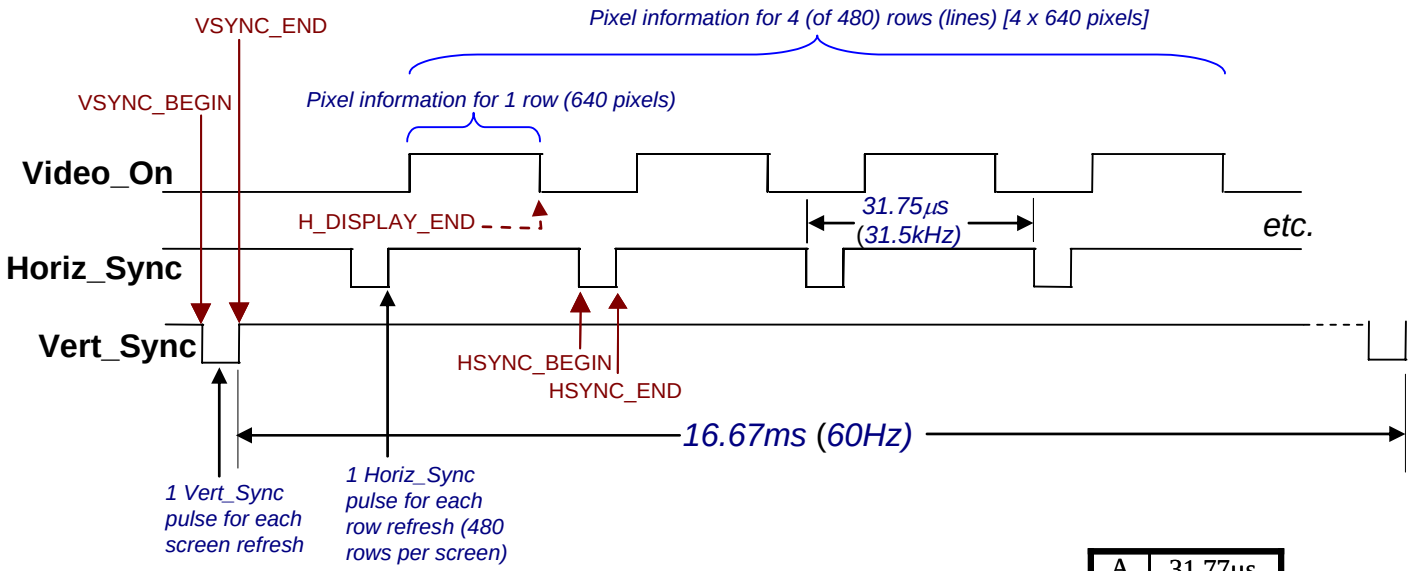


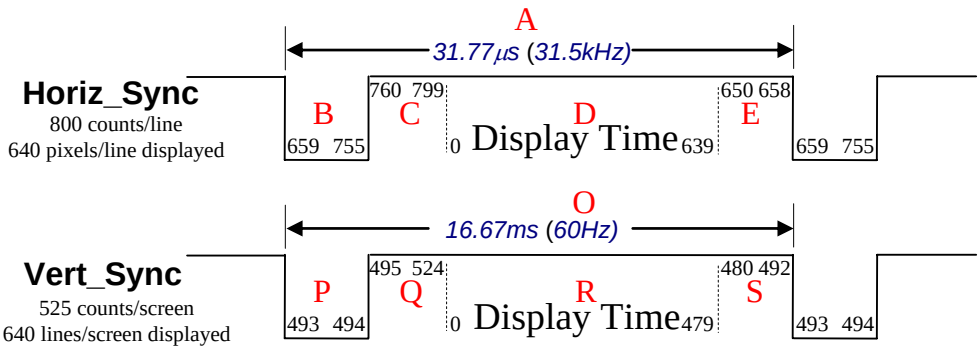
Figure 2: Timing Diagram for four rows of a VGA Display

VGA Information

```
constant H_DISPLAY_END     : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(639,10);
constant HSYNC_BEGIN       : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(659,10);
constant H_VERT_INC        : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(699,10);
constant HSYNC_END         : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(755,10);
constant H_MAX             : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(799,10);
constant V_DISPLAY_END     : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(479,10);
constant VSYNC_BEGIN       : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(493,10);
constant VSYNC_END         : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(494,10);
constant V_MAX             : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(524,10);
constant ZERO              : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(0,10);
constant ONE               : std_logic_vector(9 downto 0) := CONV_STD_LOGIC_VECTOR(1,10);
```

Figure 3: Constants for VGA Signal Generation





A	31.77μs
B	3.77μs
C	1.89μs
D	25.17μs
E	0.94μs
O	16.6ms
P	64μs
Q	1.02ms
R	15.25ms
S	0.35ms

Figure 4: VGA timing.