So You've Decided to Learn The 68HC12

A documentation of the 4744v1.4 Development Kit Board

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Background

The SKPO 4744v1.4 Development Kit board was developed by Scott Kanowitz and Patrick O'Malley at the University of Florida for use in the 4744 lab section. The board integrates the 68HC12B32 with a ROM and CPLD. All control signals are brought out to headers for wire wrapping or debugging.

Jumpers and Headers

This section has a detailed description of the useful jumpers and headers on the board as well as their functions.

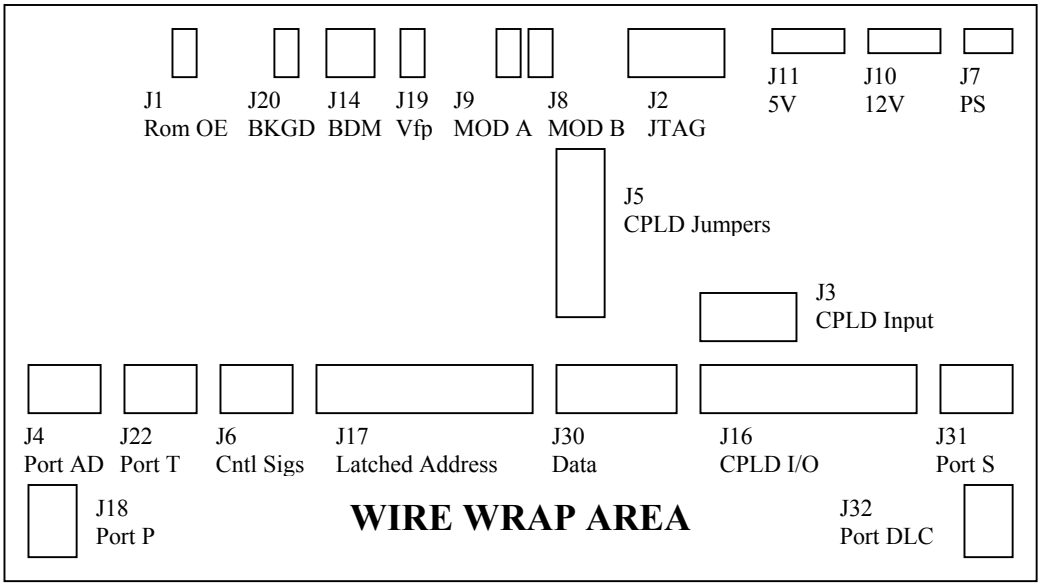


Fig 1. Header labels and board architecture

J1 (ROM OE) – J1 connects the ROM's output enable signal (OE) to the CPLD via pin 26 on the CPLD. If this jumper is removed, the ROM's OE signal is left floating.

J20 (BKGD) – J20 Connects the BKGD pin to ground putting the board into special modes for BDM control. After reset this jumper must be removed to use the BDM header.

J14 (BDM) – J14 is the Background Debug Mode (BDM) header from the 68HC12. It is the standard BDM header as defined by Motorola.

J19 (Vfp) – J19 connects the Vfp pin on the 68HC12 to the 12V header to supply the flash programming voltage. This jumper can only be used if a 12V supply is available.

J9 (MOD A) – J9 is the Mode A input to the 68HC12. This jumper has no function since board errors have forced this header to be tied to +5V putting the HC12 in expanded narrow mode.

J8 (MOD B) – J8 is the Mode B input to the 68HC12. This jumper should not be used since it was wired incorrectly making it useless. If left alone the board will be in expanded narrow mode.

J2 (JTAG) – J2 is the JTAG header for the CPLD. This is the standard JTAG programming header.

J11 (5V) – J11 is the input for a regulated 5V power source. To use this as a power input, jumper J7 (PS) must be removed.

J10 (12V) – J10 is the input for an unregulated 7-12V input. To use this as a power input, jumper J7 (PS) must be connected.

J7 (PS) – J7 allows the user to select between which power input will be used. If an unregulated power source is used through J10, J7 must be connected. If a regulated 5V power source is used through J11, J7 must be disconnected.

Power Source	J7
Reg 5V on J11	Unconnceted
Unreg 7-12V on J10	Connected

Fig 2. Jumper J7 selections

J5 (CPLD Jumpers) – J5 contains a variety of control signals to connect to the CPLD. Each signal is labeled on the board next to the pin it controls. When the jumpers are connected the signals are connected to the CPLD pins according to figure 3. All the address signals come from the latched address source, they are not the raw address signals.

Pin Signal	CPLD Pin
DBE	21
A12	20
A13	19
A14	18
A15	17
Reset	16
R/W	14
ECLK	12
XIRQ	11
IRQ	9

Fig 3. Header J5 selections

J3 (CPLD Input) – J3 contains the CPLD input pins 1, 2, 43, and 44.

J18 (Port P) – J18 contains the 6812's port W pins. This port is also referred to as port W in some Motorola documentation.

J4 (Port AD) – J4 contains the 6812's analog-to-digital port, Port AD.

J22 (Port T) – J22 contains the 6812's Port T.

J6 (Cntl Sigs) – J6 contains some commonly used bus control signals. The pinout of this header is shown in figure 4.

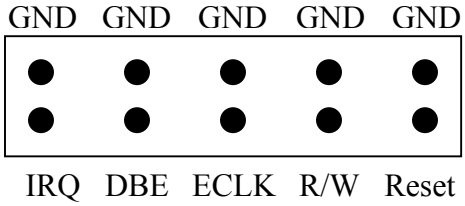


Fig 4. Header J6 pinout

J17 (Latched Address) – J17 contains the 16 bit latched address output from the 74374's.

J30 (Data) – J30 contains the 8 bit data I/O pins from the 68HC12. This header is not buffered and is connected directly to the 68HC12, therefore it also contains the raw upper 8 bit address.

J16 (CPLD I/O) – J16 contains all the CPLD I/O lines for general purpose use.

J31 (Port S) – J31 contains the 68HC12's Port S.

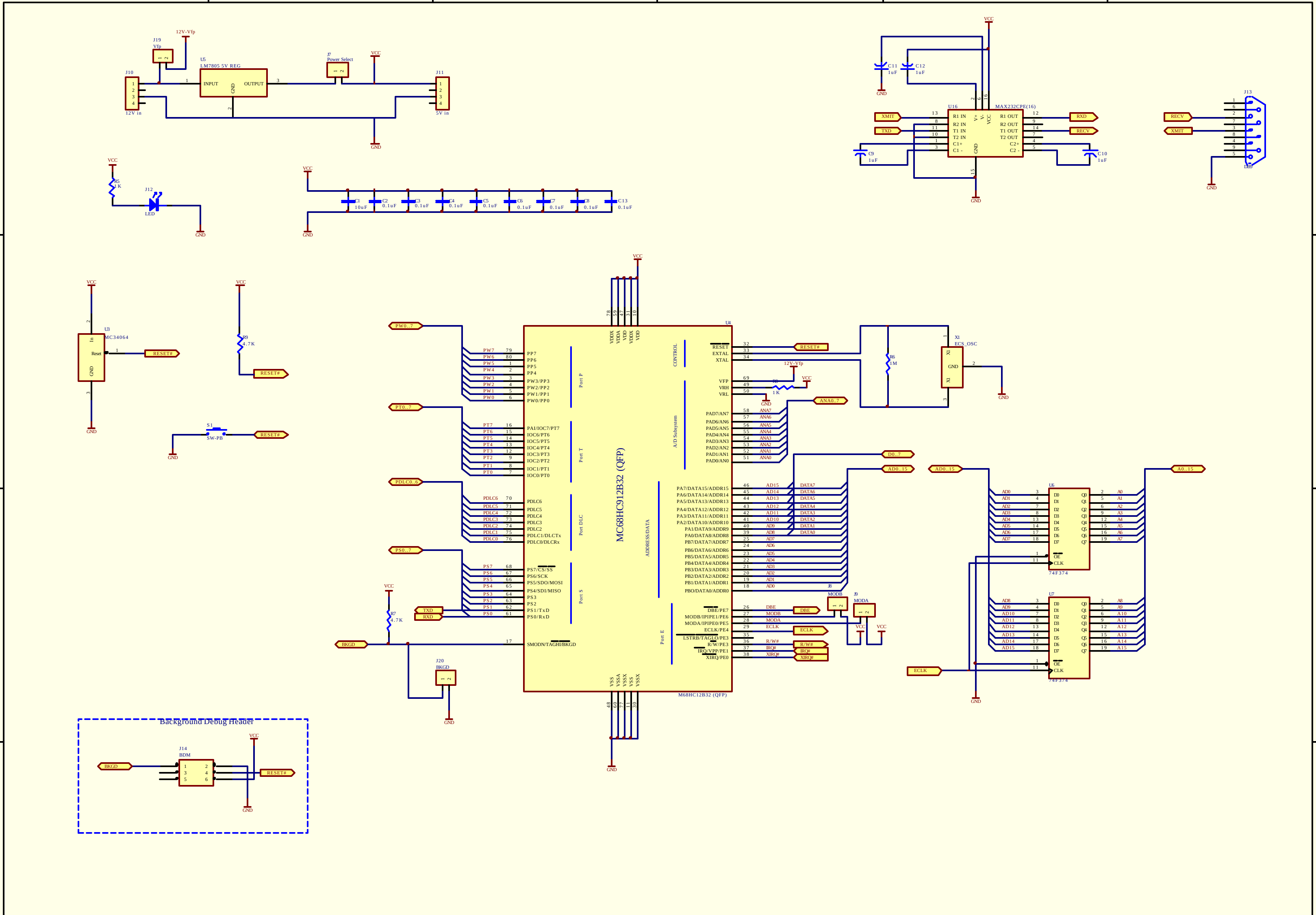
J32 (Port DLC) – J32 contains the 68HC12's Port DLC.

General Hints and Tips

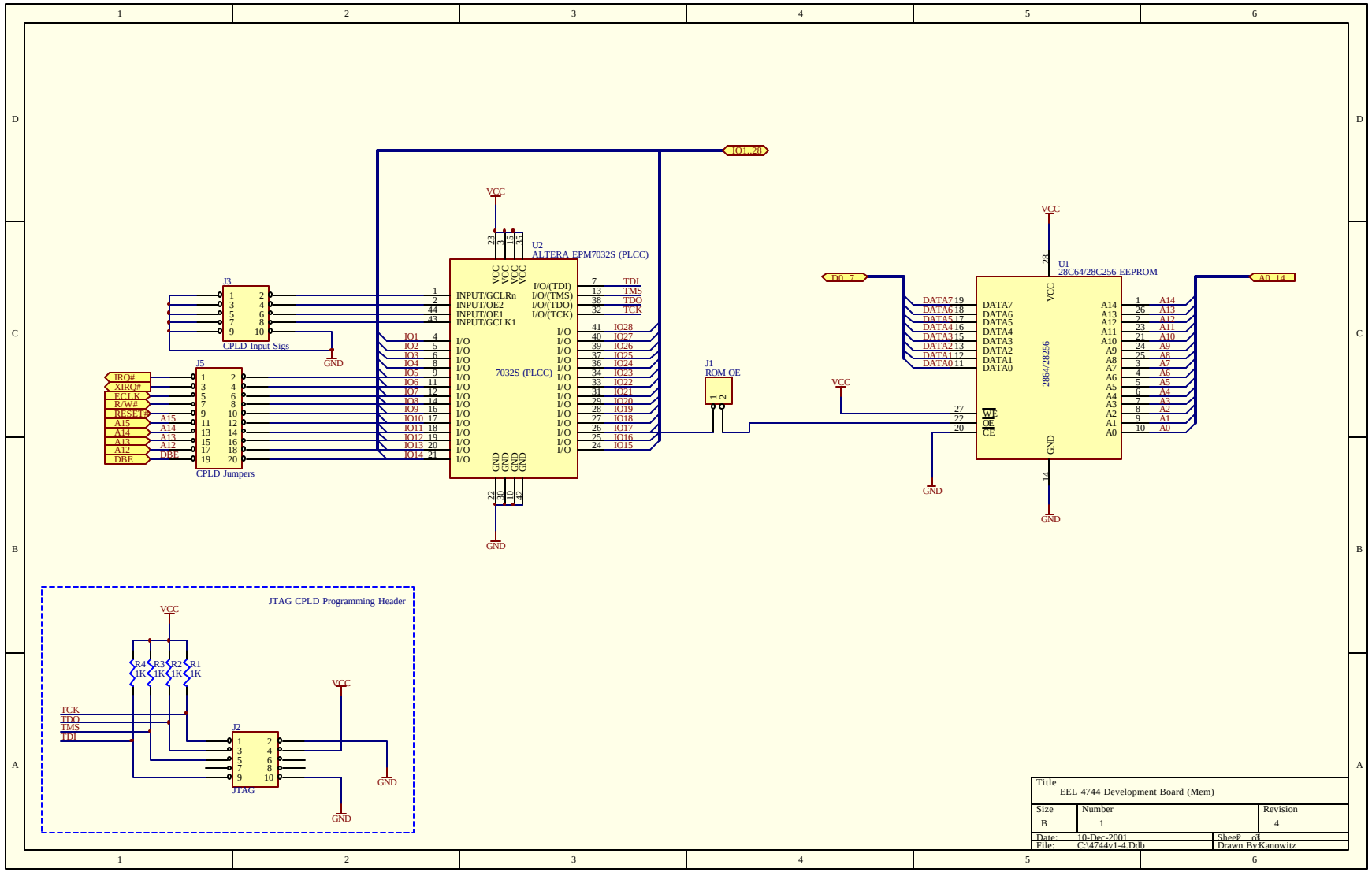
- When the 68HC12 is reset into any normal mode the COP watchdog timer is automatically enabled. To disable it write $00 to the COPCTL register at address $0016.
- When the 68HC12 is reset into any normal mode the R/W disabled externally and the pin is pulled high. To enable the R/W signal write $04 to the PEAR register at address $000A

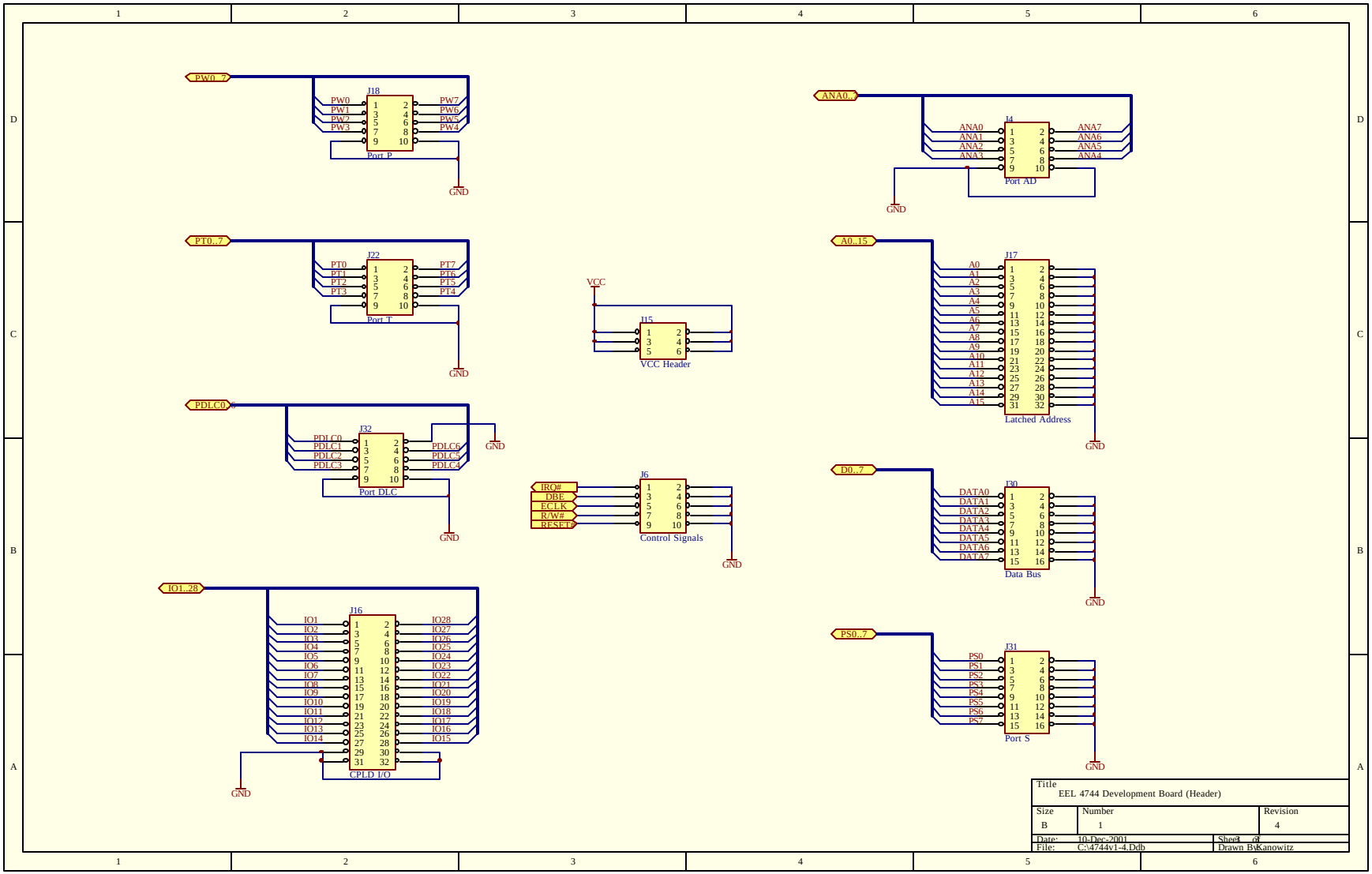
Appendix

Attached to this document are schematic sheets 1, 2, and 3, and the bill of material for the PCB. Sheet 1 contains the core of the board including the 6812, latches, and MAX 232 RS-232 driver. Sheet 2 contains the ROM and CPLD connections. Sheet 3 contains all the wire wrap area headers and their pinouts.



Title		
EEL 4744 Development Board (Core)		
Size: C	Number: 1	Revision: 4
Date: 10-Dec-2001	Sheet 1 of 3	
File: C:\4744v1-4.Ddb	Drawn By: Kanowitz	


IO1..28
VCC
U2
ALTERA EPM7032S (PLCC)
INPUT/GCLRn
INPUT/OE2
INPUT/OE1
INPUT/GCLK1
I/O/(TDI)
I/O/(TMS)
I/O/(TDO)
I/O/(TCK)
7032S (PLCC)
TDI
TMS
TDO
TCK
J3
CPLD Input Sigs
GND
J5
CPLD Jumpers
IRQ#
XIRQ#
E CLK
R/W#
RESET#
A15
A14
A13
A12
DBE
J1
ROM OE
D0..7
A0..14
U1
28C64/28C256 EEPROM
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
WE
OE
CE
JTAG CPLD Programming Header
R4 1K
R3 1K
R2 1K
R1 1K
J2
JTAG
Title
EEL 4744 Development Board (Mem)
Size
B
Number
1
Revision
4
Date: 10-Dec-2001
File: C:\4744v1-4.Ddb
Drawn By:Kanowitz


PW0..7
J18
PW0
PW1
PW2
PW3
PW7
PW6
PW5
PW4
Port P
GND
PT0..7
J22
PT0
PT1
PT2
PT3
PT7
PT6
PT5
PT4
Port T
GND
PDLC0..6
J32
PDLC0
PDLC1
PDLC2
PDLC3
PDLC6
PDLC5
PDLC4
Port DLC
GND
IO1..28
J16
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO28
IO27
IO26
IO25
IO24
IO23
IO22
IO21
IO20
IO19
IO18
IO17
IO16
IO15
CPLD I/O
GND
VCC
J15
VCC Header
IRQ#
DBE
ECLK
R/W#
RESET#
J6
Control Signals
GND
ANA0..7
J4
ANA0
ANA1
ANA2
ANA3
ANA7
ANA6
ANA5
ANA4
Port AD
GND
A0..15
J17
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
Latched Address
GND
D0..7
J30
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
Data Bus
GND
PS0..7
J31
PS0
PS1
PS2
PS3
PS4
PS5
PS6
PS7
Port S
GND
Title
EEL 4744 Development Board (Header)
Size
B
Number
1
Revision
4
Date: 10-Dec-2001
File: C:\4744v1-4.Ddb
Drawn By: Kanowitz

Comment	Designators
0.1uF	C8
0.1uF	C7
0.1uF	C6
0.1uF	C5
0.1uF	C4
0.1uF	C3
0.1uF	C2
0.1uF	C13
10uF	C1
12V in	J10
1K	R8
1K	R5
1K	R4
1K	R3
1K	R2
1K	R1
1M	R6
1uF	C12
1uF	C11
1uF	C10
1uF	C9
28C64/28C256 EEPROM	U1
4.7K	R9
4.7K	R7
5V in	J11
74F374	U7
74F374	U6
ALTERA EPM7032S (PLCC)	U2
BDM	J14
BKGD	J20
Control Signals	J6
CPLD I/O	J16
CPLD Input Sigs	J3
CPLD Jumpers	J5
Data Bus	J30
DB9	J13
ECS_OSC	X1
JTAG	J2
Latched Address	J17
LED	J12
LM7805 5V REG	U5
M68HC12B32 (QFP)	U4
MAX232CPE(16)	U16
MC34064	U3
MODA	J9
MODB	J8
Port AD	J4
Port DLC	J32
Port P	J18

Port S	J31
Port T	J22
Power Select	J7
ROM OE	J1
SW-PB	S1
VCC Header	J15
Vfp	J19