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Analog Discovery 2™ Reference Manual

Revised September 14, 2015
This manual applies to the Analog Discovery 2 rev. C

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Overview

The Digilent Analog Discovery 2™, developed in conjunction with Analog Devices®, is a multi-function instrument that allows users to measure, visualize, generate, record, and control mixed signal circuits of all kinds. The low-cost Analog Discovery 2 is small enough to fit in your pocket, but powerful enough to replace a stack of lab equipment, providing engineering students, hobbyists, and electronics enthusiasts the freedom to work with analog and digital circuits in virtually any environment, in or out of the lab. The analog and digital inputs and outputs can be connected to a circuit using simple wire probes; alternatively, the Analog Discovery BNC Adapter and BNC probes can be used to connect and utilize the inputs and outputs. Driven by the free WaveForms software, the Analog Discovery 2 can be configured to work as any one of several traditional instruments, which include:

The Analog Discovery 2.

- Two-channel oscilloscope (1MΩ, ±25V, differential, 14-bit, 100Msample/sec, 30MHz+ bandwidth - with the Analog Discovery BNC Adapter Board)
- Two-channel arbitrary function generator (±5V, 14-bit, 100Msample/sec, 20MHz+ bandwidth - with the Analog Discovery BNC Adapter Board)
- Stereo audio amplifier to drive external headphones or speakers with replicated AWG signals
- 16-channel pattern generator (3.3V CMOS, 100Msample/sec)[i] [ii]
- 16-channel virtual digital I/O including buttons, switches, and LEDs – perfect for logic training applications[iii] [iv]
- 16-channel digital logic analyzer (3.3V CMOS, 100Msample/sec)[v] [vi]
- Two input/output digital trigger signals for linking multiple instruments (3.3V CMOS)[vii]
- Two programmable power supplies (0…+5V , 0…-5V. The maximum available output current and power depend on the Analog Discovery 2 powering choice:
- 250mW max for each supply or 500mW total when powered through USB
- 700mA max or 2.1W max for each supply when using an external wall power supply
- Single channel voltmeter (AC, DC, ±25V)
- Network analyzer – Bode, Nyquist, Nichols transfer diagrams of a circuit. Range: 1Hz to 10MHz
- Spectrum Analyzer – power spectrum and spectral measurements (noise floor, SFDR, SNR, THD, etc.)
- Digital Bus Analyzers (SPI, I²C, UART, Parallel)

The Analog Discovery 2 was designed for students in typical university-based circuits and electronics classes. Its features and specifications, as well as the additional requirements of operating from USB or external power, maintaining the small and portable form factor, the robustness to withstand student use in a variety of environments, and low-cost are based directly on feedback that was obtained from numerous professors from several universities. Meeting all of these requirements proved challenging; however, the task ultimately generated some new and innovative circuits. This document describes the Analog Discovery 2's circuits, with the intent of providing a better understanding of its electrical functions, operations, and a more detailed description of the hardware's features and limitations. It is not intended to provide enough information to enable complete duplication of the Analog Discovery 2, or to allow users to design custom configurations for programmable parts in the design.

Analog Discovery 2 is the next generation of the very popular Analog Discovery. The main improvements are:

- Ability to use an external power supply and consequently deliver more power to the user supplies. When USB-powered, the Analog Discovery 2 delivers to the user same power as the Analog Discovery.
- New enclosure with enhanced design and improved connector reliability.
- Improved signal/noise and crosstalk performances for both the scope and waveforms generator.
- Better defined bandwidth for both the scope and waveforms generator.

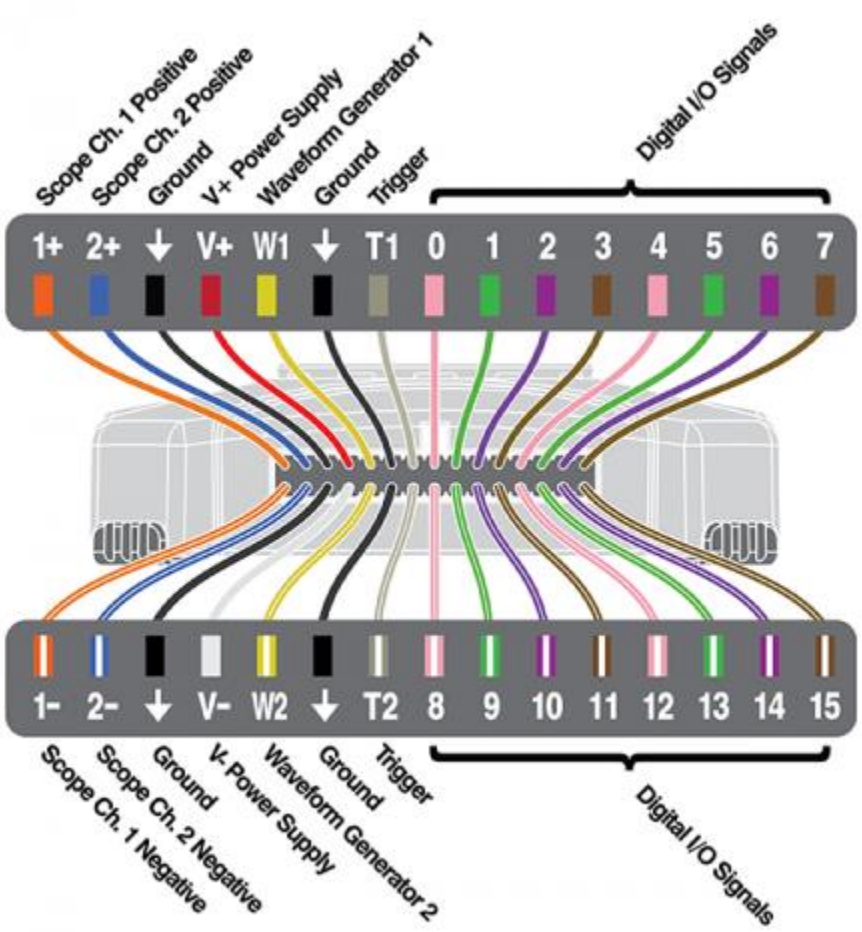

Figure 1. Analog Discovery 2 pinout diagram.

1 Architectural Overview and Block Diagram

Analog Discovery 2's high-level block diagram is presented in Fig. 2 below. The core of the Analog Discovery 2 is the Xilinx® Spartan®-6 FPGA (specifically, the XC6SLX16-1L device). The WaveForms application automatically programs the Discovery's FPGA at start-up with a configuration file designed to implement a multi-function test and measurement instrument. Once programmed, the FPGA inside the Discovery communicates with the PC-based WaveForms application via a USB 2.0 connection. The WaveForms software works with the FPGA to control all the functional blocks of the Analog Discovery 2, including setting parameters, acquiring data, and transferring and storing data.

Signals in the **Analog Input** block, also called the **Scope**, use "SC" indexes to indicate they are related to the scope block. Signals in the **Analog Output** block, also called **AWG**, use "AWG" indexes, and signals in the **Digital** block use a **D** index – all of the instruments offered by the Discovery 2 and WaveForms use the circuits in these three

blocks. Signal and equations also use certain naming conventions. Analog voltages are prefixed with a "V" (for voltage), and suffixes and indexes are used in various ways: to specify the location in the signal path (IN, MUX, BUF, ADC, etc.); to indicate the related instrument (SC, AWG, etc.); to indicate the channel (1 or 2); and to indicate the type of signal (P, N, or diff). Referring to the block diagram in Figure 2 below:

- The **Analog Inputs/Scope** instrument block includes:
  - **Input Divider and Gain Control**: high bandwidth input adapter/divider. High or low-gain can be selected by the FPGA
  - **Buffer**: high impedance buffer
  - **Driver**: provides appropriate signal levels and protection to the ADC. Offset voltage is added for vertical position setting
  - **Scope Reference and Offset**: generates and buffers reference and offset voltages for the scope stages
  - **ADC**: the analog-to-digital converter for both scope channels.
- The **Arbitrary Outputs/AWG** instrument block includes:
  - **DAC**: the digital-to-analog converter for both AWG channels
  - **I/V**: current to bipolar voltage converters
  - **Out**: output stages
  - **Audio**: audio amplifiers for headphone
- A precision **Oscillator** and a **Clock Generator** provide a high quality clock signal for the AD and DA converters.
- The **Digital I/O** block exposes protected access to the FPGA pins assigned for the Digital Pattern Generator and Logic Analyzer.
- The **Power Supplies and Control** block generates all internal supply voltages as well as user supply programmable voltages. The control block also monitors the device power consumption for USB compliance when power is supplied via the USB connection. When external power supply is used, the control block allows more power for the user supplies. Under the FPGA control, power for unused functional blocks can be turned off.
- The **USB Controller** interfaces with the PC for programming the volatile FPGA memory after power on or when a new configuration is requested. After that, it performs the data transfer between the PC and FPGA.
- The **Calibration Memory** stores all calibration parameters. Except for the "Probe Calibration" trimmers in the scope Input divider, the Analog Discovery 2 includes no analog calibration circuitry. Instead, a calibration operation is performed at manufacturing (or by the user), and parameters are stored in memory. The WaveForms software uses these parameters to correct the acquired data and the generated signals

In the sections that follow, schematics are not shown separately for identical blocks. For example, the Scope Input Divider and Gain Selection schematic is only shown for channel 1 since the schematic for channel 2 is identical. Indexes are omitted where not relevant. As examples, in equation **(4)** below, V_(in diff) does not contain the instrument index (which by context is understood to be the Scope), nor the channel index (because the equation applies to both channels 1 and 2). In equation **(3)**, the type index is also missing because V*mux* and V*in* refer to any of *P*(positive), *N* (negative) or *diff* (differential) values.

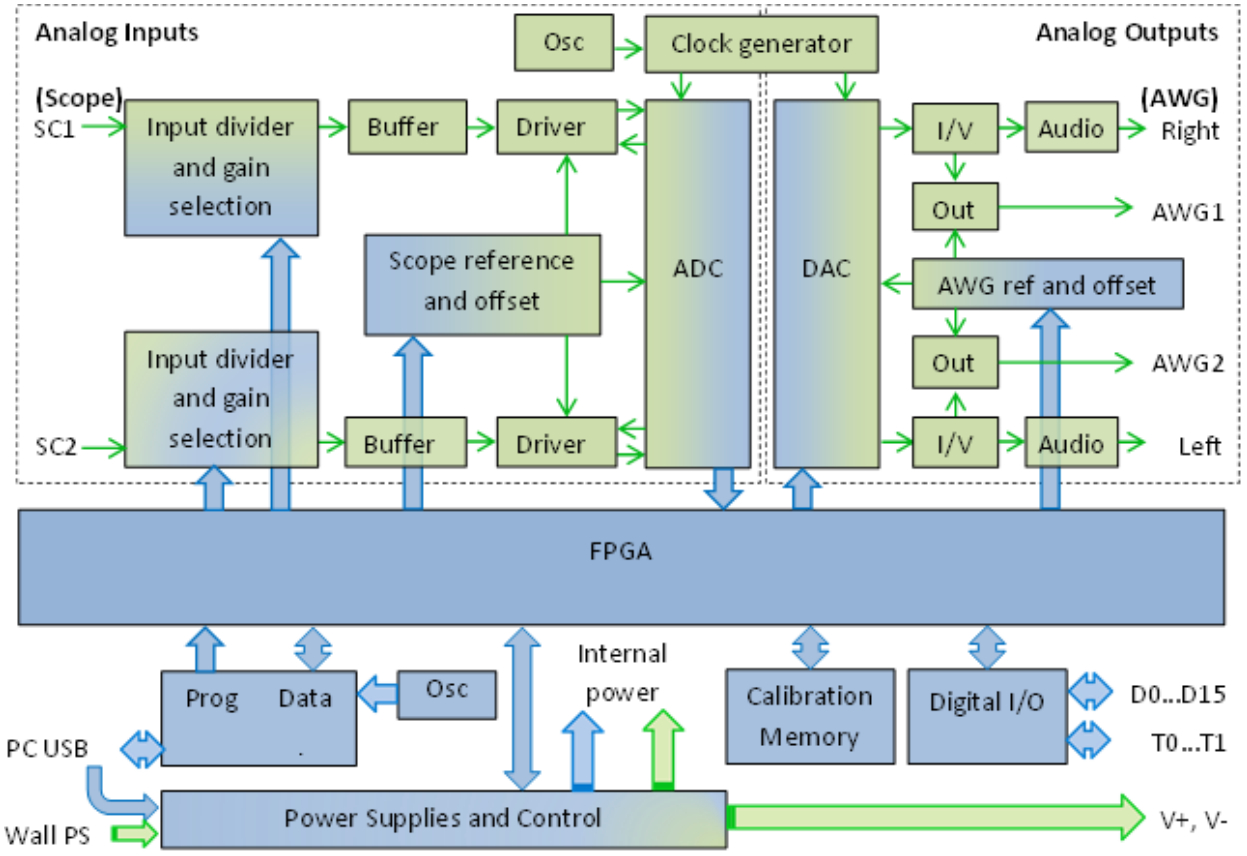

Figure 2. Analog Discovery 2 block diagram.

2 Scope

Important Note: *Unlike traditional inexpensive scopes, the Analog Discovery 2 inputs are fully differential. However, a GND connection to the circuit under test is needed to provide a stable common mode voltage. The Analog Discovery 2 GND reference is connected to the USB GND. Depending on the PC powering scheme, and other PC connections (Ethernet, audio, etc. – which might also be grounded) the Analog Discovery 2 GND reference might be connected to the whole GND system and ultimately to the power network protection (earth ground). The circuit under test might also be connected to earth or possibly floating. For safety reasons, it is the user's responsibility to understand the powering and grounding scheme and make sure that there is a common GND reference between the Analog Discovery 2 and the circuit under test, and that the common mode and differential voltages do not exceed the limits shown in equation (1). Furthermore, for distortion-free measurements, the common mode and differential voltages need to fit into the linear range shown in Figs. 12 and 13. For those applications which scope GND cannot be the USB ground, a USB isolation solution, such as what is described in ADI's CN-0160 can be used; however, this will limit things to USB full speed (12 Mbps), and will impact the update rate (screen refresh rates, not sample rates) of the Analog Discovery 2.*

2.1 Scope Input Divider and Gain Selection

Error! Reference source not found. shows the scope input divider and gain selection stage.

Two symmetrical R-C dividers provide:

- Scope input impedance = 1MOhm || 24pF
- Two different attenuations for high-gain/low-gain (10:1)
- Controlled capacitance, much higher than the parasitical capacitance of subsequent stages
- Constant attenuation and high CMMR over a large frequency range (trimmer adjusted)
- Protection for overvoltage (with the ESD diodes of the ADG612 inputs)

The maximum voltage rating for scope inputs is limited by C1 thru C24 to:

$$-\mathbf{50}\boldsymbol{V} < \boldsymbol{V_{inP}}, \boldsymbol{V_{inN}} < \mathbf{50}\boldsymbol{V} \qquad \textbf{(1)}$$

The maximum swing of the input signal to avoid signal distortion by opening the ADG612 ESD diodes is (for both low-gain and high-gain):

$$-\mathbf{26}\boldsymbol{V} < \boldsymbol{V_{inP}}, \boldsymbol{V_{inN}} < \mathbf{26}\boldsymbol{V} \qquad \textbf{(2)}$$

An analog switch (ADG612) allows selecting high-gain versus low-gain (EN_HG_SC1, EN_LG_SC1) signals from the FPGA. The P and N branches of the differential path are switched together.

The ADG612 quad switch was used because it provides excellent impedance and bandwidth parameters:

- 1 pC charge injection
- ±2.7 V to ±5.5 V dual-supply operation
- 100 pA maximum at 25°C leakage currents
- 85 Ω on resistance
- Rail-to-rail switching operation
- Typical power consumption: <0.1 µW
- TTL-/CMOS-compatible inputs

- -3 dB Bandwidth 680 MHz
- 5 pF each of CS, CD (ON or OFF)

The Low Gain is:

$$\frac{V_{mux}}{V_{in}} = \frac{R_6}{R_1 + R_4 + R_6} = 0.019 \quad (3)$$

The Low Gain is used for input voltages:

$$|V_{in\,diff}| = |V_{in\,P} - V_{in\,N}| < 50V \quad (4)$$

The High Gain is:

$$\frac{V_{mux}}{V_{in}} = \frac{R_4 + R_6}{R_1 + R_4 + R_6} = 0.212 \quad (5)$$

The High Gain is used for input voltages:

$$|V_{in\,diff}| = |V_{in\,P} - V_{in\,N}| < 7V \quad (6)$$

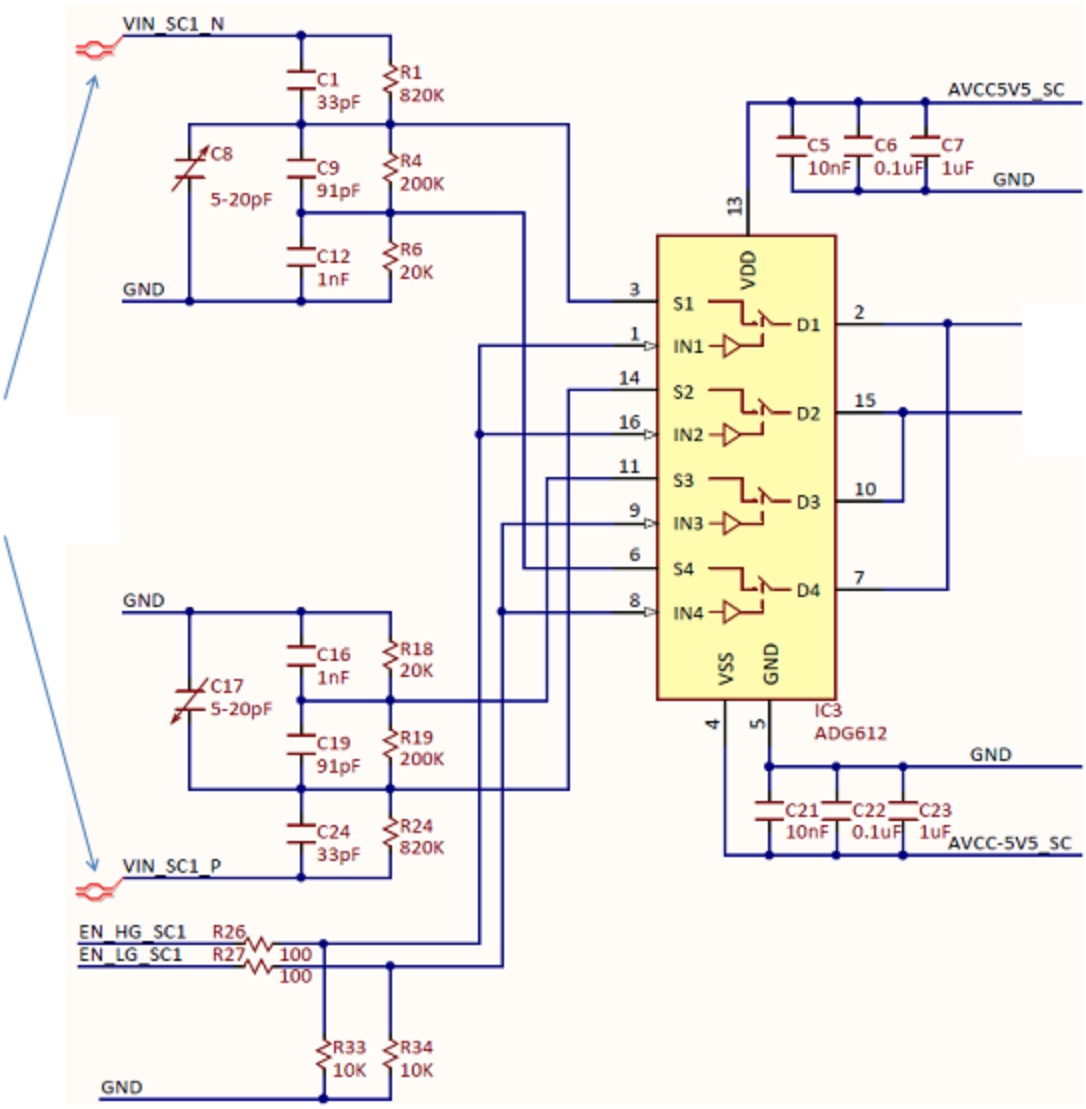

Figure 3. Input divider and gain selection.

2.2 Scope Buffer

A non-inverting OpAmp stage provides very high impedance as load for the input divider (Figure 4.

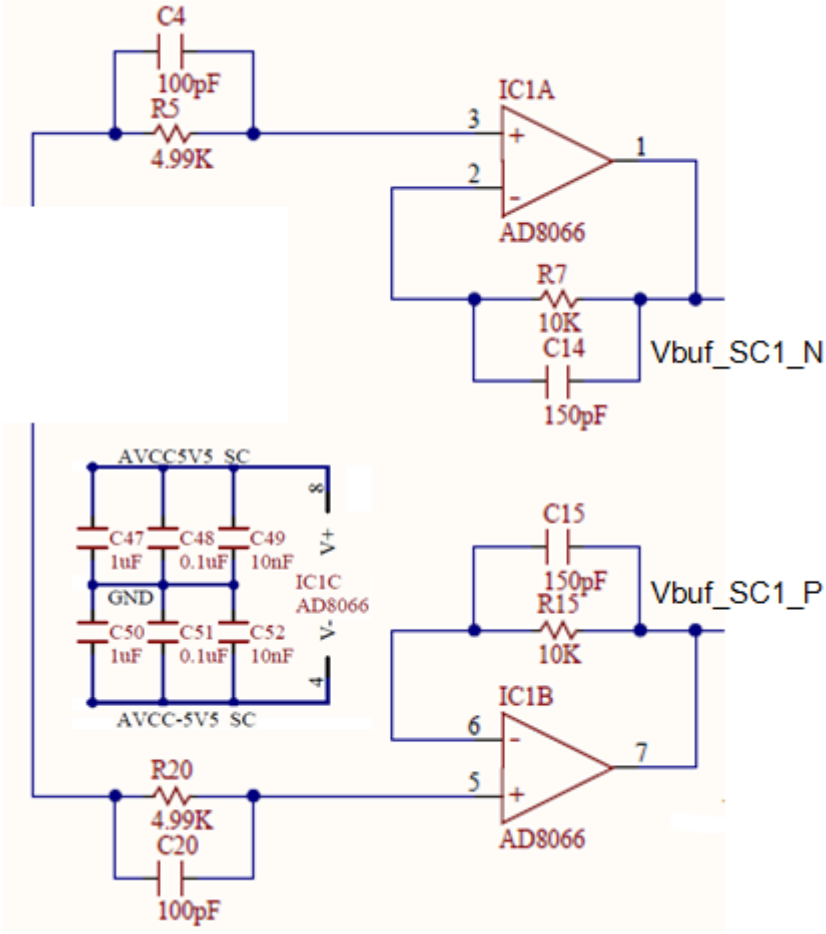

Figure 4. Scope buffer.

The useful features of the AD8066 are:

- FET input amplifier
- 1 pA input bias current
- Low cost
- High speed: 145 MHz, −3 dB bandwidth (G = +1)
- 180 V/µs slew rate (G = +2)
- Low noise 7 nV/√Hz (f = 10 kHz), 0.6 fA/√Hz (f = 10 kHz)
- Wide supply voltage range: 5 V to 24 V
- Rail-to-rail output
- Low offset voltage 1.5 mV maximum
- Excellent distortion specifications
- SFDR −88 dBc @ 1 MHz
- Low power: 6.4 mA/amplifier typical supply current
- Small packaging: MSOP-8

Resistors and capacitors in the figure help to maximize the bandwidth and reduce peaking (which might be significant at unity gain).

The AD8066 is supplied ± 5.5V.

The maximum input voltage swing is: $$-5.5V < V_{mux\,P}, V_{mux\,N} < 2.2V \quad (7)$$

The maximum output voltage swing is: $$-5.38V < V_{buf\,P}, V_{buf\,N} < 5.4V \quad (8)$$

The Gain is: $$\frac{V_{buf}}{V_{mux}} = 1 \quad (9)$$

2.3 Scope Reference and Offset

Figure 5. shows the scope voltage reference sources and offset control stage. A low noise reference is used to generate reference voltages for all the scope stages. Buffered and scaled replicas of the reference voltages are provided for the buffer stages and individually for each scope channel to minimize crosstalk. A dual channel DAC generates the offset voltages, to be added over the input signal, for vertical position. Buffers are used to provide low impedance.

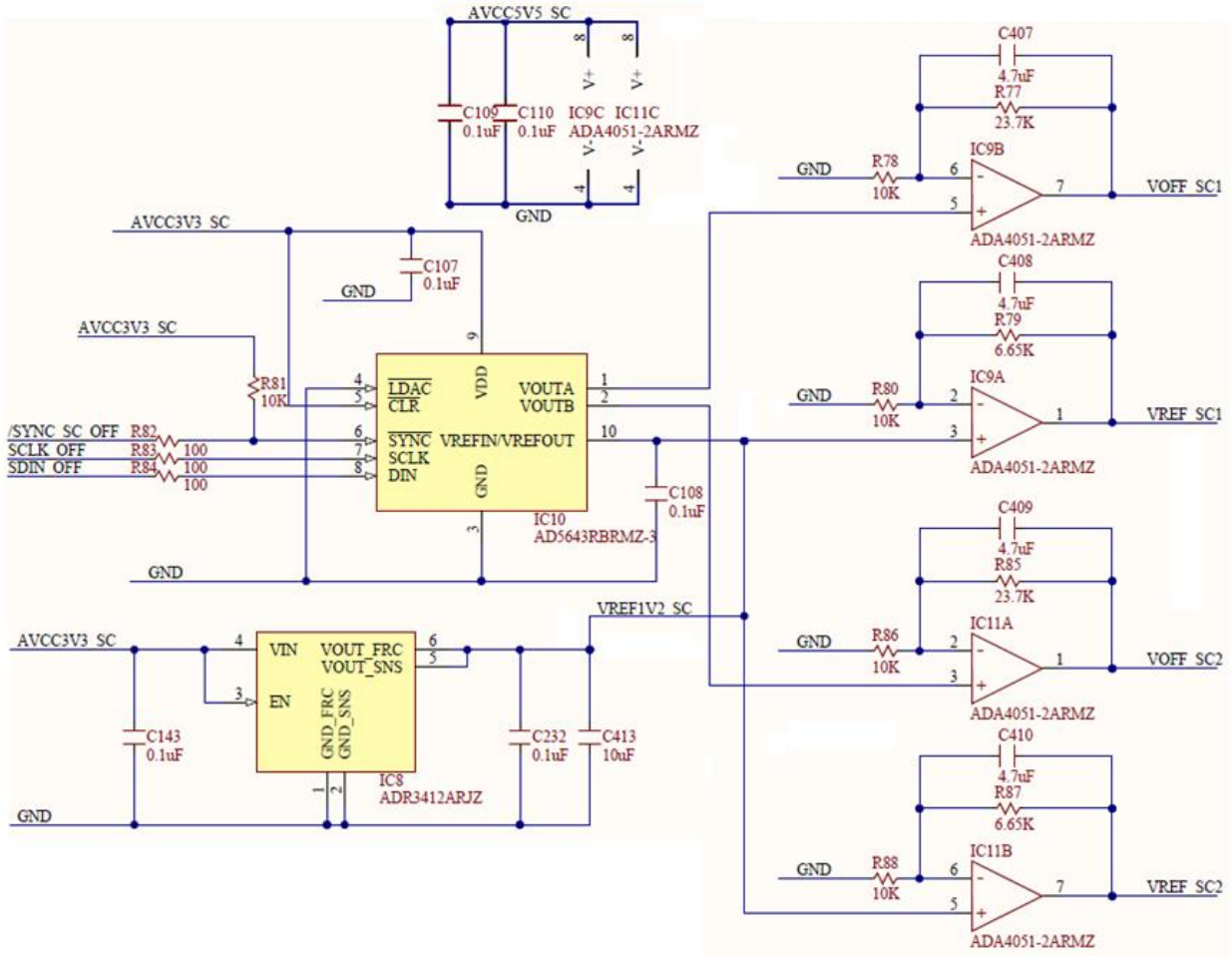

Figure 5. Scope reference and offset.

ADR3412ARJZ – Micropower, high accuracy voltage reference:

- Initial accuracy: ±0.1% (maximum)
- Low temperature coefficient: 8 ppm/°C
- Low quiescent current: 100 µA (maximum)
- Output noise (0.1 Hz to 10 Hz): <10 µV p-p at 1.2 V (typical)

AD5643 - Dual 14-Bit nanoDAC®:

- Low power, smallest dual nanoDAC
- 2.7 V to 5.5 V power supply
- Serial interface up to 50 MHz

ADA4051-2 – Micropower, Zero-drift, Rail-to-rail input/output Op Amp:

- Very low supply current: 13 µA typical
- Low offset voltage: 15 µV maximum
- Offset voltage drift: 20 nV/°C
- High PSRR: 110 dB minimum
- Rail-to-rail input/output
- Unity-gain stable

The reference voltages generated for the scope stages are:

$$\boldsymbol{V_{ref\ SC} = V_{ref\ 1V2} \cdot \left(1 + \frac{R_{79}}{R_{80}}\right) = 2V} \qquad \textbf{(10)}$$

The offset voltages for the scope stages are:

$$\boldsymbol{0 \leq V_{off\ SC} = V_{out\ AD5643} \cdot \left(1 + \frac{R_{77}}{R_{78}}\right) < 4.044V} \qquad \textbf{(11)}$$

2.4 Scope Driver

ADA4940 ADC driver features:

- Small signal bandwidth: 260 MHz
- Extremely low harmonic distortion: -122 dB THD at 50 kHz, -96 dB THD at 1 MHz
- Low input voltage noise: 3.9 nV/√Hz
- 0.35 mV maximum offset voltage
- Settling time to 0.1%: 34 ns
- Rail-to-rail output
- Adjustable output common-mode voltage
- Flexible power supplies: 3 V to 7 V(LFCSP)
- Ultra-low power: 1.25mA

IC2 (**Error! Reference source not found.**6) is used for:

- Driving the differential inputs of the ADC (with low impedance outputs)
- Providing the common mode voltage for the ADC
- Adding the offset (for vertical position on the scope). VREF_SC1 is constant at midrange of VOFF_SC1. This way, the added offset can be either positive or negative.

- ADC protection by clamping the output signals. Protection is important since IC2 is supplied ±3.3V, while the ADC inputs only support -0.1…2.1V. The IC2A constant output signals act as clamping voltages for the Schottky diodes D1, D2.

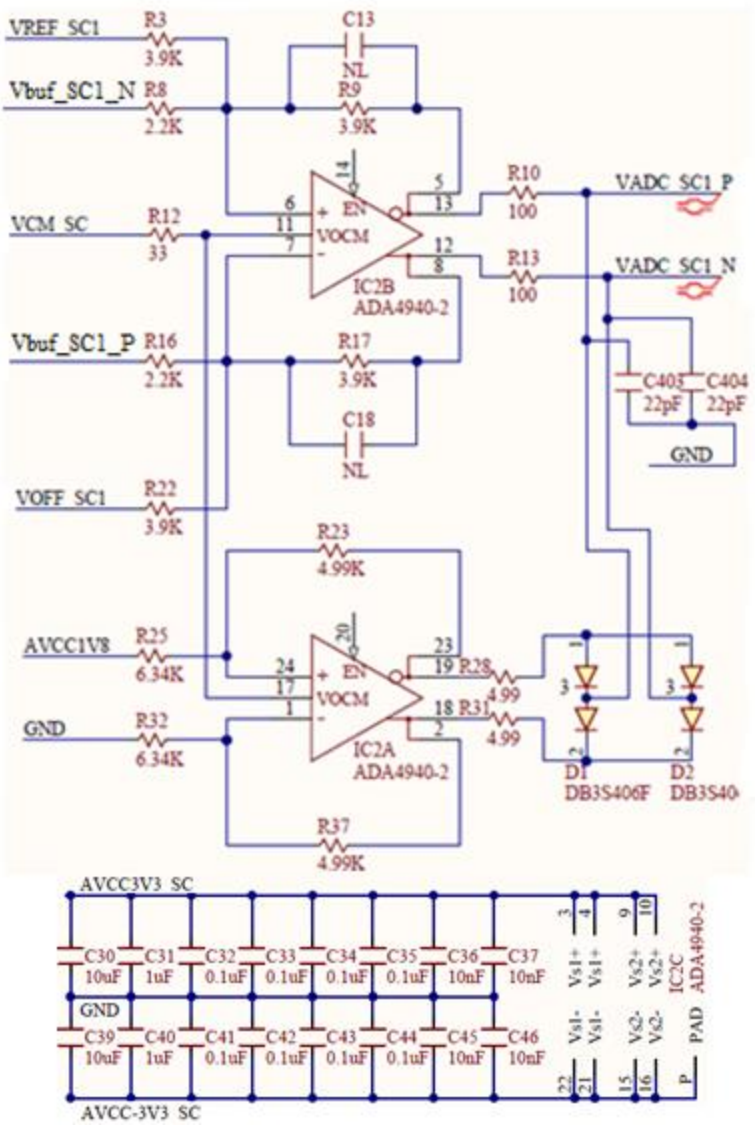

Figure 6. Scope driver.

ADA4940 is supplied ±3.3V. The common mode voltage range is:

$$-3.5V < V_{+\,ADA4940} = V_{-\,ADA4940} < 2.1V \quad (12)$$

The Signal Gain is:

$$\frac{V_{ADC\,diff}}{V_{buf\,diff}} = \frac{R_9}{R_8} = \frac{R_{17}}{R_{16}} = 1.77 \quad (13)$$

The Offset Gain is:

$$\frac{V_{ADC\,diff}}{V_{offSC} - V_{refSC}} = \frac{R_9}{R_3} = \frac{R_{17}}{R_{22}} = 1 \quad (14)$$

The Common Mode Gain is:

$$\frac{V_{CM}}{\frac{V_{ADC\,P} + V_{ADC\,N}}{2}} = 1 \quad (15)$$

The Clamping Voltages are:

$$V_{Out-IC2A} = V_{CM} - \frac{AVCC1V8}{2} \cdot \frac{R_{23}}{R_{25}} = 0.9V - \frac{1.8V}{2} \cdot \frac{4.99K}{6.34K} = 0.2V \quad (16)$$

$$V_{Out+IC2A} = V_{CM} + \frac{AVCC1V8}{2} \cdot \frac{R_{23}}{R_{25}} = 0.9V + \frac{1.8V}{2} \cdot \frac{4.99K}{6.34K} = 1.6V \quad (17)$$

D1, D2 clamp the VADC signals to the protected levels of:

$$-0.1V < V_{+ADA4940} = V_{-ADA4940} < 1.9V \quad (18)$$

2.5 Clock Generator

A precision oscillator (IC31) generates a low jitter, 20 MHz clock (see Figure 8).

The ADF4360-9 Clock Generator PLL with Integrated VCO is configured for generating a 200 MHz differential clock for the ADC and a 100 MHz single-ended clock for the DAC.

Analog Devices ADIsimPLL software was used for designing the clock generator (see Figure 7). The PLL filter is optimized for constant frequency (low Loop Bandwidth = 50 kHz and Phase Margin = 60°). Simulation results are shown below. The Phase jitter using a brick wall filter (10.0 kHz to 100 kHz) is 0.04° rms.

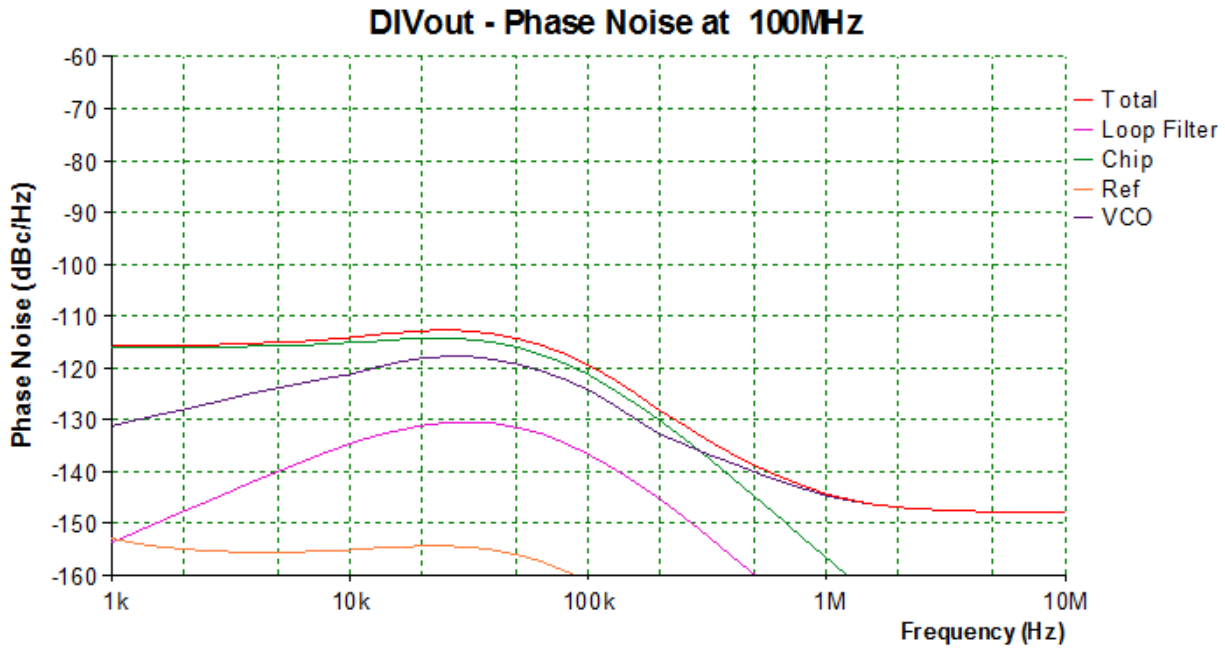

Figure 7. Phase noise figure for the clock generator.

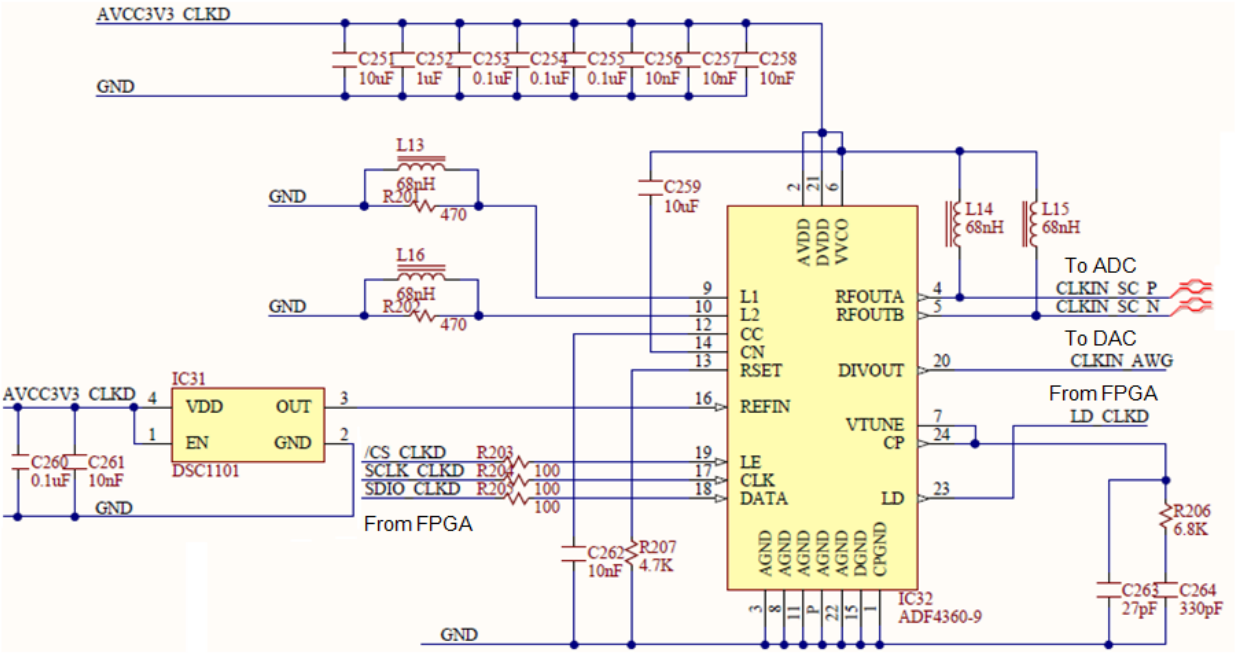

Figure 8. Clock generator.

2.6 Scope ADC

2.6.1 Analog Section

The Analog Discovery 2 uses a dual channel, high speed, low power, 14 bit, 105MSPS ADC (Analog part number AD9648), as shown in Figure 9.

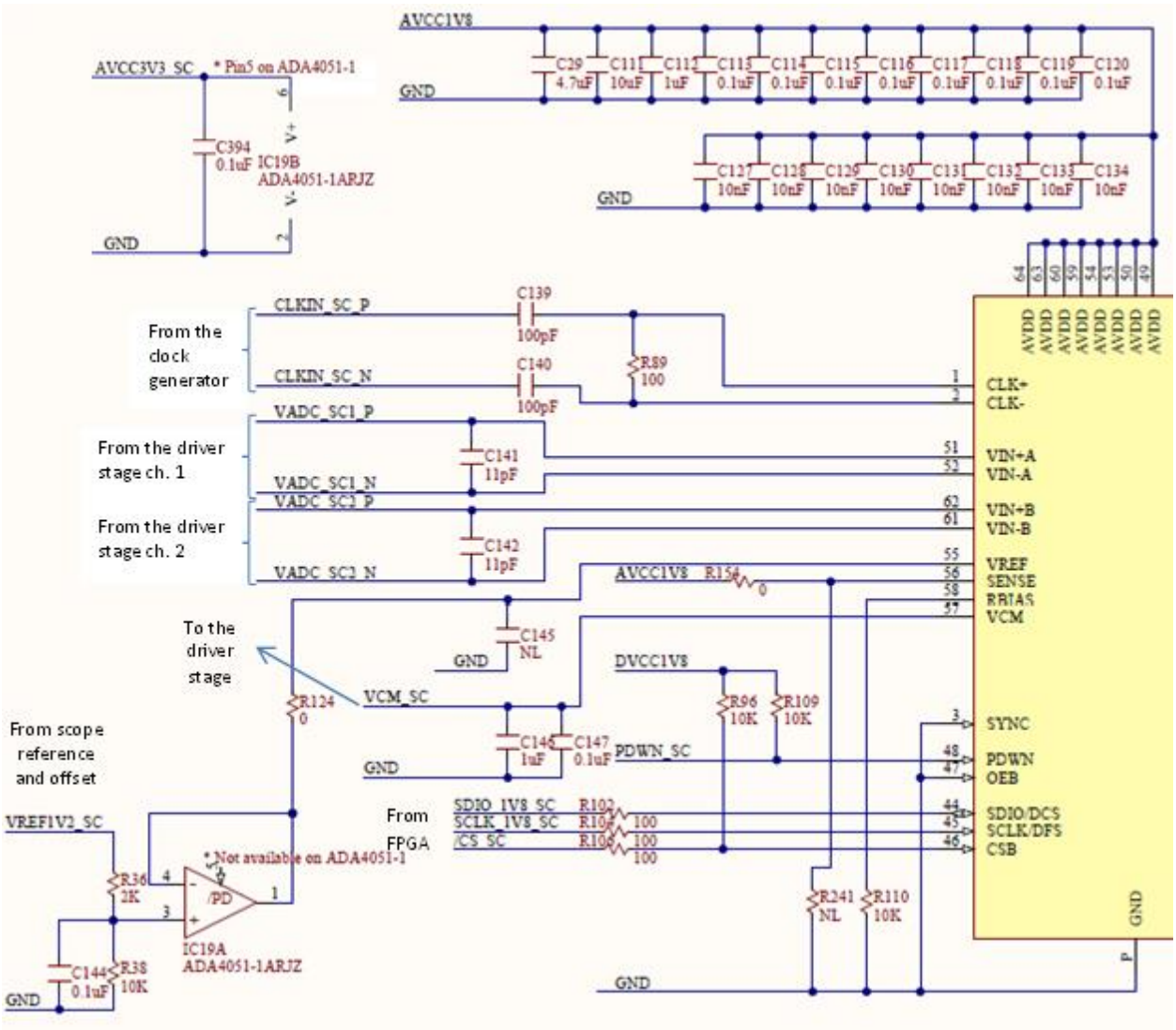

Figure 9. ADC - analog section.

The important features of AD9648:

- SNR = 74.5dBFS @70 MHz
- SFDR =91dBc @70 MHz
- Low power: 78mW/channel ADC core@ 125MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.35 LSB
- Serial port control options
- Offset binary, gray code, or two's complement data format
- Optional clock duty cycle stabilizer
- Integer 1-to-8 input clock divider
- Data output multiplex option
- Built-in selectable digital test pattern generation
- Energy-saving power-down modes

- Data clock out with programmable clock and data alignment

The differential inputs are driven via a low-pass filter comprised of C141 together with R10 through R13, in the buffer stage. The differential clock is AC-coupled and the line is impedance matched. The clock is internally divided by two for operating at a constant 100 MHz sampling rate. An external reference voltage is used, buffered by IC 19. The ADC generates the common mode reference voltage (VCM_SC) to be used in the buffer stage.

The differential input voltage range is: $$-1V < V_{ADC\ diff} < 1V \quad (19)$$

2.6.2 Digital Section

The digital stage of the ADC and the corresponding FPGA bank are supplied at 1.8V.

To minimize the number of used FPGA pins; a multiplexed mode is used, to combine the two channels on a single data bus. CLKOUT_SC is provided to the FPGA for synchronizing data (see Figure 10).

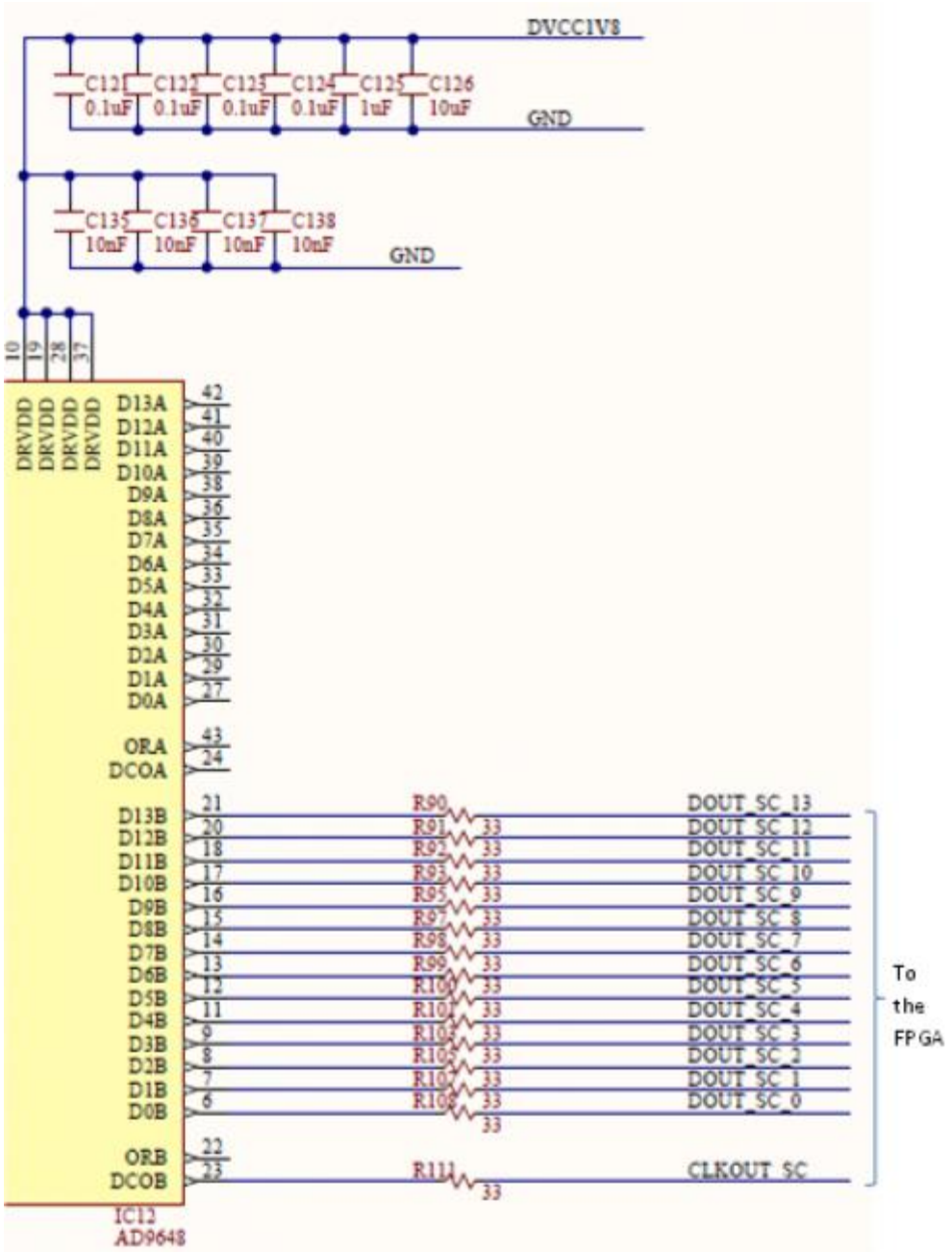

Figure 10. ADC - digital section.

2.7 Scope Signal Scaling

Combining Gain equations **(3)**, **(5)**, **(9)**, **(13)**, **(14)**, and **(15)** from previous chapters, the total scope gains are:

$$\boldsymbol{Low\ Gain} = \frac{\boldsymbol{V_{ADC\ diff}}}{\boldsymbol{V_{in\ diff}}} = \mathbf{0.034}$$

$$\boldsymbol{High\ Gain} = \frac{\boldsymbol{V_{ADC\ diff}}}{\boldsymbol{V_{in\ diff}}} = \mathbf{0.375} \qquad \textbf{(20)}$$

Combining the ADC input voltage range shown in **(19)** with V_{offsc} at the midrange of **(11)** (scope vertical position at 0), the Vin range is:

$$\boldsymbol{at\ Low\ Gain}: \ -\mathbf{30}\boldsymbol{V} < \boldsymbol{V_{in\ diff}} < 28.\mathbf{6}\boldsymbol{V}$$
$$\boldsymbol{at\ High\ Gain}: \ -\mathbf{2.7}\boldsymbol{V} < \boldsymbol{V_{in\ diff}} < 2.6\boldsymbol{V} \qquad \textbf{(21)}$$

To cover component value tolerances and to allow software calibration, only the ranges below are specified.

$$\boldsymbol{at\ Low\ Gain}: \ -\mathbf{25}\boldsymbol{V} < \boldsymbol{V_{in\ diff}} < 25\boldsymbol{V}$$
$$\boldsymbol{at\ High\ Gain}: \ -\mathbf{2.5}\boldsymbol{V} < \boldsymbol{V_{in\ diff}} < 2.5\boldsymbol{V} \qquad \textbf{(22)}$$

The effect of the offset setting (scope vertical position) can be calculated from **(10)**, **(11)** and **(14)**:

$$-\mathbf{2}\boldsymbol{V} < V_{offSC} - \boldsymbol{V_{refSC}} < 2.\mathbf{044}\boldsymbol{V} \qquad \textbf{(23)}$$

The vertical position setting moves the signals vertically on the scope screen (relative to vertical screen center) by $V_{off\ eq\ in}$:

$$\boldsymbol{at\ Low\ Gain}: \ -\mathbf{59.3}\boldsymbol{V} < V_{\boldsymbol{off\ eq\ in}} < 5\mathbf{9.3}\boldsymbol{V}$$
$$\boldsymbol{at\ High\ Gain}: \ -\mathbf{5.39}\boldsymbol{V} < V_{\boldsymbol{off\ eq\ in}} < 5.3\mathbf{9}\boldsymbol{V} \qquad \textbf{(24)}$$

The above adds an equivalent offset voltage $V_{off\ eq\ in}$ to $V_{in\ diff}$, translating the ranges in **(21)** and **(22)** by $V_{off\ eq\ in}$, up to the limits in **(24)**.

Equations **(2)**, **(7)**, **(8)**, **(12)** and **(19)** show signal range boundaries for keeping ICs in the input/output voltage ranges. Combining these with the gain equations, the overall linear scope operation range is shown Figure 1 and Figure 1. Each equation is represented by a closed polygon. Each figure is shown at the full range and at a detailed range. Separate figures are shown for Low Gain and for High Gain. The right hand diagrams use *Vin diff* and *Vin CM* coordinates while left hand ones use *VinP* and *VinN* coordinates.

To be visible on the scope screen and not distorted, a signal should be included in all the solid line polygons of a figure (**linear range** = geometrical intersection of the surfaces).

Only the differential input voltage is shown on the scope screen. The common mode voltage information is removed by the differential structure of the Analog Discovery 2 scope. A signal overpassing the linear range will be distorted on the scope screen, i.e. the graphical representation will be clamped. In the diagrams below, a signal outside the linear range will be clamped to the closest point in the linear range. The clamping point is not necessarily at the scope screen top or bottom edge, as explained below.

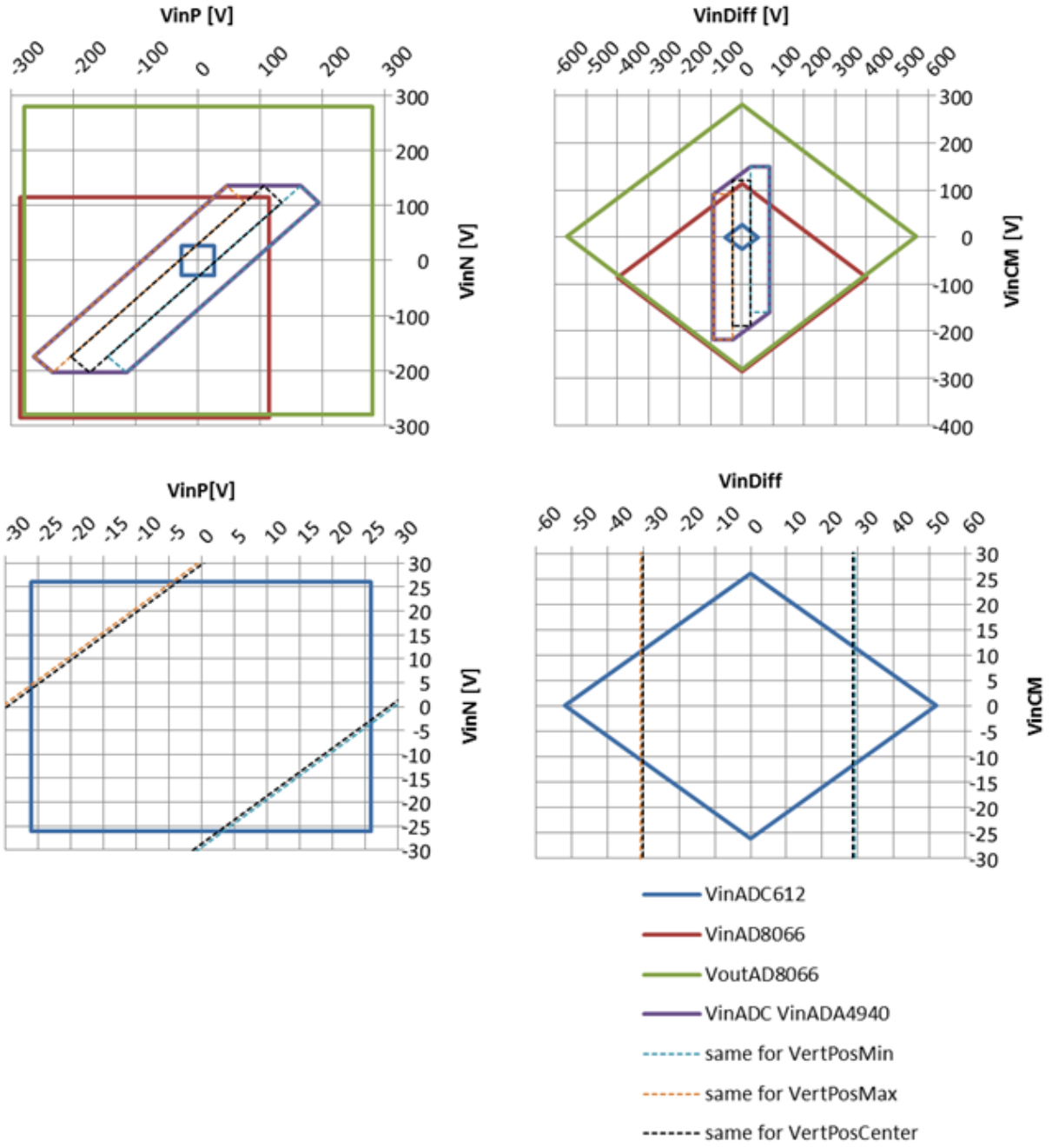

Figure 11. Scope input signal range.

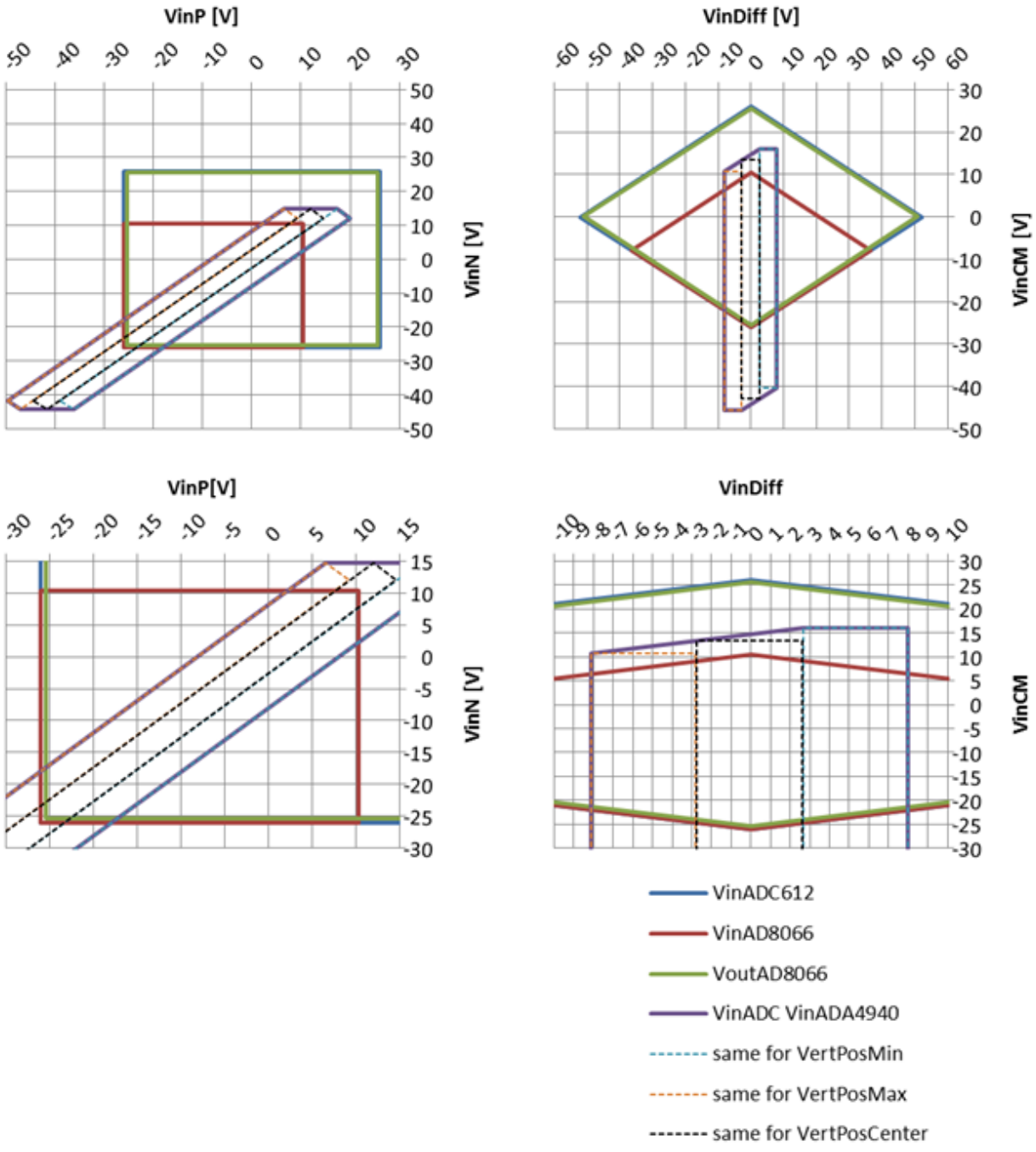

Figure 12. Scope input signal range.

The dashed rectangles represent the display area on the scope screen. There are three dashed rectangles in each diagram: the middle one corresponds to the vertical position set to 0 (*VoffSc = 2.022V* in equation **(11)**. The left one shows the display area when vertical position is set to maximum (*VoffSc = 4.044V*), and the right one corresponds to the minimum (negative) vertical position (*VoffSc = 0V*). Any intermediate vertical position is possible, moving the displayable area (virtual dashed rectangle) to any intermediate position. A signal crossing the long side of the dashed rectangle exceeds the displayable input voltage range causing the ADC to saturate (either at zero or at Full Scale). This is represented on the scope screen with dashed line warning to the user.

A signal keeping within the dashed rectangle but crossing any solid line, overrides electrical limits of intermediate circuits in the signal path (see the legend of the figures). This results in distorting the signal without saturating the

ADC. The software has no information about this situation and cannot warn the user with specific signal representation. It is the user's responsibility to understand and avoid such situations.

For Low Gain (Figure 1), the simple condition to stay in the linear range is to keep both positive and negative inputsV_{inP}, V_{inN} in the ±26V range (as shown by equation **(2)**).

For High Gain (Figure 1), by combining equations **(7)** and **(5)**, both positive and negative inputs in must stay in the range:

$$-26V < V_{inP}, V_{inN} < 10V \quad \textbf{(25)}$$

Additionally, the differential input signal (combined with the equivalent offset voltage – vertical position) is visible only within the range:

$$-7.5V < V_{inDiff} < 7.5V \quad \textbf{(26)}$$

Note the difference between typical parameter values considered by the figures and the safer min/max values used for the equations.

Figure 13 shows an example of a signal distorted due to a common mode input voltage that is too large. They grey line is the reference, not distorted, signal. The differential input voltage is a 4Vpp triangle on top of a -5V DC component. The common mode input voltage is 10V. The vertical position of the scope is set to 5V and high gain is selected. The yellow line shows an identical signal, except the common mode input voltage is 15V.

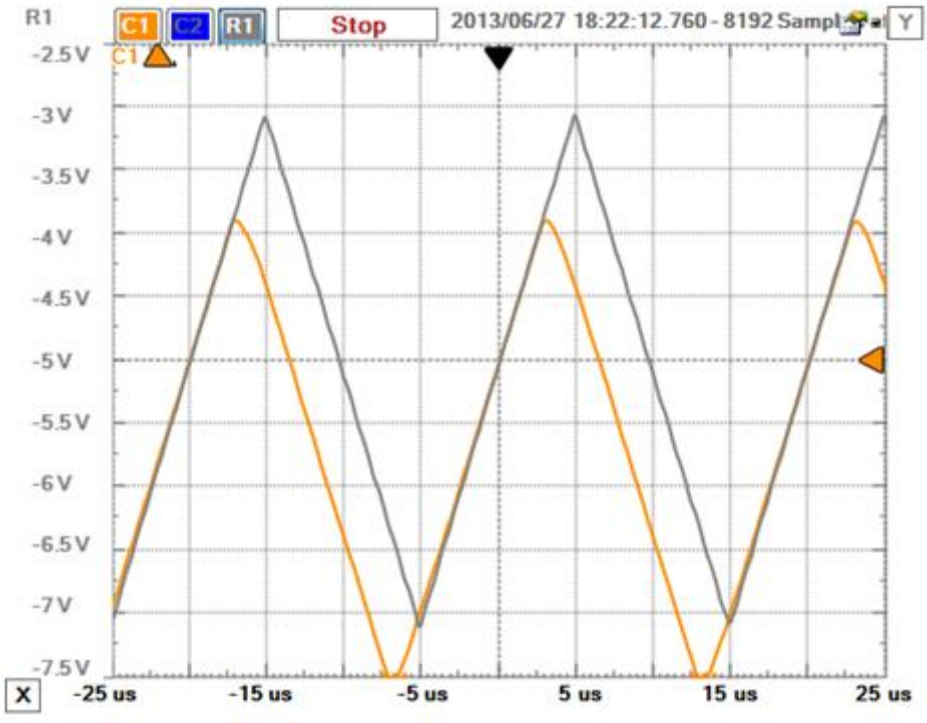

Figure 13. Common mode input voltage limitation.

2.8 Scope Spectral Characteristics

Figure 14 shows a typical spectral characteristic of the scope. An Agilent 3320A 20 MHz Function/Arbitrary Waveform Generator was used to generate the input signal of 1VRMS. The signal swept from 100 Hz to 30 MHz. A coax cable and a Digilent Discovery BNC adapter were used to connect the input signal to the Discovery inputs.

The Network Analyzer was used, the WaveGen was set to External, the Gain was set at x10 (high-gain) for the upper figure, and x0.1 (low-gain) for the lower one. For both scales, the 3dB bandwidth is 30 MHz+. The 0.5dB badwidth is 10 MHz and the 0.1dB bandwidth is 5 MHz.

The standard -3dB bandwidth definition is derived from filter theory. At cutout frequency, the scope attenuates the spectral components by 0.707, assuming an error of ~30%, way too high for a measuring instrument. The bandwidth with a specified flatness is useful to better define the scope spectral performances. The Analog Discovery 2 exhibits 10 MHz @ 0.5dB, meaning that a 10 MHz sinusoidal signal is shown with a flatness error of a max 5.6%. 5 MHz @ 1dB means that a 5 MHz sinusoidal signal is shown with a flatness error of a max 1.5%.

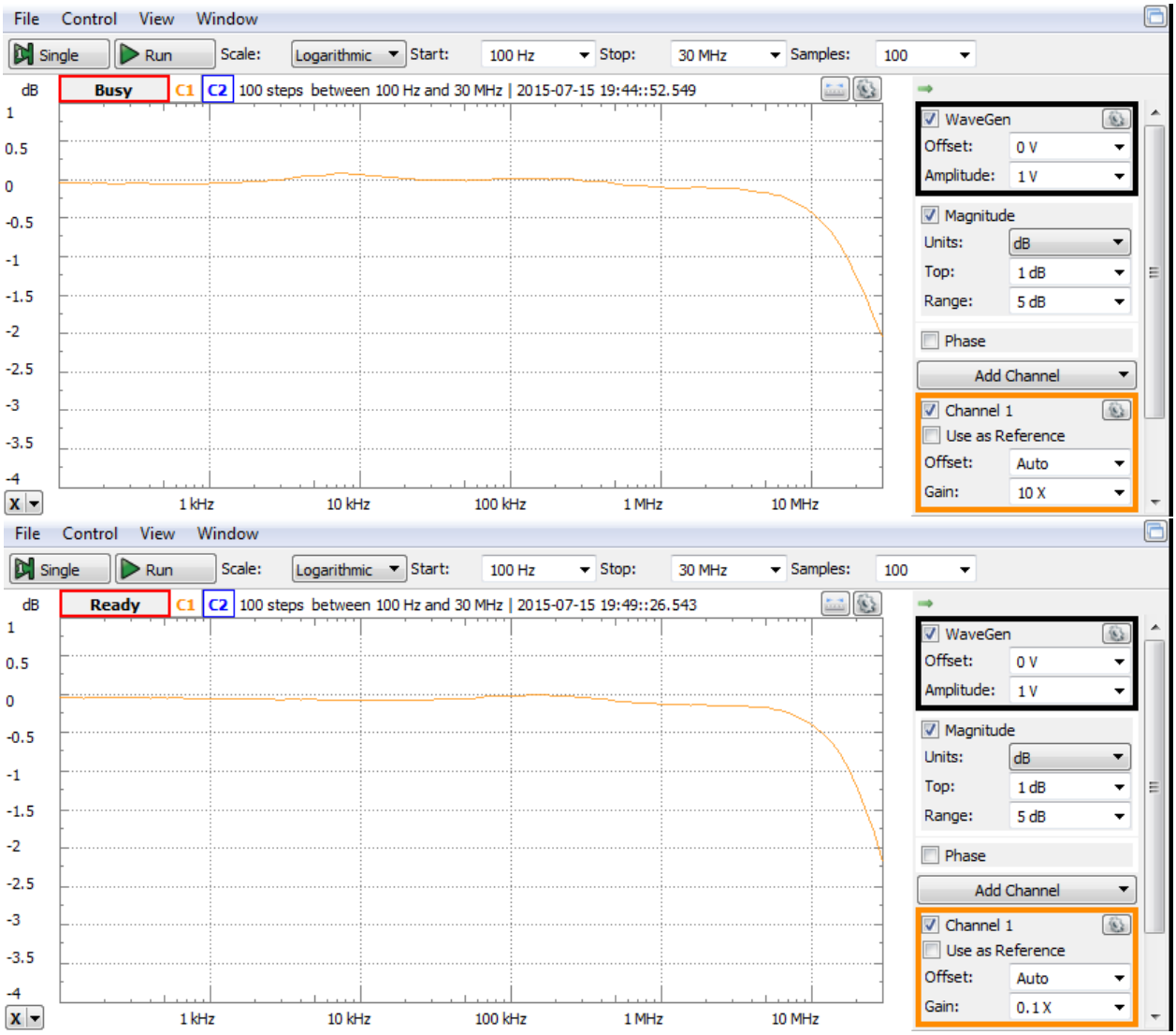

Figure 14. Scope spectral characteristic diagram

- Low Gain (up)
- High Gain (down)

As shown above, the measurements in Figure 14 were taken with a coax cable and a Digilent Discovery BNC adapter. This is the optimal setup that allows maximal Analog Discovery 2 spectral performance. The wire kit included with the Analog Discovery 2 is a cheap, easy-to-use probing solution. However, the wire kit reduces the bandwidth of the scope and is susceptible to inducing noise and crosstalk from adjacent circuits.

3 Arbitrary Waveform Generator

3.1 AWG DAC

The Analog Devices AD9717 dual, low-power 14-bit TxDAC digital-to-analog converter is used to generate the wave (Figure 15). The main features are:

- Power dissipation @ 3.3V, 2 mA output: 86 mW @ 125 MSPS, sleep mode: < 3 mW @ 3.3V
- Supply voltage: 1.8V to 3.3V
- SFDR to Nyquist: 84 dBc @ 1 MHz output, 75 dBc @ 10 MHz output
- AD9717 NSD @ 1 MHz output, 125 MSPS, 2 mA: −151 dBc/Hz
- Differential current outputs: 1 mA to 4 mA
- CMOS inputs with single-port operation
- Output common mode: 0 to 1.2 V
- Small footprint, 40-lead LFCSP RoHS-compliant package

The parallel data bus and the SPI configuration bus are driven by the FPGA. The single ended 100 MHz clock is provided by the clock generator. External Vref1V_AWG reference voltage is used. The output currents (Iout_AWGx_P and _N) are converted to voltages in the I/V stage. The Full Scale is set via the FSADJx pins (see Figure 1). The ADG787 2.5Ω CMOS Low Power Dual 2:1 MUX/DEMUX is used to connect R_set of either 8kΩ or 32kΩ from FSADJx pin to GND.

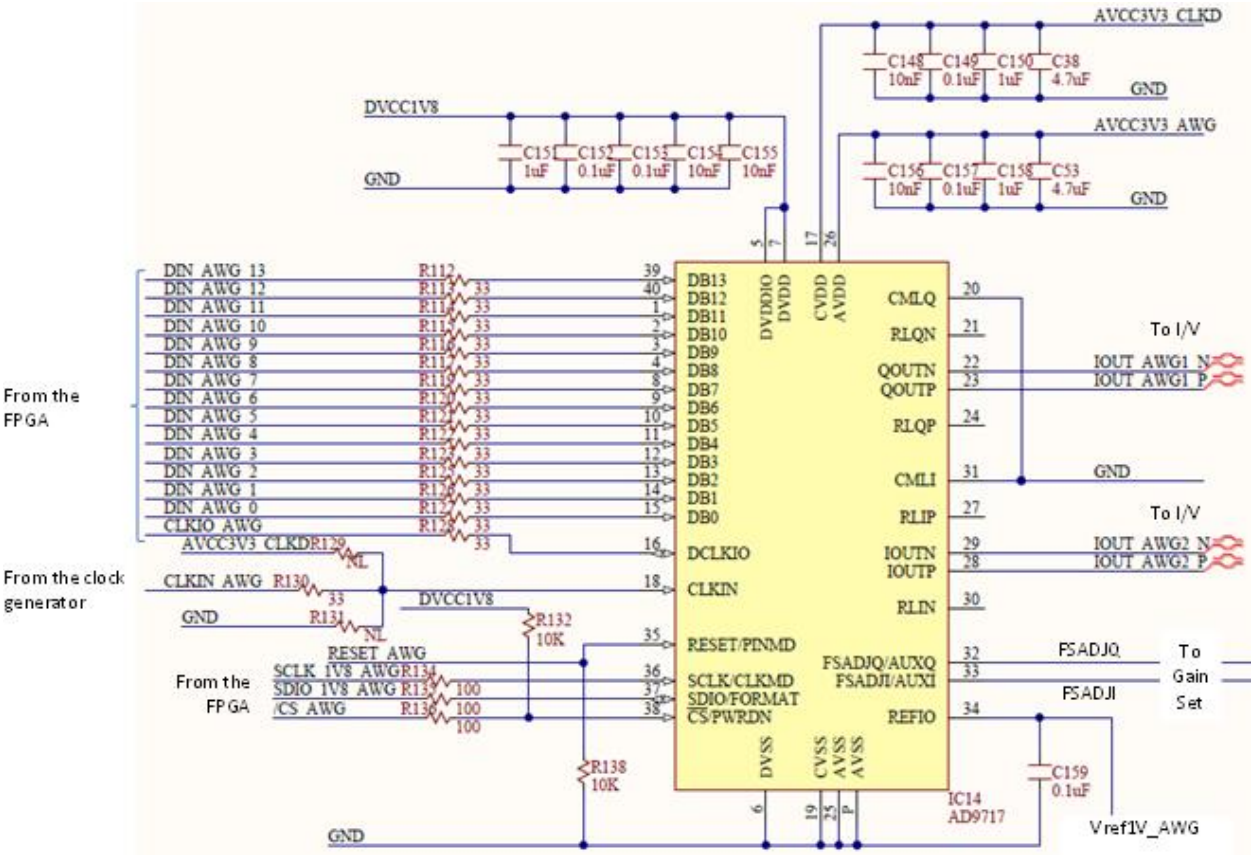

Figure 15. DAC.

The ADG787 features:

- -3 dB bandwidth, 150 MHz
- Single-supply 1.8V to 5.5V operation
- Low on resistance: 2.5 Ω typical

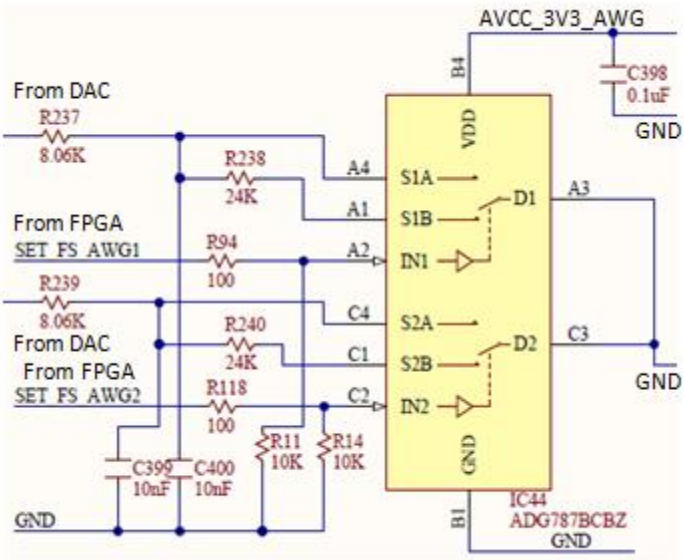

Figure 16. DAC - gain set.

3.2 AWG Reference and Offset

As shown in Figure 16, the reference voltage for the AWG is generated by IC42 (ADR3412ARJZ). A divided version is provided to the DAC:

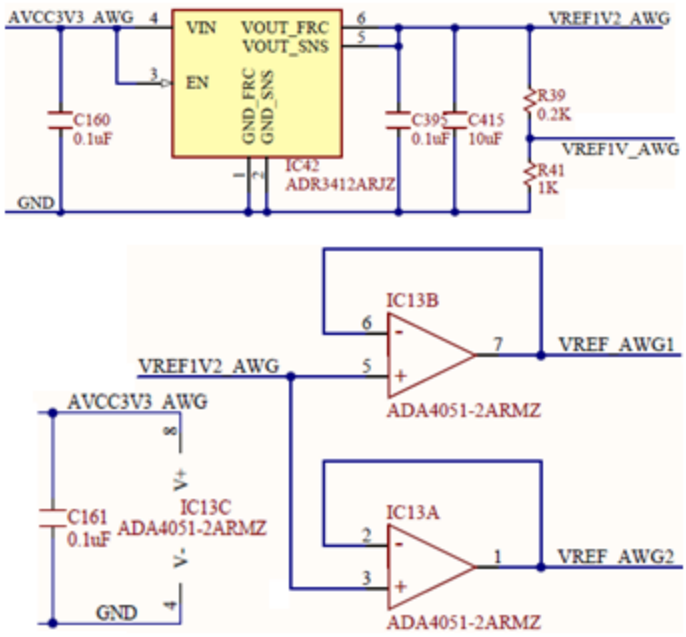

Figure 17. DAC - Reference voltages.

$$V_{ref1V\_AWG} = V_{ref1V2\_AWG} \cdot \frac{R_{41}}{R_{39} + R_{41}} = 1V \quad (27)$$

Buffered versions are provided to the I/V stages and individually for each AWG channel, to minimize crosstalk.

The Full Scale DAC output current is:

$$I_{outAWGFS} = 32 \cdot \frac{V_{ref1V\_AWG}}{R_{set}} \quad (28)$$

For High Gain:

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{8k\Omega} = 4mA \quad (29)$$

For Low Gain:

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{32k\Omega} = 1mA \quad (30)$$

An AD5645R Quad 14-bit nanoDAC generates the offset voltages to add a DC component to the AWG output signal (Figure 18). The same circuit also generates VSET+ USR and VSET- USR, used to set the +/= user supplied voltages.

- Low power, smallest quad 14-bit nanoDAC
- 2.7 V to 5.5 V power supply
- Monotonic by design
- Power-on reset to zero scale/midscale (important for starting the AWG with 0 DC component)

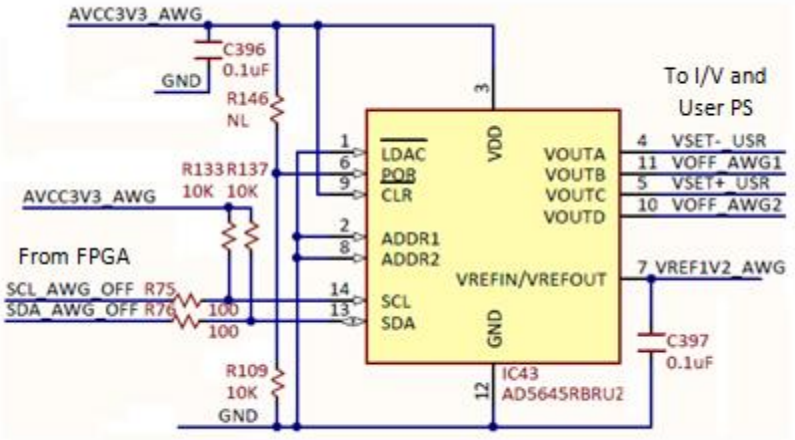

Figure 18. DAC - Offset voltages.

The Full Scale voltage of IC43 is:

$$V_{offAWGFS} = V_{SET\_USRFS} = V_{ref1V2AWG} = 1.2V \quad (31)$$

4.3 AWG I/V

IC 15 in

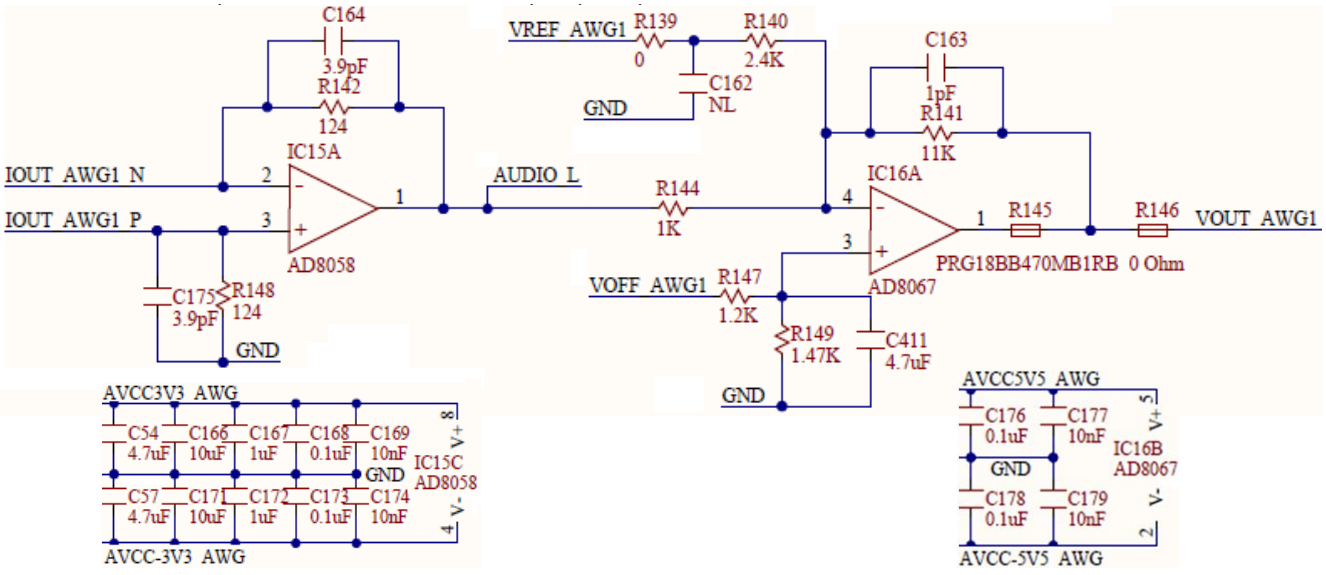

Figure 19. AWG I/V and out.

Important AD8058 features:

- Low cost
- 325 MHz, −3 dB bandwidth (G = +1)
- 1000 V/µs slew rate
- Gain flatness: 0.1 dB to 28 MHz
- Low noise: 7 nV/√Hz
- Low power: 5.4 mA/amplifier typical @ 5 V
- Low distortion: −85 dBc@5MHz, RL=1kΩ
- Wide supply range from 3 V to 12 V
- Small packaging

$$\begin{gathered} \boldsymbol{V_{Audio} = I_{outAWGP} \cdot R_{148} - I_{outAWGN} \cdot R_{142} =} \\ \boldsymbol{= (1 - 2 \cdot \{A_U\}) \cdot I_{outAWGFS} \cdot R_{142} = \{A_B\} \cdot I_{outAWGFS} \cdot R_{142}} \end{gathered} \quad \textbf{(32)}$$

Where:

$$\begin{gathered} \boldsymbol{\{A_U\} = \frac{D}{2^N} \in [0 \dots 1);\ -\ normalized\ unipolar\ DAC\ input\ number} \\ \boldsymbol{\{A_B\} = (1 - 2 \cdot \{A_U\}) \in [-1 \dots 1);\ -\ normalized\ bipolar\ DAC\ input\ number\ (binary\ offset)} \\ \boldsymbol{D \in [0 \dots 2^{14}) = [0 \dots 2^{14} - 1];\ -\ integer\ unipolar\ DAC\ input\ number} \end{gathered} \quad \textbf{(33)}$$

The Voltage range extends between:

$$\boldsymbol{-V_{AudioFS} \leq V_{Audio} < -V_{AudioFS}} \quad \textbf{(34)}$$

Where (for High Gain respectively Low Gain):

$$\begin{gathered} \boldsymbol{V_{AudioFS\_HG} = I_{outAWGFS\_HG} \cdot R_{142} = 496\text{mV}} \\ \boldsymbol{V_{AudioFS\_LG} = I_{outAWGFS\_LG} \cdot R_{142} = 124\text{mV}} \end{gathered} \quad \textbf{(35)}$$

3.4 AWG Out

IC16 in

Figure 19 is the output stage of the AWG. AD8067 features:

- FET input: 0.6 pA input bias current
- Stable for gains ≥8 for High-Capacitive Load
- High speed: 54 MHz@−3 dB (G = +10)
- 640 V/µs slew rate
- Low noise:6.6 nV/√Hz; 0.6 fA/√Hz
- Low offset voltage (1.0 mV max)
- Rail-to-rail output
- Low distortion: SFDR 95 dBc @ 1 MHz
- Low power: 6.5 mA typical supply current

- Low cost; Small packaging: SOT-23-5

Matching the impedances in the inverting and non-inverting inputs of IC16:

$$\frac{\mathbf{1}}{\mathbf{R_{140}}}+\frac{\mathbf{1}}{\mathbf{R_{141}}}+\frac{\mathbf{1}}{\mathbf{R_{144}}}=\frac{\mathbf{1}}{\mathbf{R_{147}}}+\frac{\mathbf{1}}{\mathbf{R_{149}}} \quad \textbf{(36)}$$

$$\boldsymbol{V_{outAWG}} = -\boldsymbol{V_{Audio}}\cdot\frac{\mathbf{R_{141}}}{\mathbf{R_{144}}}+\left(\mathbf{2}\cdot\boldsymbol{V_{offAWG}}-\boldsymbol{V_{ref1V2AWG}}\right)\cdot\frac{\mathbf{R_{141}}}{\mathbf{R_{140}}} \quad \textbf{(37)}$$

The first term in equation **(37)** represents the actual wave amplitude, with a range of:

$$\begin{aligned} -5.45V < -\mathbf{5V} < V_{ACoutAWG\_HG} < \mathbf{5V} < 5.45V \\ -1.36V < \mathbf{1.25V} < V_{ACoutAWG\_LG} < \mathbf{1.25V} < 1.36V \end{aligned} \quad \textbf{(38)}$$

Low-gain is used to generate low amplitude signals with improved accuracy. Any amplitude of the output signal is derivable by combining LowGain/HighGain setting (rough) with the digital signal amplitude (fine).

The second term in equation **(37)** shows the DC component (AWG offset), with a range of (for either LowGain or HighGain):

$$-5.5V < \mathbf{5V} < V_{DCoutAWG} < \mathbf{5V} < 5.5V \quad \textbf{(39)}$$

AD8067 is supplied with $\pm 5.5V$; to avoid saturation the user should keep the sum of AC and DC components in **(37)** to:

$$-5.5V < \mathbf{5V} < V_{outAWG} < \mathbf{5V} < 5.5V \quad \textbf{(40)}$$

Only **bolded** ranges are used in equations **(38)**, **(39)** and **(40)**, for providing tolerance margins.

The R145 PTC thermistor provides thermal protection in case of an output shortcut.

3.5 Audio

A stereo audio output combines the two AWG channels (Figure 20). AD8592 was used for its features:

- Single-supply operation: 2.5 V to 6 V
- High output current: ±250 mA
- Low shutdown supply current: 100 nA
- Low supply current: 750 µA/Amp
- Very low input bias current

A single 3.3V supply is used.

$$\boldsymbol{V_{outIC18}} = -\mathbf{2}\cdot\boldsymbol{V_{Audio}}+\mathbf{1.5V} \quad \textbf{(41)}$$

The first term in equation **(41)** is the audio signal. The second term is the common mode DC component, removed by AC coupling.

The audio signal range is:

$$V_{AudioJack} = -2 \cdot V_{Audio}$$
$$-992mV < V_{AudioJack} < 992mV \ (High\ Gain)$$
$$-248mV < V_{AudioJack} < 248mV \ (Low\ Gain) \qquad (42)$$

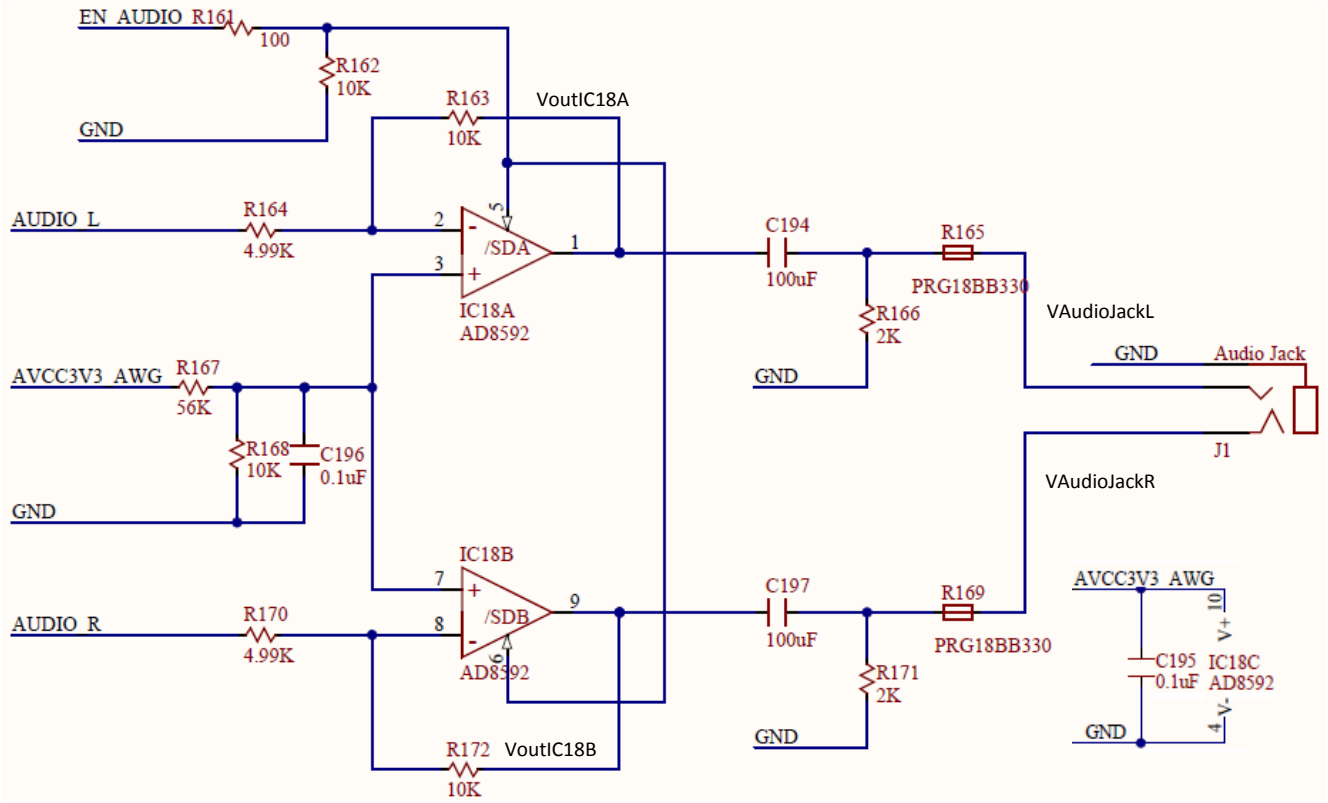

Figure 20. Audio.

3.6 AWG Spectral Characteristics

Figure 21 shows the typical spectral characteristic of the AWG. In the first experiment (solid line), a coax cable and a Digilent Discovery BNC adapter were used to connect the AWG signal to the Scope inputs. For the second experiment (dashed line), the AWG was connected to the scope inputs via the Analog Discovery wire kit. The Analog Discovery Scope hardware was considered a reference for the experiments above because it has preferred spectral characteristics to the AWG.

The Network Analyzer virtual instrument in WaveForms is used to perform synchronized signal synthesis and acquisition. It takes control of channel 1 of AWG and of both scope channels. Start/Stop frequencies are set to

10kHz/10MHz, respectively. Sinus amplitude is set to 1V. The characteristic is built in 1000 steps. The 0.5dB bandwidth is 5.5 MHz with the coax cable and 3.6 MHz with the wire kit.

Similar to the Scope stage, the AWG exceeds the requirement of 5 MHz bandwidth.

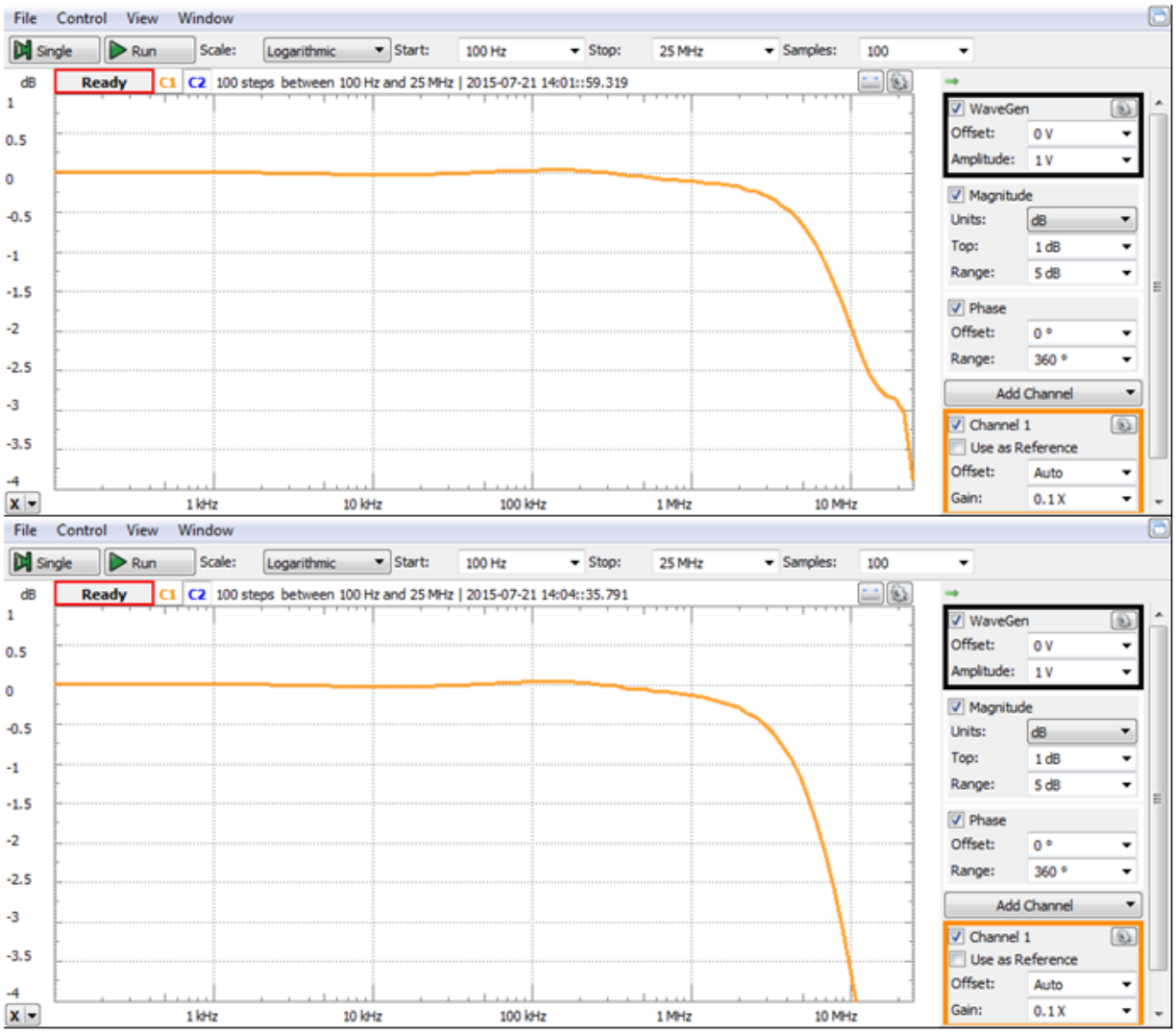

Figure 21. AWG spectral characteristic.

4 Calibration Memory

The analog circuitry described in previous chapters includes passive and active electronic components. The datasheet specs show parameters (resistance, capacitance, offsets, bias currents, etc.) as typical values and tolerances. The equations in previous chapters consider typical values. Component tolerances affect DC, AC, and CMMR performances of the Analog Discovery. To minimize these effects, the design uses:

- 0.1% resistors and 1% capacitors in all the critical analog signal paths
- Capacitive trimmers for balancing the Scope Input Divider and Gain Selection

- No other mechanical trimmers (as these are big, expensive, unreliable and affected by vibrations, aging, and temperature drifts)
- Software calibration, at manufacturing
- User software calibration, as an option

A software calibration is performed on each device as a part of the manufacturing test. AWG signals are passed to a reference instrument and reference signals are connected to the Scope inputs. A set of measurements is used to identify all the DC errors (Gain, Offset) of each analog stage. Correction (Calibration) parameters are computed and stored in the Calibration Memory, on the Analog Discovery device, as Factory Calibration. The WaveForms software allows the user performing an in-house calibration and overwrite the Calibration Data. Returning to Factory Calibration is always possible.

The WaveForms Software reads the calibration parameters from the connected Analog Discovery and uses them to correct both generated and acquired signals.

5 Digital I/O

Figure 22 shows half of the Digital I/O pin circuitry (the other half is symmetrical). J3 is the Analog Discovery 2 user signal connector.

General purpose FPGA I/O pins are used for Analog Discovery 2 Digital I/O. FPGA pins are set to SLOW slew rate and 4mA drive strength, with no internal pull.

PTC thermistors provide thermal protection in case of shortcuts. Schottky Diodes double the internal FPGA ESD protection diodes for increasing the acceptable current in case of overvoltage. Nominal resistance of the PTCs (220Ω) and parasitical capacitance of the Schottky diodes (2.2pF) and FPGA pins (10pF) limit the bandwidth of the input pins. For output pins, the PTCs and the load impedance limit the bandwidth and power.

Input and output pins are LVCMOS3V3. Inputs are 5V tolerant. Overvoltage up to ±20V is supported.

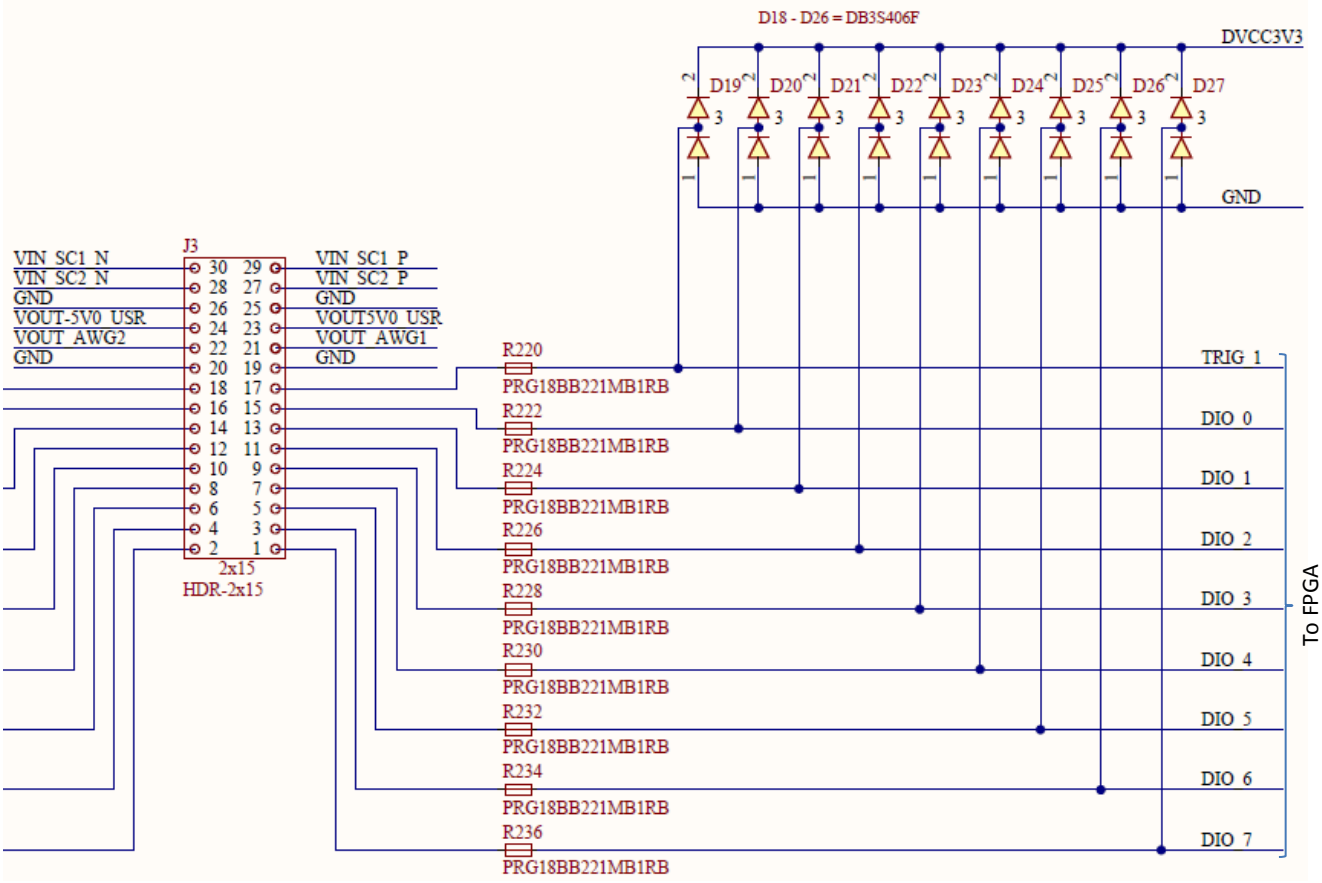

Figure 22. Digital I/O.

6 Power Supplies and Control

This block includes all power monitoring and control circuitry, internal power supplies, and user power supplies.

6.1 USB Power Control

As shown in Figure 23, the Analog Discovery 2 can be supplied either from the USB port (VBUS) or from an external power supply (J4 connector).

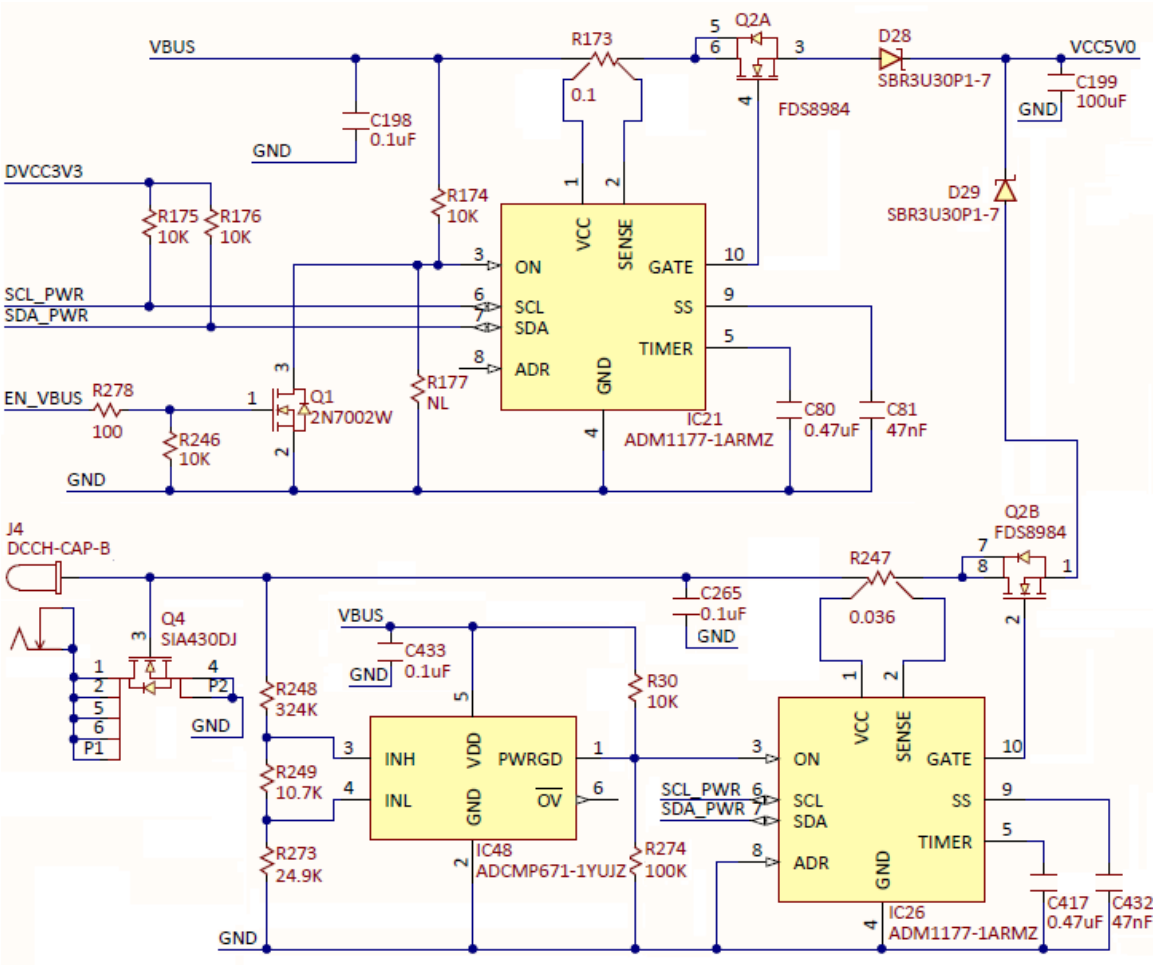

Figure 23. USB power control.

The external power input is protected against reverse voltage; Q4 turns OFF if a floating power supply with negative polarity on central pin of J4 is used. However, the device is not protected for a very unlikely use case:

- Analog Discovery 2 connected to the USB port of a PC which has GND connected to EARTH
- External power supply with negative polarity on central pin of J4 and with exterior pin connected to EARTH.

In this case, the external EARTH loop acts as a shortcut of Q4.

ADCMP671 is a window comparator with the following features:

- Window monitoring with minimum processor I/O
- Individually monitoring N rails with only N + 1 processor I/O
- 400 mV ± 0.275% threshold at VDD = 3.3 V, 25°C
- Supply range: 1.7 V to 5.5 V
- Low quiescent current: 8.55 µA maximum
- Input range includes ground
- Internal hysteresis: 9.2 mV typical
- Low input bias current: ±2.5 nA maximum
- Open-drain outputs
- Power good indication output
- Designated over voltage indication output

- Low profile (1 mm), 6-lead TSOT package

IC48 drives PWRGD output HIGH (turning IC26 ON) when Vext is in the range:

$$\mathbf{4.11V} = \mathbf{400mV} \cdot \frac{\boldsymbol{R_{248} + R_{249} + R_{273}}}{\boldsymbol{R_{249} + R_{273}}} < V_{ext} < 400\mathbf{mV} \cdot \frac{\boldsymbol{R_{248} + R_{249} + R_{273}}}{\boldsymbol{R_{273}}} = \mathbf{5.76V} \quad \textbf{(43)}$$

The Analog Discovery 2 exhibits two main powering modes: **USB** and **External**. Temporary modes (**Racing OFF**, **USB OFF** and **Racing**) are explained here for design clarifications, but have no importance for the user observed behavior.

- **Racing OFF –** immediately after reset, before FPGA is programmed, if an external power supply is attached and in the right range (PWRGD = HIGH).
- **USB OFF –** immediately after reset, before FPGA is programmed, if external power supply is missing or out-of-range (PWRGD = LOW).
- **USB –** all the power is drained from the Vbus (IC21 = ON, IC26 = OFF). The external power supply is either missing or out of the right voltage range. The power available for both User Supplies is limited to 0.7W.
- **Racing –** when external power supply is in the right voltage range (PWRGD = HIGH), before WaveForms stops the USB Power Controller. During racing mode, both USB Power Controller (IC21) and External Power controller (IC26) are ON, the device drains power from whatever supply has a higher voltage (D28 and D29 work as a maxim voltage detector). The Racing mode is temporary, it ends when the FPGA is configured and communicates with the WaveForms software. During **Racing** mode, the power available for User Supplies is limited.
- **External –** the device is powered from an external supply (via the 5V DC connector and IC26). Vext is in the range shown by equation **(43)** (PWRGD = HIGH, and WaveForms already stopped the USB Power Controller (IC21). The User Supplies current and power limits are increased to 700mA or 2.1W each. The only circuit still supplied from the USB VBUS is the USB controller (IC41).

At Power ON, the FPGA is not programmed, EN_VBUS is HiZ, the pulldown resistor R246 turns Q1 OFF, IC21 is ON via R174. The Analog Discovery 2 starts in **USB OFF** mode (when PWRGD = LOW) or **Racing OFF** mode (when PWRGD = HIGH). The WaveForms software first configures the FPGA, and the device turns into **USB** or **Racing** mode, depending on presence/absence of correct external supply voltage. The FPGA continuously monitors the voltage at the 5V DC connector. When detecting the **Racing** mode (PWRGD = HIGH), WaveForms sends the command to drive EN_VBUS HIGH, turning the USB Power Controller (IC21) OFF, thus switching to **External** mode.

If external Power Supply is attached after WaveForms started and runs several instruments, the device steps seamlessly trough **USB** -> **Racing** -> **External** modes. Running instruments are not affected, except User Supplies get more available power.

However, removing the external power supply during **External** mode is not seamless. Only the USB controller keeps working (as supplied from the USB port). The FPGA gets unpowered and loses configuration data. The device stops all the instruments, EN_VBUS go HiZ, which leads to the **USB OFF** mode. WaveForms will prompt the user to select the device, which will re-program the FPGA. All the instruments can then be run, in the **USB** mode.

An ADM1177 Hot Swap Controller and Digital Power Monitor with Soft Start Pin is used to provide USB power compliance during **USB** and **Racing** modes (IC21 in Figure 2).

Remarkable ADM1177 features are:

- Safe live board insertion and removal

- Supply voltages from 3.15 V to 16.5 V
- Precision current sense amplifier
- 12-bit ADC for current and voltage read
- Adjustable analog current limit with circuit breaker
- ±3% accurate hot swap current limit level
- Fast response limits peak fault current
- Automatic retry or latch-off on current fault
- Programmable hot swap timing via TIMER pin
- Soft start pin for reference adjustment and programming of initial current ramp rate
- I2C fast mode-compliant interface (400 kHz maximum)

When enabled, (in **USB** or **Racing** modes), IC21 limits the current consumed from the USB port to:

$$\boldsymbol{I_{limit} = \frac{100mV}{R_{173}} = \frac{100mV}{0.1\Omega} = 1A} \quad \textbf{(44)}$$

For a maximum time of:

$$\boldsymbol{t_{fault} = 21.7[ms/\mu F] \cdot C_{80} = 21.7[ms/\mu F] \cdot 0.47\mu F = 10.2ms} \quad \textbf{(45)}$$

If the consumed current does not fall below I_{limit} before t_{fault}, IC21 turns off Q2A. A hot swap retry is initiated after:

$$\boldsymbol{t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550\left[\frac{ms}{\mu F}\right] \cdot 0.47\mu F = 258.5ms} \quad \textbf{(46)}$$

To avoid a current rush at hot swap, Soft Start circuitry limits the current slop to:

$$\boldsymbol{\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{81}} \cdot \frac{1}{10 \cdot R_{173}} = 212\frac{mA}{ms}} \quad \textbf{(47)}$$

If the current drops below I_{limit} before t_{fault}, normal operation begins.

Similarly, IC26 (in **Racing** or **External** modes), limits the current consumed from the external power supply to:

$$\boldsymbol{I_{limit} = \frac{100mV}{R_{247}} = \frac{100mV}{0.036\Omega} = 2.78A} \quad \textbf{(48)}$$

$\boldsymbol{t_{fault}}$ and $\boldsymbol{t_{cool}}$ are same as for IC21, and the current slope limit is:

$$\boldsymbol{\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{432}} \cdot \frac{1}{10 \cdot R_{247}} = 591\frac{mA}{ms}} \quad \textbf{(49)}$$

The Analog Discovery 2 user pins are overvoltage protected. Overvoltage (or ESD) diodes short when a user pin is overdriven by the external circuitry (Circuit Under Test), back powering the input/output block and all the circuits sharing the same internal power supply. If the back-powered energy is higher than the used energy, the bi-directional power supply recovers the difference and delivers it to the previous node in the power chain.

Eventually, the back-powering energy could arrive to the USB VBUS, raising the voltage above the 5V nominal value. D28 in Figure 2 protects the PC USB port against such a situation.

6.2 Analog Supply Control

During **USB** mode, the FPGA constantly reads from IC21 the current value through R173. (Optionally displayed on Main Window/Discovery or Status button). A warning is generated when exceeding 500mA (Status: OC = Over Current). If a value of 600mA is reached and Overcurrent protection is enabled (MainWindow/Device/Settings/Overcurrent protection), WaveForms turns off IC20 (ADP197) shown in Figure 14 and IC27 shown Figure 2, disabling the analog blocks and user power supplies.

ADP197 main features:

- Low RDSon of 12mΩ
- Low input voltage range: 1.8V to 5.5V
- 1.2V logic compatible enable logic
- Overtemperature protection
- Ultrasmall 1.0mmX1.5mm, 6 ball, 0.5mm pitch WLCSP

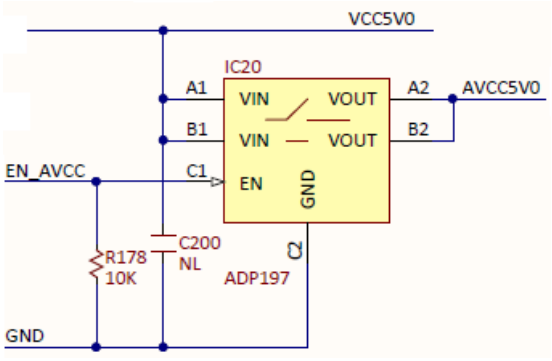

Figure 1. Analog supply control.

6.3 User Supply Control

IC27 in Figure 25 controls the power available for the user supplies. ADM1270 was selected for its main features:

- Controls supply voltages from 4 V to 60 V
- Gate drive for low voltage drop reverse supply protection
- Gate drive for P-channel FETs
- Inrush current limiting control
- Adjustable current limit
- Foldback current limiting
- Automatic retry or latch-off on current fault
- Programmable current-limit timer for safe operating area (SOA)
- Power-good and fault outputs
- Analog undervoltage (UV) and overvoltage (OV) protection
- 16-lead 3x3mm LFCSP package
- 16-lead QSOP package

IC27 limits the current consumed by both user power supplies together. The WaveForms software commands the FPGA to change the limit, depending on the power mode.

During **USB** and **Racing** modes, SET_ILIM_USR pin is driven LOW by the FPGA. The voltage at the ISET pin of IC27 is:

$$V_{Iset} = \frac{\frac{V_{cap}}{R_{253}}}{\frac{1}{R_{253}} + \frac{1}{R_{254}} + \frac{1}{R_{255}}} = \frac{\frac{3.6V}{10k\Omega}}{\frac{1}{10k\Omega} + \frac{1}{1.74k\Omega} + \frac{1}{22.6k\Omega}} = 0.5V \quad (50)$$

The current limit is set to:

$$I_{limit} = \frac{V_{Iset}}{40 \cdot R_{21}} = \frac{0.5V}{40 \cdot 0.043\Omega} = 290mA \quad (51)$$

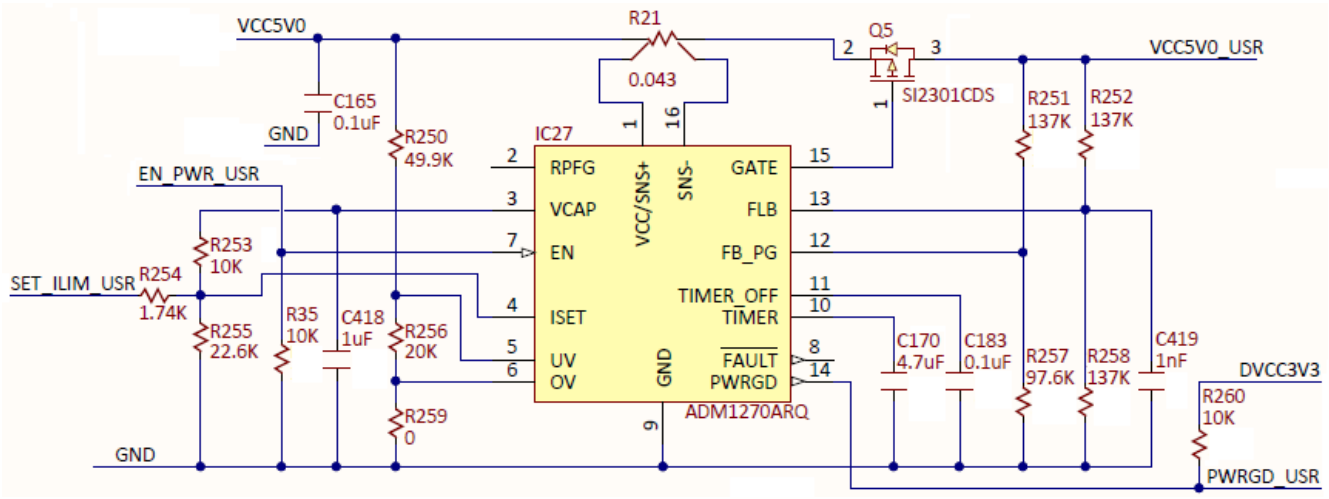

Figure 25. User supplies control.

During **External** and **OFF** modes, SET_ILIM_USR pin is driven HiZ by the FPGA. The voltage at the ISET pin of IC27 is:

$$V_{Iset} = \frac{V_{cap} \cdot R_{255}}{R_{253} + R_{255}} = \frac{3.6V \cdot 22.6k\Omega}{10k\Omega + 22.6k\Omega} = 2.5V \quad (52)$$

The current limit is set to:

$$I_{limit} = \frac{V_{Iset}}{40 \cdot R_{21}} = \frac{2.5V}{40 \cdot 0.043\Omega} = 1.45A \quad (53)$$

In both cases, I_{limit} is allowed for a maximum time of:

$$t_{fault} = 21.7[ms/\mu F] \cdot C_{170} = 21.7[ms/\mu F] \cdot 4.7\mu F = 102ms \quad (54)$$

If the consumed current does not fall below I_{limit} before t_{fault}, IC21 turns off Q2. A hot swap retry is initiated after:

$$t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550[ms/\mu F] \cdot 4.7\mu F = 2.585s \quad (55)$$

Soft Start is not used; C183 is a No Load.

If the current drops below I_{limit} before t_{fault}, normal operation begins.

The current limited by equations **(51)** and **(53)** is shared by both positive and negative user power supplies. After considering the efficiency of the user supply stages, about 100mA is available for user in both supplies together, in **USB Only** mode. In **External** mode, the current/power limit for user is set in the User Voltage Supplies, as explained below.

6.4 User Voltage Supplies

The user power supplies (Figure 26. 6) use ADP1612 Switching Converter in Buck-Boost DC-to-DC topology. Main features:

- 1.4A current limit
- Minimum input voltage 1.8V
- Pin-selectable 650 kHz or 1.3 MHz PWM frequency
- Adjustable output voltage up to 20 V
- Adjustable soft start
- Undervoltage lockout

IC46A/B op amps insert the command voltages VSET+_USR, respectively VSET-_USR in the feedback loop. Additionally, IC46B introduces the required inversion for the negative supply.

Since the op amps are included in negative feedback loops, the input pins voltages are equal:

$$V_{+IC46A} = \frac{\frac{V_{OUT+\_USR}}{R_{188}} + \frac{V_{SET+\_USR}}{R_{193}}}{\frac{1}{R_{188}} + \frac{1}{R_{193}}} = V_{-IC46A} = \frac{\frac{V_{FB}}{R_{266}}}{\frac{1}{R_{265}} + \frac{1}{R_{266}}} \quad (56)$$

$$V_{+IC46B} = \frac{\frac{V_{OUT-\_USR}}{R_{187}} + \frac{V_{FB}}{R_{270}}}{\frac{1}{R_{187}} + \frac{1}{R_{270}}} = V_{-IC46B} = \frac{\frac{V_{SET-\_USR}}{R_{190}}}{\frac{1}{R_{72}} + \frac{1}{R_{190}}} \quad (57)$$

The input impedances for the op amps are matched:

$$\frac{1}{R_{188}} + \frac{1}{R_{193}} = \frac{1}{R_{265}} + \frac{1}{R_{266}} \quad (58)$$

$$\frac{1}{R_{187}} + \frac{1}{R_{270}} = \frac{1}{R_{72}} + \frac{1}{R_{190}} \quad (59)$$

The user voltages are:

$$V_{OUT+\_USR} = V_{FB} \cdot \frac{R_{188}}{R_{266}} - V_{SET+_{USR}} \cdot \frac{R_{188}}{R_{193}} = 5.33V - 4.87 \cdot V_{SET+\_USR} \quad (60)$$

$$V_{OUT-\_USR} = -V_{FB} \cdot \frac{R_{187}}{R_{270}} + V_{SET-\_USR} \cdot \frac{R_{187}}{R_{190}} = -5.33V + 4.87 \cdot V_{SET-\_USR} \quad (61)$$

Where:

$$V_{FB} = 1.235V\ typical \quad (62)$$

IC43 (Figure 1) generates the setting voltages in the range:

$$0 < V_{SET+\_USR}, V_{SET-\_USR} < 1.2V \quad (63)$$

Which would allow output voltages to be set in the ranges:

$$-0.51V \leq V_{OUT+USR} < 5.33V \quad (64)$$
$$0.51V \geq V_{OUT+USR} > -5.33V \quad (65)$$

The margins allow for compensating the components' tolerances. After calibration, the WaveForms SW only allows the ranges 0 to +/-5V respectively. Even so, output voltages below absolute value of 0.5V are not guaranteed. With light loads, such voltages might exhibit significant ripple (~15mV).

Each supply can be disabled by the FPGA.

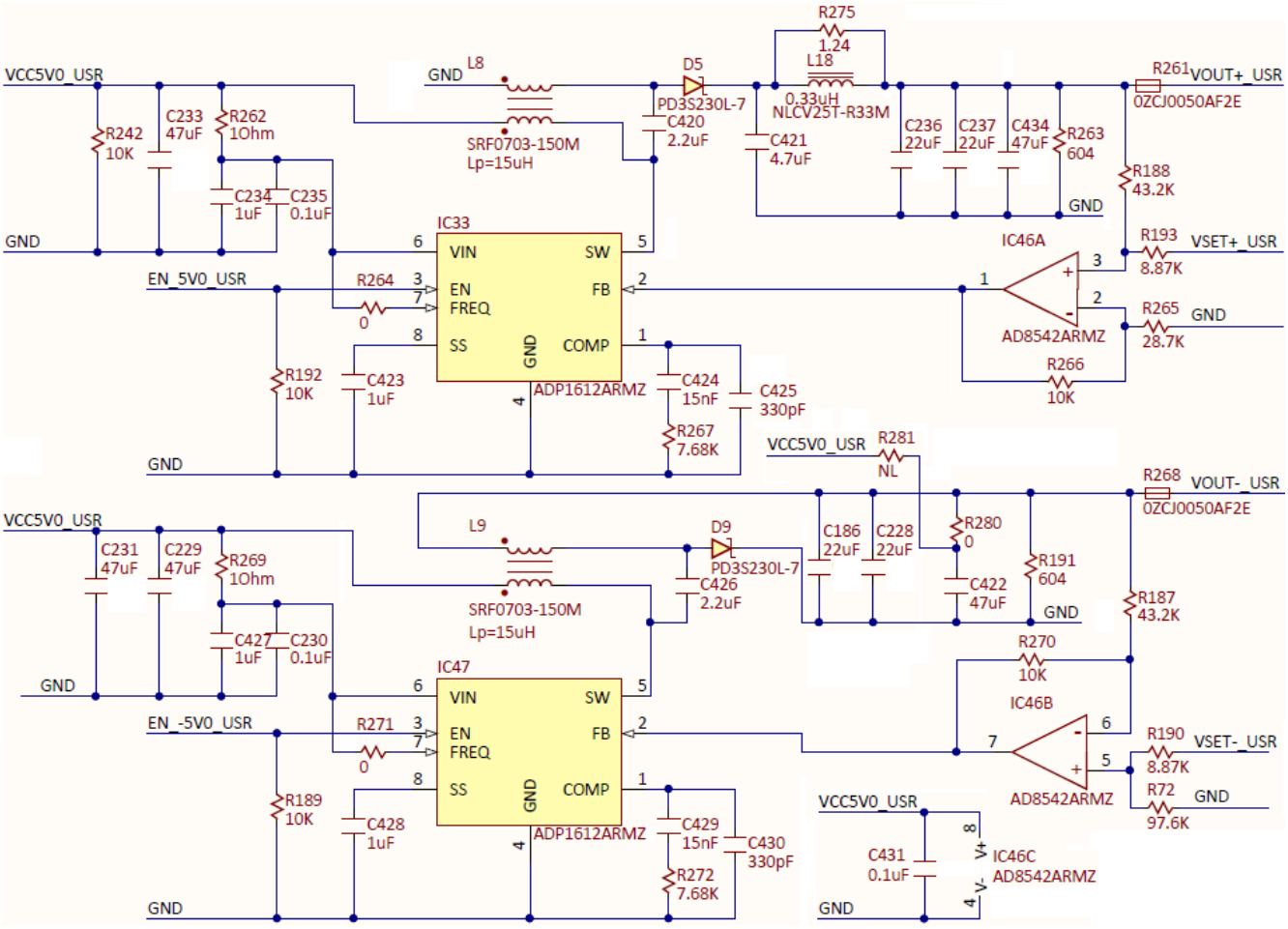

Figure 26. User power supplies.

6.5 Internal Power Supplies

6.5.1 Analog Supplies

Analog supplies need to have very low ripple to prevent noise from coupling into analog signals. Ferrite beads are used to filter the remaining switching noise and to separate the power supplies that go to the main analog circuit blocks, to avoid crosstalk.

The 3.3V (Figure 27) and 1.8V (Figure 28) analog power supplies are implemented around an ADP2138 Fixed Output Voltage, 800mA, 3MHz, Step-Down DC-to-DC converter. To insure low output voltage ripple a second, LC filter is added and forced PWM mode is selected.

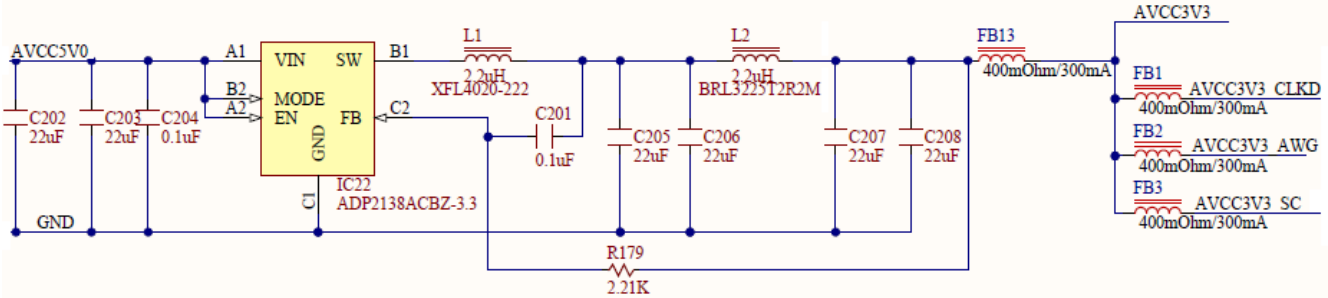

Figure 27. 3.3V internal analog power supply.

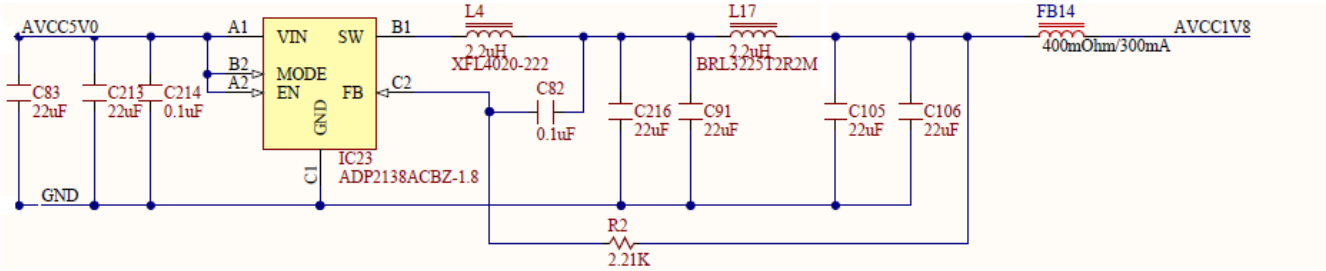

Figure 28. 1.8V internal analog power supply.

- Input voltage: 2.3 V to 5.5 V
- Peak efficiency: 95%
- 3 MHz fixed frequency operation
- 6-lead, 1 mm × 1.5 mm WLCSP package
- Fast load and line transient response
- 100% duty cycle low dropout mode
- Internal synchronous rectifier, compensation, and soft start
- Current overload and thermal shutdown protections
- Forced PWM and automatic PWM/PSM modes

The -3.3V analog power supply (Figure 29) is implemented with the ADP2301 Step-Down regulator in an inverting Buck-Boost configuration. See application Note AN-1083: Designing an Inverting Buck Boost Using the ADP2300 and ADP2301. The ADP2301 features:

- 1.2 A maximum load current
- ±2% output accuracy over temperature range
- 1.4 MHz switching frequency
- High efficiency up to 91%
- Current-mode control architecture
- Output voltage from 0.8 V to 0.85 × VIN
- Automatic PFM/PWM mode switching
- Integrated high-side MOSFET and bootstrap diode,
- Internal compensation and soft start
- Undervoltage lockout (UVLO), Overcurrent protection (OCP) and thermal shutdown (TSD)
- Available in ultrasmall, 6-lead TSOT package

The Output voltage is set with an external resistor divider from Vout to FB:

$$\frac{R_{180}}{R_{181}} = \frac{-V_{out} - V_{ref}}{V_{ref}} \quad (66)$$

Choosing $R_{181} = 10.2k\Omega$:

$$R_{180} = \frac{3.3V - 0.8V}{0.8V} \cdot 10.2k\Omega = 31.87\text{k}\Omega \quad (67)$$

Closest standard value is $R_{180} = 31.6k\Omega$

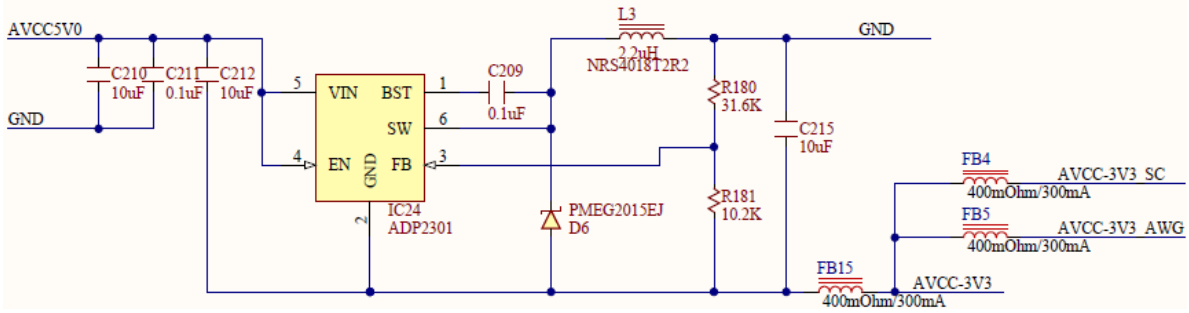

Figure 29. 3.3V internal analog power supply.

The 5.5V and -5.5V supplies (Figure 31) are created with a Sepic-Cuk topology, built around a single ADP1612 Step-Up DC-to DC converter. Both Sepic and Cuk converters are connected to the same switching pin of the regulator. Only the positive Sepic output is regulated, while the negative output tracks the positive one. This is an accepted behavior, since similar load currents are expected on both positive and negative rails.

The output current in a Sepic is discontinuous which results in a higher output ripple. To lower this ripple an additional output filter is added to the positive rail.

For more information see application note: AN-1106: An Improved Topology for Creating Split Rails from a Single Input Voltage.

Setting the Output Voltage:

$$\frac{R_{184}}{R_{185}} = \frac{V_{out} - V_{ref}}{V_{ref}} \quad (68)$$

Choosing $R_{185} = 13.7k\Omega$:

$$R_{184} = \frac{5.5V - 1.235V}{1.235V} \cdot 13.7k\Omega = 47.31\text{k}\Omega \quad (69)$$

Closest standard value is $R_{184} = 47.5k\Omega$

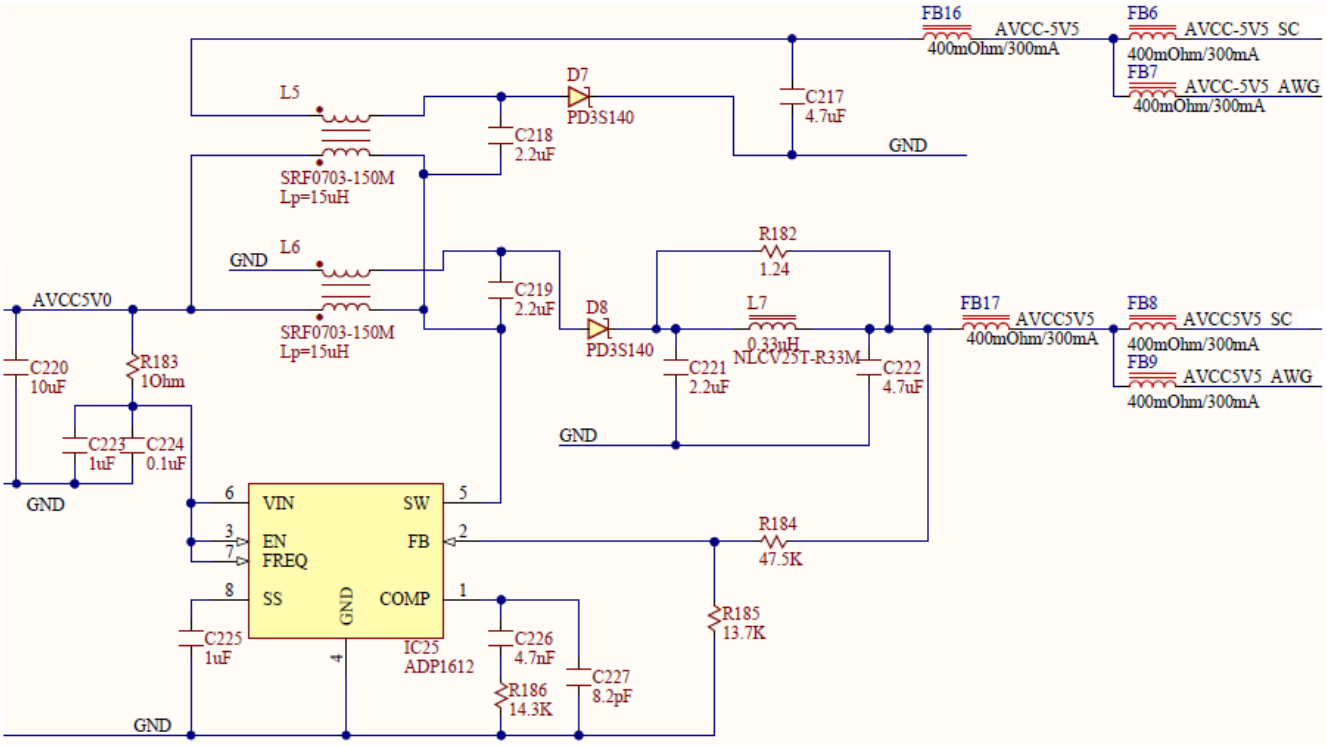

Figure 31. ±5.5V internal analog supplies.

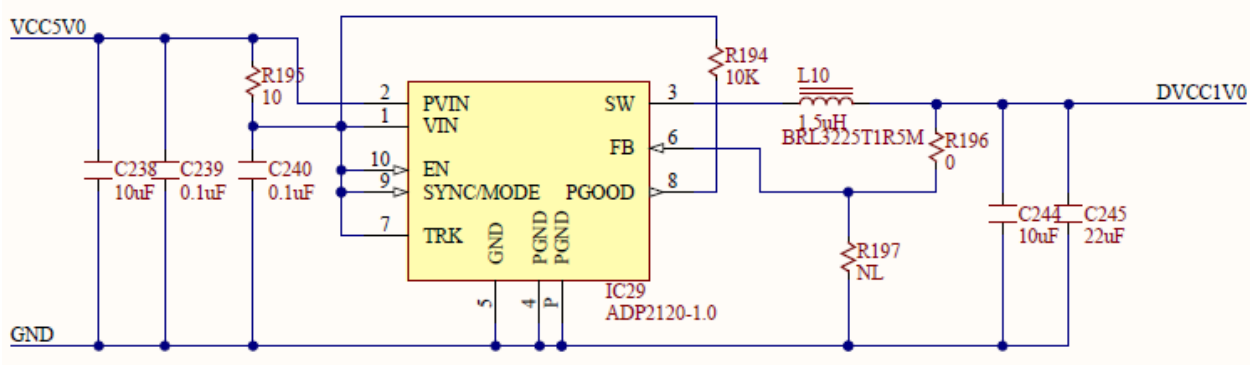

Figure 32. 1V internal digital supply.

6.5.2 Digital Supplies

The 1V digital supply (Figure 321) is implemented with the ADP2120-1. It has a fixed 1V output voltage option and a ±1.5% output accuracy which makes it suitable for the FPGA internal power supply. It also features:

- 1.25A continuous output current
- 145 mΩ and 70 mΩ integrated MOSFETs
- Input voltage range from 2.3 V to 5.5 V; output voltage from 0.6 V to VIN
- 1.2 MHz fixed switching frequency; Selectable PWM or PFM mode operation
- Current mode architecture
- Integrated soft start; Internal compensation
- UVLO, OVP, OCP, and thermal shutdown
- 10-lead, 3 mm × 3 mm LFCSP_WD package

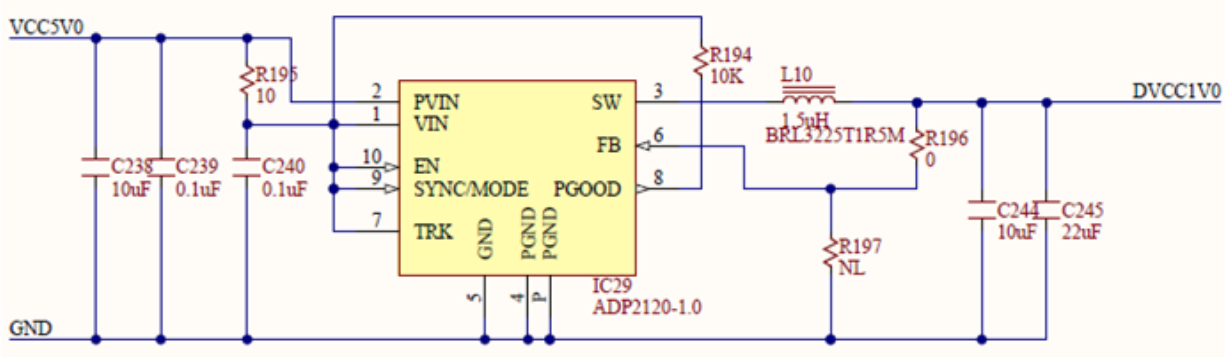

Figure 31. 1V internal digital supply.

The 3.3V digital supply (Figure 32) uses ADP2503-3.3 600mA, 2.5MHz Buck-Boost DC-to-DC Converter:

- Seamless transition between modes
- 38 µA typical quiescent current
- 2.5 MHz operation enables 1.5 µH inductor
- Input voltage: 2.3 V to 5.5 V;
- Fixed output voltage: 3.3 V
- Forced fixed frequency
- Internal compensation
- Soft start
- Enable/shutdown logic input
- Overtemperature protection
- Short-circuit protection
- Reverse current capability
- Undervoltage lockout protection
- Small 10-lead 3 mm × 3 mm package, 1 mm height profile
- Compact PCB footprint

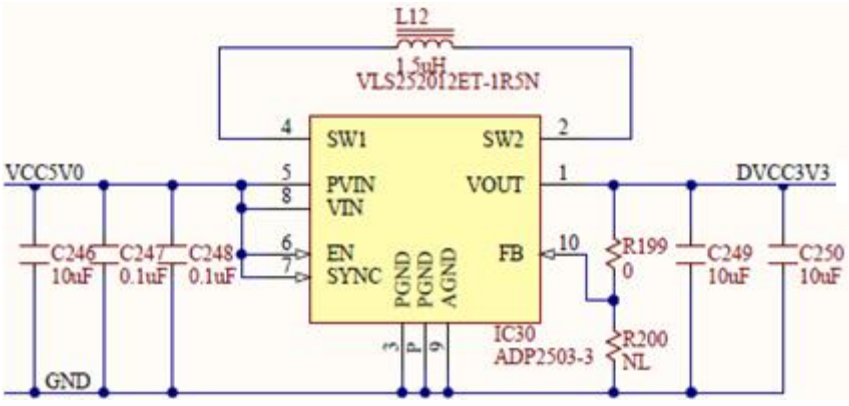

Figure 32. 3.3V internal digital supply.

The main requirement for the 3.3V digital supply is the reverse current capability. When a user pin is overdriven the protection diode opens and back powers circuitry connected to this supply. If the back powered energy is higher than the used energy the regulator delivers it to its input, preventing the 3.3V from rising.

The 1.8V digital power supply (Figure 33) is implemented with ADP2138-1.8 Fixed Output Voltage, 800mA, 3MHz, Step-Down DC-to-DC converter. This ensures a very small solution size due to the 3MHz switching frequency and the 1mm × 1.5 mm WLCSP package.

The ADP2138 also features:

- Input voltage: 2.3 V to 5.5 V
- Peak efficiency: 95%
- Typical quiescent current: 24 µA
- Fast load and line transient response
- 100% duty cycle low dropout mode
- Internal synchronous rectifier, compensation, and soft start
- Current overload and thermal shutdown protections
- Ultralow shutdown current: 0.2 µA (typical)
- Forced PWM and automatic PWM/PSM modes

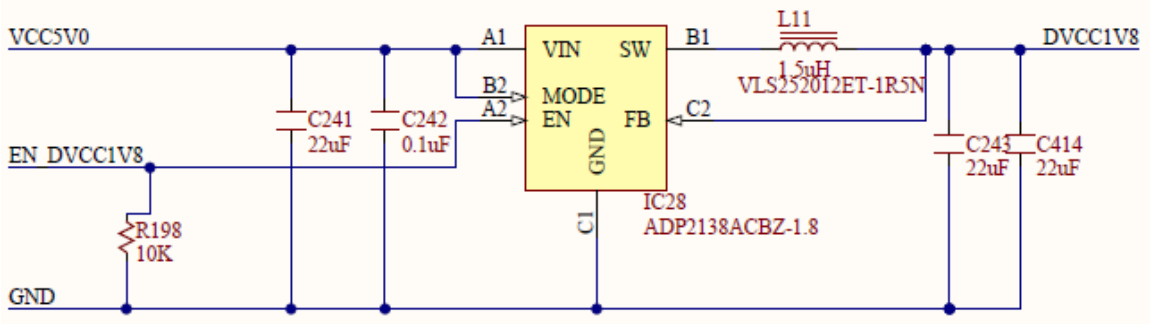

Figure 33. 1.8V internal digital supply.

6.6 Temperature Measurement

The Analog Discovery 2 uses the AD7415 Digital Output Temperature Sensor (Figure 24). AD7415 main features are:

- 10-bit temperature-to-digital converter
- Temperature range: −40°C to +125°C
- Typical accuracy of ±0.5°C at +40°C
- SMBus/I²C®-compatible serial interface
- Temperature conversion time: 29µs (typical)
- Space-saving 5-lead SOT-23 package
- Pin selectable addressing via AS pin

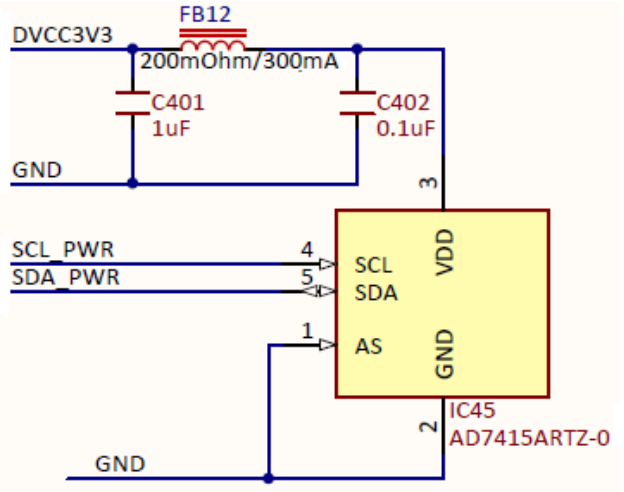

Figure 2. Temperature measurement.

7 USB Controller

The USB interface performs two tasks:

- **Programming the FPGA**: There is no non-volatile FPGA configuration memory on the Analog Discovery 2. The WaveForms software identifies the connected device and downloads an appropriate .bit file at power-up via a Digilent USB-JTAG interface. Adept run-time is used for low-level protocols.
- **Data exchange**: All instrument configuration data, acquired data and status information is handled via a Digilent synchronous parallel bus and USB interface. Speed up to 20MB/sec. is reached, depending on USB port type and load as well as PC performance.

8 FPGA

The core of the Analog Discovery 2 is the Xilinx the Spartan-6 FPGA circuit XC6SLX16-1L. The configured logic performs:

- Clock management (12 MHz and 60 MHz for USB communication, 100 MHz for data sampling)
- Acquisition control and Data Storage (Scope and Logic Analyzer)
- Analog Signal synthesis (look-up tables, AM/FM modulation for AWG)
- Digital signal synthesis (for pattern generator)
- Trigger system (trigger detection and distribution for all instruments)
- Power supplies control and instruments enabling
- Power and temperature monitoring
- Calibration memory control
- Communication with the PC (settings, status data)

Block and Distributed RAM of the FPGA are used for signal synthesis and acquisition. Multiple configuration files are available through the WaveForms software to allocate the RAM resources according to the application.

A detail of the trigger system is shown in Figure 35. Each instrument generates a trigger signal when a trigger condition is met. Each trigger signal (including external triggers) can trigger any instrument and drive the external trigger outputs. This way, all the instruments can synchronize to each other.

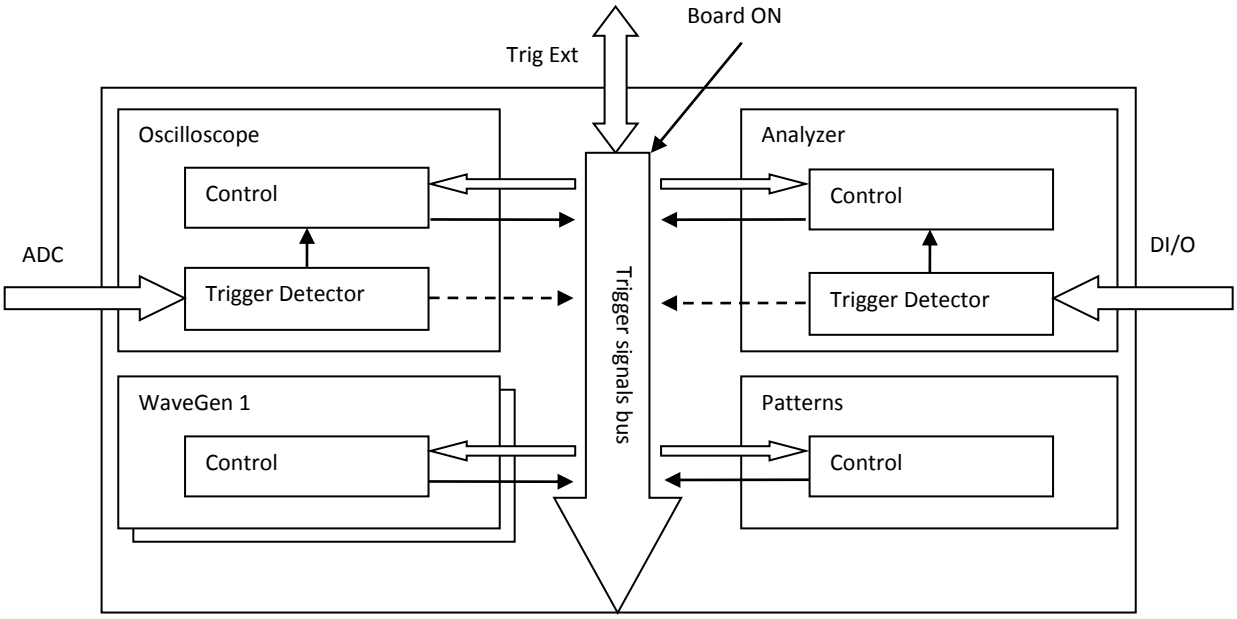

Figure 35. FPGA configuration trigger block diagram.

9 Features and Performances

This sections shows the features and performances as described in the Analog Discovery 2 datasheet. Footnotes add detailed information and annotate the HW description in this manual.

9.1 Analog Inputs (Scope)

- Two fully differential channels[viii]; 14-bit converters; 100 MSPS real-time sample rate
- 500uV to 5V/division[ix]; 1MΩ, 24pF inputs with 5 MHz analog bandwidth[x]
- Input voltages up to ±25V on each input (±50V differential); protected to ±50V[xi]
- Up to 16k samples/channel buffer length[xii]
- Advanced triggering modes (edge, pulse, transition types, hysteresis, etc.)[xiii]
- Trigger in/trigger out allows multiple instruments to be linked[xiv]
- Cross-triggering with Logic Analyzer, Waveform Generator, Pattern Generator or external trigger[xv]
- Selectable channel sampling mode (average, decimate, min/max)[xvi]
- Mixed signal visualization (analog and digital signals share same view pane)[xvii]
- Real-time FFTs, XY plots, Histograms and other functions always available[xviii]
- Multiple math channels support complex functions[xix]
- Cursors with advanced data measurements available on all channels[xx]
- All captured data files can be exported in standard formats[xxi]
- Scope configurations can be saved, exported and imported[xxii]

9.2 Analog Outputs (Arbitrary Waveform Generator)

- Two channels; 14-bit converters; 100 MSPS real-time sample rate[xxiii]
- Single-ended waveforms with offset control and up to ±5 V amplitude[xxiv]

- 5 MHz analog bandwidth[31] and up to 16k samples/channel[xxv]
- Easily defined standard waveforms (sine, triangle, sawtooth, etc.)
- Easily defined sweeps, envelopes, AM and FM modulation[xxvi]
- User-defined arbitrary waveforms can be defined within WaveForms software user interface or using standard tools (e.g. Excel)[xxvii]
- Cross-triggering between Analog input channels, Logic Analyzer, Pattern Generator or external trigger[xxviii]

9.3 Logic Analyzer

- 16 signals shared between analyzer, pattern generator, and discrete I/O[xxix]
- 100 MSPS, with buffers supporting up to 16K transitions per pin[xxx]
- LVCMOS (3.3V) logic level inputs
- Multiple trigger options including pin change, bus pattern, etc[xxxi]
- Trigger in/trigger out allows multiple instruments to be linked[xxxii]
- Cross-triggering between Analog input channels, Logic Analyzer, Pattern Generator or external trigger[xxxiii]
- Interpreter for SPI, I2C, UART, Parallel bus[xxxiv]
- Captured signals can be saved and exported in standard file formats[xxxv]

9.4 Digital Pattern Generator

- 16 signals shared between analyzer, pattern generator, and discrete I/O[xxxvi]
- 100 MSPS
- Algorithmic pattern generator (no memory buffers used)[xxxvii]
- Custom pattern editor with buffers supporting up to 16K transitions per pin[xxxviii]
- 3.3V outputs
- Data file import/export using standard formats[xxxix]
- Customized visualization options for signals and busses[xl]

9.5 Digital I/O

- 16 signals shared between analyzer, pattern generator, and discrete I/O[xli]
- LVCMOS (3.3 V) logic level inputs and outputs
- PC-based virtual I/O devices (buttons, switches & displays) drive physical pins[xlii]
- Customized visualization options available[xliii]

9.6 Power Supplies

- Two fixed power supplies derive power from USB port
- +5V up to 50mA and -5V up to 50mA (100mA total)

9.7 Network Analyzer[xliv]

- Waveform generator drives circuits with swept sine waves up to 10 MHz
- Input waveforms settable from 1 Hz to 10 MHz, with 5 to 1000 steps[xlv]
- Settable input amplitude and offset
- Analog input records response at each frequency[xlvi]
- Response magnitude and phase delay displayed in Bode, Nichols, or Nyquist formats[xlvii]

9.8 Voltmeters[xlviii]

- Two independent meters (shared with Analog input channels)
- Automatic measurements include DC, AC RMS and True RMS values[xlix]
- Single-ended and differential measurement capability
- Up to ±25V on each pin (±50V max peak-peak)
- Auto-range feature selects best gain range[l]

9.9 Spectrum Analyzer[li]

- Performs FFT or CZT algorithm on analog input channels and displays power spectrum[lii]
- Frequency range adjustments in center/span or start/stop modes[liii]
- Linear or logarithmic frequency scale[liv]
- Peak tracking option finds peak power and adjusts display to keep peak in center of display[lv]
- Vertical axis supports voltage-peak, voltage-RMS, dBV and dBu display options[lvi]
- Windowing options include rectangular, triangular, hamming, Cosine, and many others[lvii]
- Cursors and automatic measurements including noise floor, SFDR, SNR, THD and many others[lviii]
- Data file import/export using standard formats[lix]

9.10 Other Features

- USB powered; all needed cables included
- High-speed USB2 interface for fast data transfer
- Waveform Generator output can be played on stereo audio jack
- Two external trigger pins can link triggers across multiple devices[lx]
- Cross triggering between instruments[lxi]
- Help screens, including contextual help[lxii]
- New! Supported by MATLAB and the MATLAB student edition
- Instruments and workspaces can be individually configured; configurations can be exported[lxiii]

[i] These 16 digital lines are shared by the Logic Analyzer, Pattern Generator and Digital I/O. They are always inputs, some of them can be set to be outputs also. Digital I/O has precedence in case of output conflict with the Pattern Generator.
[ii] When inputs, these lines can be set to be 1.8V CMOS compatible.
[iii] These 16 digital lines are shared by the Logic Analyzer, Pattern Generator and Digital I/O. They are always inputs, some of them can be set to be outputs also. Digital I/O has precedence in case of output conflict with the Pattern Generator.
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[vi] When inputs, these lines can be set to be 1.8V CMOS compatible.
[vii] When inputs, these lines can be set to be 1.8V CMOS compatible.
[viii] See the Note in Scope
[ix] High-gain or low-gain is used in the analog signal input path for rough scaling. “Digital Zooming” is used for multiple scope scales.
[x] The Scope bandwidth depends on probes. The Analog Discovery wire kit is an affordable, easy-to-use solution, but it limits the frequency, noise, and crosstalk performances. With a coax cable and Analog Discovery BNC adapter, the 0.5dB Scope bandwidth is 10 MHz (see Fig. 14).
[xi] As shown in Fig. 11, a ±50V differential input signal does not fit in a single scope screen (ADC range). However, Vertical Position setting allows visualization of either +50V or -50V levels.
[xii] Default Scope buffer size is 8kSamples/channel. The WaveForms Device Manager (WaveForms Main Window/Device/Manager) provides alternate FPGA configuration files, with different resource allocation. With no memory allocated to the Digital I/O and reduced memory assigned to the AWG, the scope buffer size can be chosen to be 16kSamples/channel.
[xiii] Trigger Detectors and Trigger Distribution Networks are implemented in the FPGA. This allows real time triggering and cross-triggering of different instruments within the Analog Discovery device. Using external Trigger inputs/outputs, cross-triggering between multiple Analog Discovery devices is possible.
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[xv] Trigger Detectors and Trigger Distribution Networks are implemented in the FPGA. This allows real time triggering and cross-triggering of different instruments within the Analog Discovery device. Using external Trigger inputs/outputs, cross-triggering between multiple Analog Discovery devices is possible.
[xvi] Real time sampling modes are implemented in the FPGA. The ADC always works at 100Msamples/sec. When a lower sampling rate is required, (108/N samples/sec), N ADC samples are used to build a single recorded sample, either by averaging or decimating. In the Min/Max mode, every 2N samples are used to calculate and store a pair of Min/Max values. The stored sample rate is reduced by half in Min/Max mode.
[xvii] In mixed signal mode, the scope and Digital I/O acquisition blocks use the same reference clock, for synchronization.
[xviii] This functionality is implemented by WaveForms software in the PC, using the buffered data from the FPGA. After acquiring a complete data buffer at the FPGA level and uploading it to the PC, the data is processed and displayed, while a new acquisition is started.
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[xxi] This functionality is implemented by WaveForms software, in the PC.
[xxii] This functionality is implemented by WaveForms software, in the PC.
[xxiii] The AWG DAC always works at 100Msamples/sec. When a lower sampling rate is required, (108/N samples/sec), each sample is sent N times to the DAC.
[xxiv] The AWG output voltage is limited to ±5V. This refers to the sum of AC signal and DC offset.
[xxv] Default AWG buffer size is 4kSamples/channel. The WaveForms Device Manager (WaveForms Main Window/Device/Manager) provides alternate FPGA configuration files, with different resources allocation. With no memory allocated to the Digital I/O and reduced memory assigned to the Scope, the AWG buffer size can be chosen to be 16kSamples/channel.
[xxvi] Real time implemented in the FPGA configuration.

[xxvii] This functionality is implemented by WaveForms software, in the PC.
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[xxix] All digital I/O pins are always available as inputs, to be acquired and displayed in the Logic Analyzer and Static I/O WaveForms instruments. The user selects which pins are also used as outputs, by the Pattern Generator or Static I/O instruments. When a signal is driven by both Pattern Generator and Static I/O instruments, the Static I/O instrument has priority, except if Static I/O attempts to drive a HiZ value.
[xxx] Default Logic Analyzer buffer size is 4kSamples/channel. The WaveForms Device Manager (WaveForms Main Window/Device/Manager) provides alternate FPGA configuration files, with different resource allocation. With no memory allocated to the Scope and AWG, the Logic Analyzer buffer size can be chosen to be 16kSamples/channel.
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[xxxvi] All digital I/O pins are always available as inputs, to be acquired and displayed in the Logic Analyzer and Static I/O WaveForms instruments. The user selects which pins are also used as outputs, by the Pattern Generator or Static I/O instruments. When a signal is driven by both Pattern Generator and Static I/O instruments, the Static I/O instrument has priority, except if Static I/O attempts to drive a HiZ value.
[xxxvii] Real time implemented in the FPGA configuration.
[xxxviii] Default Pattern Generator buffer size is 1kSamples/channel. The WaveForms Device Manager (WaveForms Main Window/Device/Manager) provides alternate FPGA configuration files, with different resources allocation. With no memory allocated to the Scope and AWG, the Pattern Generator buffer size can be chosen to be 16kSamples/channel.
[xxxix] This functionality is implemented by WaveForms software, in the PC.
[xl] This functionality is implemented by WaveForms software, in the PC.
[xli] All digital I/O pins are always available as inputs, to be acquired and displayed in the Logic Analyzer and Static I/O WaveForms instruments. The user selects which pins are also used as outputs, by the Pattern Generator or Static I/O instruments. When a signal is driven by both Pattern Generator and Static I/O instruments, the Static I/O instrument has priority, except if Static I/O attempts to drive a HiZ value.
[xlii] This functionality is implemented by WaveForms software, in the PC.
[xliii] This functionality is implemented by WaveForms software, in the PC.
[xliv] The Network Analyzer instrument in WaveForms uses Analog Outputs (AWG) channel1 and Analog Inputs (Scope) hardware resources. When it starts running, all other instruments using the same HW resources (competing instruments: AWG channel 1, Scope, Voltmeters, Spectrum Analyzer) are forced to a BUSY state. When running a competing instrument, the Network Analyzer is forced to a BUSY state
[xlv] This functionality is implemented by WaveForms software, in the PC.
[xlvi] This functionality is implemented by WaveForms software, in the PC.
[xlvii] This functionality is implemented by WaveForms software, in the PC.
[xlviii] The Voltmeter instrument in WaveForms uses Analog Inputs (Scope) Hardware resources competing with other WaveForms instruments (Scope, Network Analyzer, Spectrum Analyzer). When it starts running, the competing instruments are forced to a BUSY state. When running a competing instrument, the Voltmeter is forced in BUSY state.
[xlix] This functionality is implemented by WaveForms software, in the PC.
[l] This functionality is implemented by WaveForms software, in the PC.
[li] The Spectrum Analyzer instrument in WaveForms uses Analog Inputs (Scope) Hardware resources competing with other WaveForms instruments (Scope, Network Analyzer, Voltmeter). When it starts running, the competing instruments are forced to a BUSY state. When running a competing instrument, the Spectrum Analyzer is forced to a BUSY state.
[lii] This functionality is implemented by WaveForms software, in the PC.
[liii] This functionality is implemented by WaveForms software, in the PC.
[liv] This functionality is implemented by WaveForms software, in the PC.
[lv] This functionality is implemented by WaveForms software, in the PC.

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[lvii] This functionality is implemented by WaveForms software, in the PC.
[lviii] This functionality is implemented by WaveForms software, in the PC.
[lix] This functionality is implemented by WaveForms software, in the PC.
[lx] Trigger Detectors and Trigger Distribution Networks are implemented in the FPGA. This allows real time triggering and cross-triggering of different instruments within the Analog Discovery device. Using external Trigger inputs/outputs, cross-triggering between multiple Analog Discovery devices is possible.
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[lxii] This functionality is implemented by WaveForms software, in the PC.
[lxiii] This functionality is implemented by WaveForms software, in the PC.