Figure 7.29 Development of the ASM chart for the controller.
Figure 7.30 Block diagram of the multiplier.
Figure 7.32 Preliminary design of the multiplier circuit.
(b) Flowchart for the controller

Figure 7.32 (cont.)
MCAND

4-bit storage register with a synchronous LD input

MPLIER

Same as PRODHI register except that a CLR input is not required

PRODHI

4-bit shift-right register
SI = serial input
LD = synchronous load input
CLR = synchronous clear input
SHF = synchronous shift-right input

ADDER

S = A plus B
COUT = 0 if no overflow
= 1 if has overflow

COUNT

2-bit synchronous counter (CT = 3) with a synchronous clear input (CLR = true)

PRODLO

Same as PRODHI register except that an LD input is not required

CY

Gated D flip-flop: i.e., a 1-bit storage register with a synchronous LD input and a synchronous CLR input

Figure 7.33 Detailed specifications for the circuit elements.
Figure 7.34 Refined design of the multiplier circuit.
7.8 DESIGN EXAMPLES

(b) ASM chart for the controller

Figure 7.34 (cont.)
Figure 7.35  Refinement of the ASM chart for the controller.
Figure 7.36  Final design for the multiplier circuit.
(b) ASM chart for the controller

Figure 7.36 (cont.)
Figure 7.37 Realization of the circuit elements.

Where 0 = false
1 = true
X = don't care
State assignments:

\[ C_1 \quad C_0 \]

WTINIT 0 0
TSBIT 0 1
SHIFT 1 0

(a) Block diagram and state assignment

<table>
<thead>
<tr>
<th>present state</th>
<th>inputs</th>
<th>outputs</th>
<th>next state</th>
<th>flip-flop inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_1 \quad C_0 )</td>
<td>MPLIER.( Z_0 ) (CT = 3)</td>
<td>LDNUM</td>
<td>INITL</td>
<td>SHIFT</td>
</tr>
<tr>
<td>0 0 X X X 0</td>
<td>0 0 0 0 0 0 1</td>
<td>0 0 0 0 0 0 1</td>
<td>0 1</td>
<td>0 0</td>
</tr>
<tr>
<td>0 0 X X 1</td>
<td>0 0 0 0 0 1 0</td>
<td>0 0 0 0 0 0 1</td>
<td>0 1</td>
<td>0 1</td>
</tr>
<tr>
<td>0 1 0 X X</td>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 1</td>
<td>0 1</td>
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<tr>
<td>0 1 0 X X</td>
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<td>0 0 0 0 0 0 0</td>
<td>0 0</td>
<td>0 0</td>
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<tr>
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<td>0 0 0 0 0 0 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
</tbody>
</table>

Where 0 = false
1 = true
X = don't care

(b) Next-state and output table

Figure 7.38 Outline of the realization of the controller.