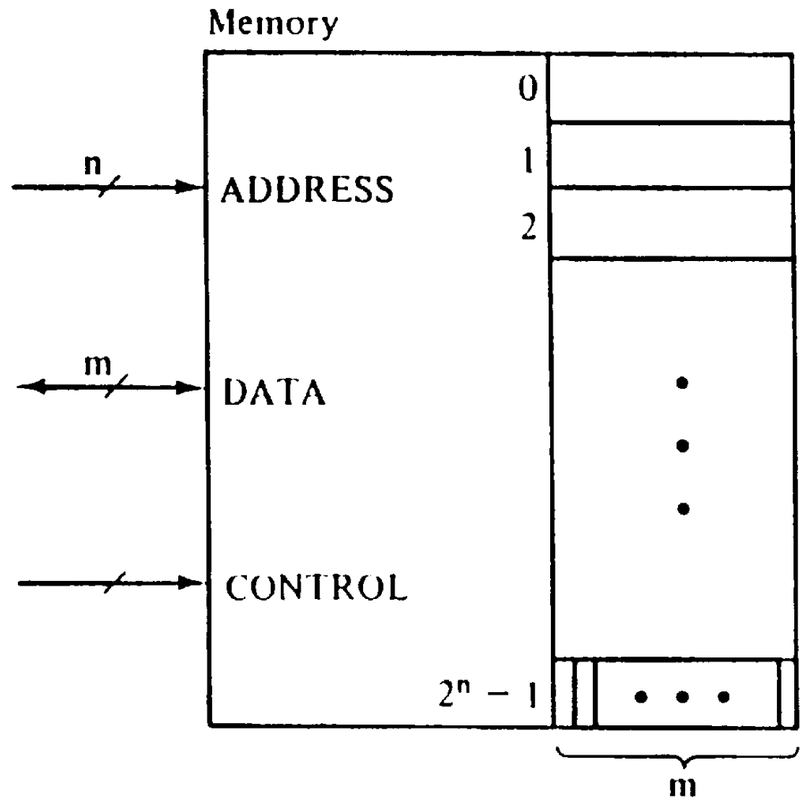
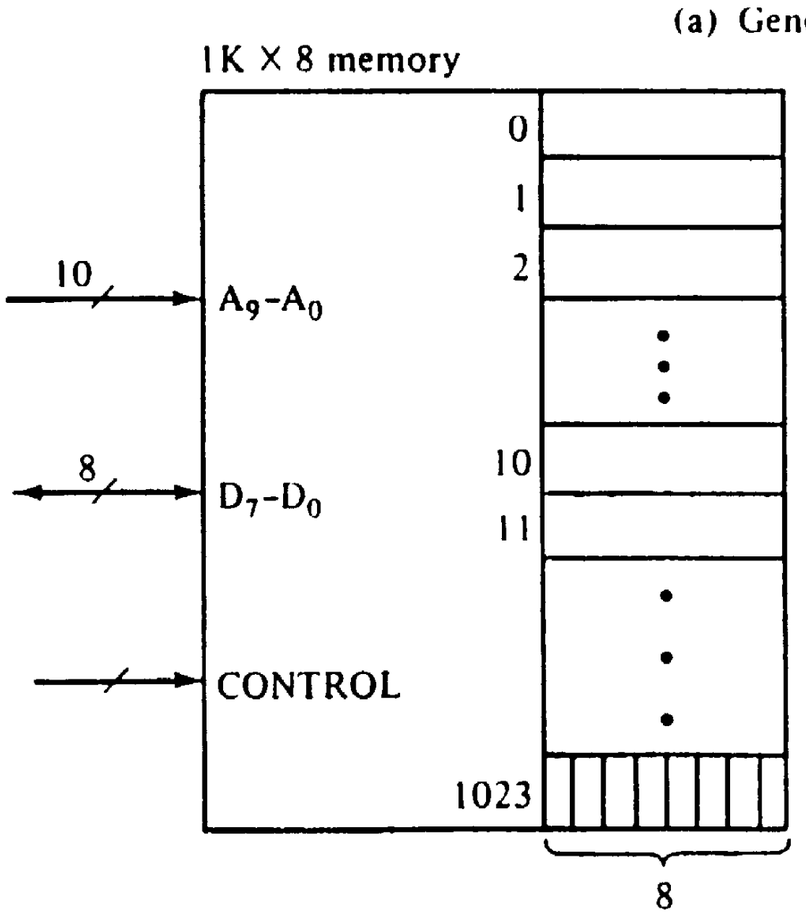
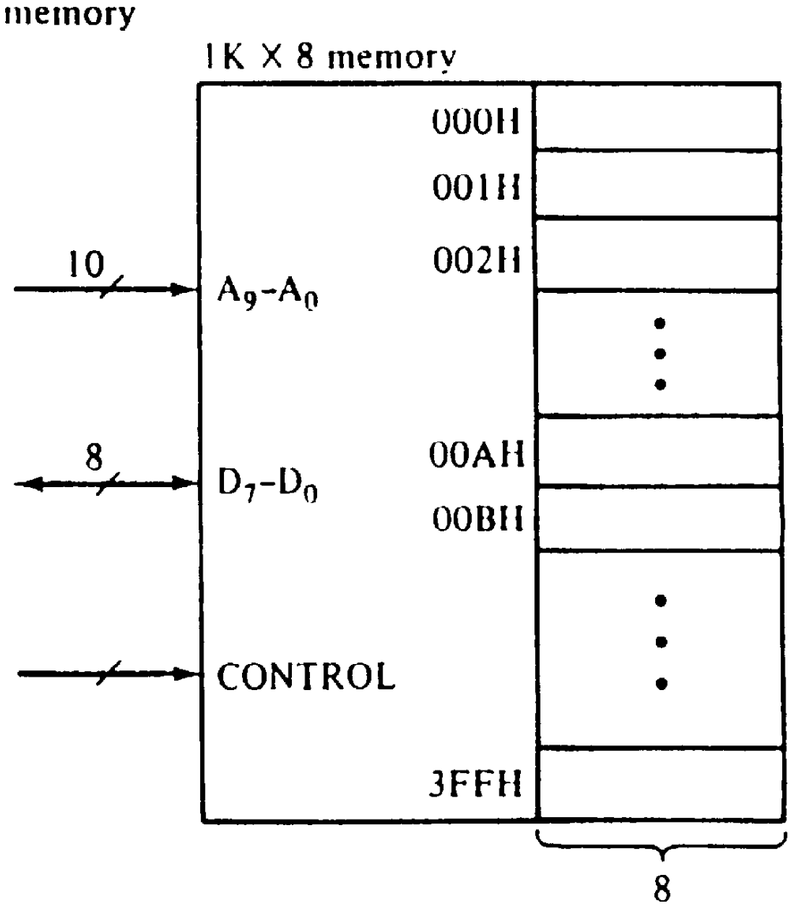


(a) General model of a memory

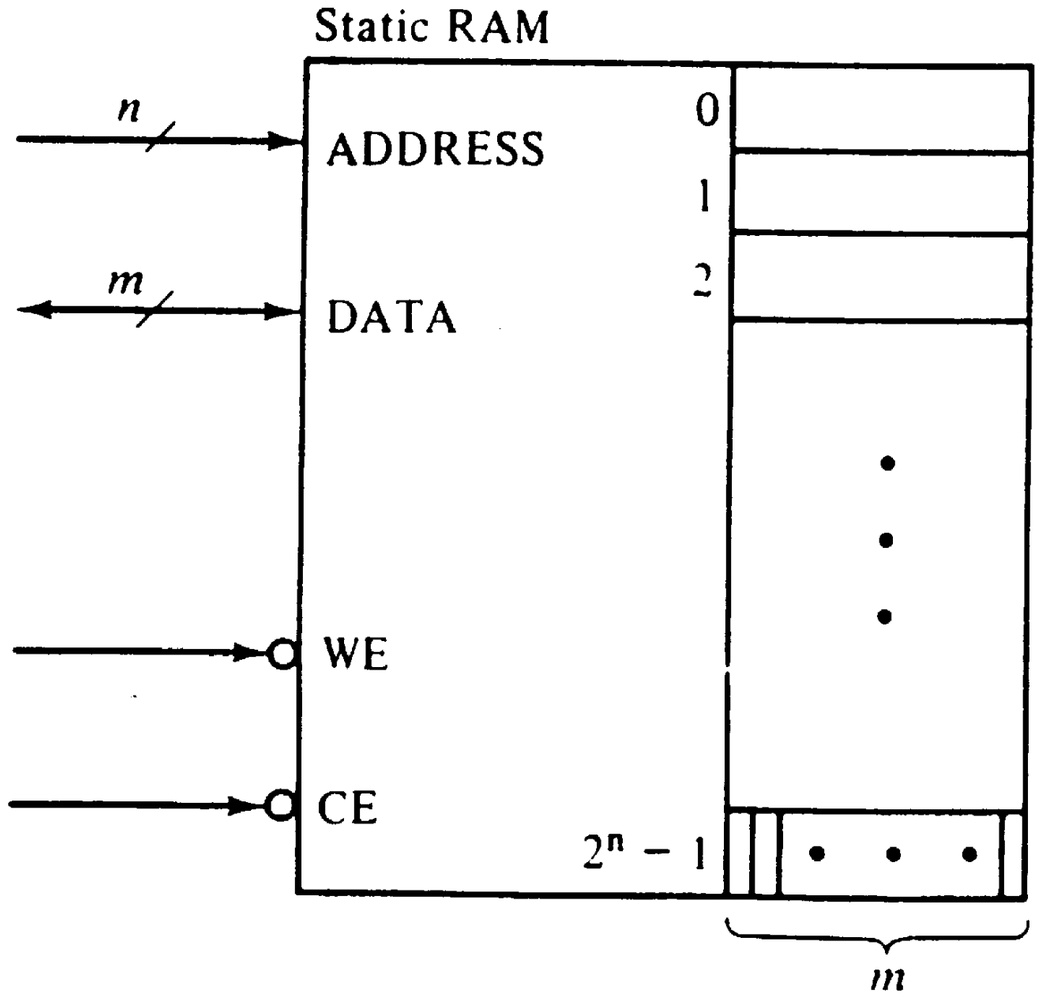


(b) 1K X 8 memory with addresses in decimal



(c) 1K X 8 memory with addresses in hexadecimal

Figure 6.21 Models of memories.



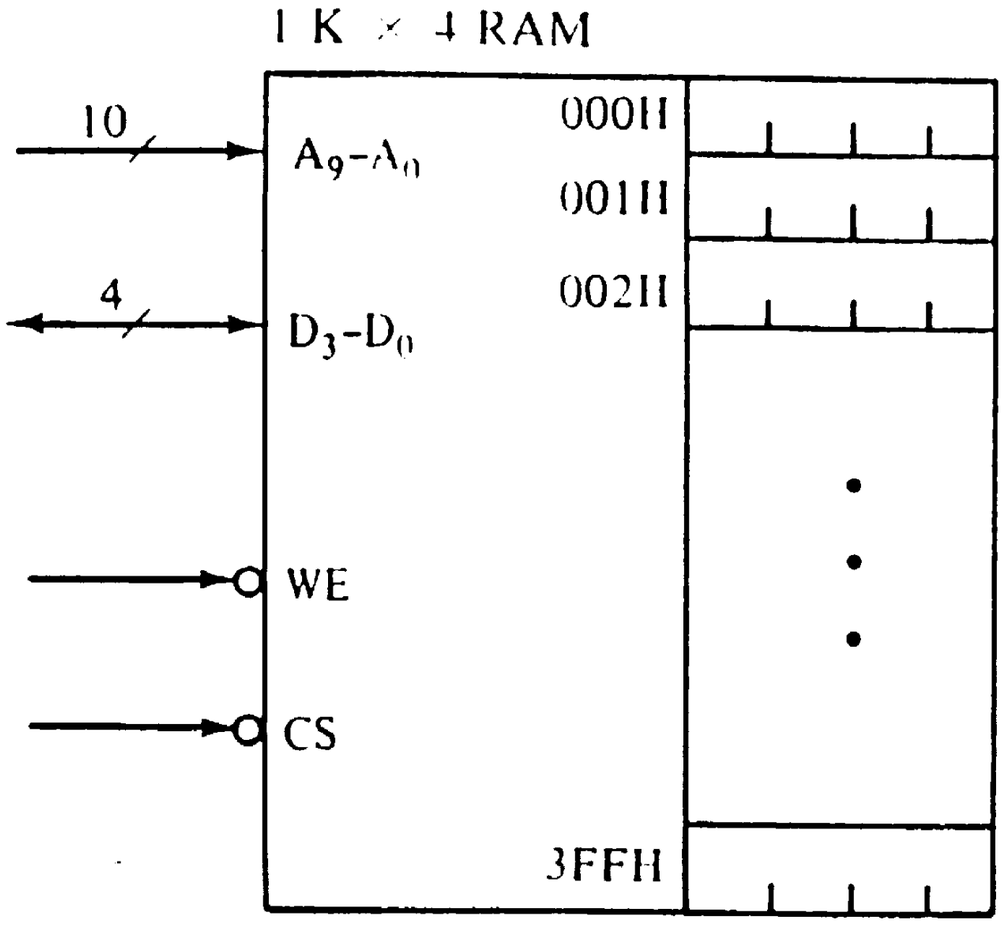
(a) A model of static RAM

Operation	CE	WE
Disable RAM	F(H)	X
Read	T(L)	F(H)
Write	T(L)	T(L)

Where F: false
T: true
X: don't care
L: low
H: high

(b) Operations

Figure 6.22 Static RAM.



(a) Block diagram

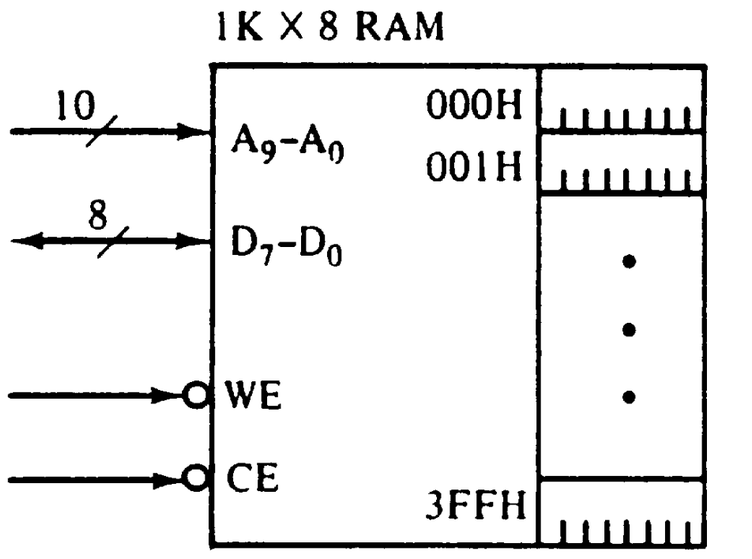
Operation	CS	WE
High-Z outputs	H	X
Read	L	H
Write	L	L

Where L: Low-voltage level
H: High-voltage level
X: Don't care

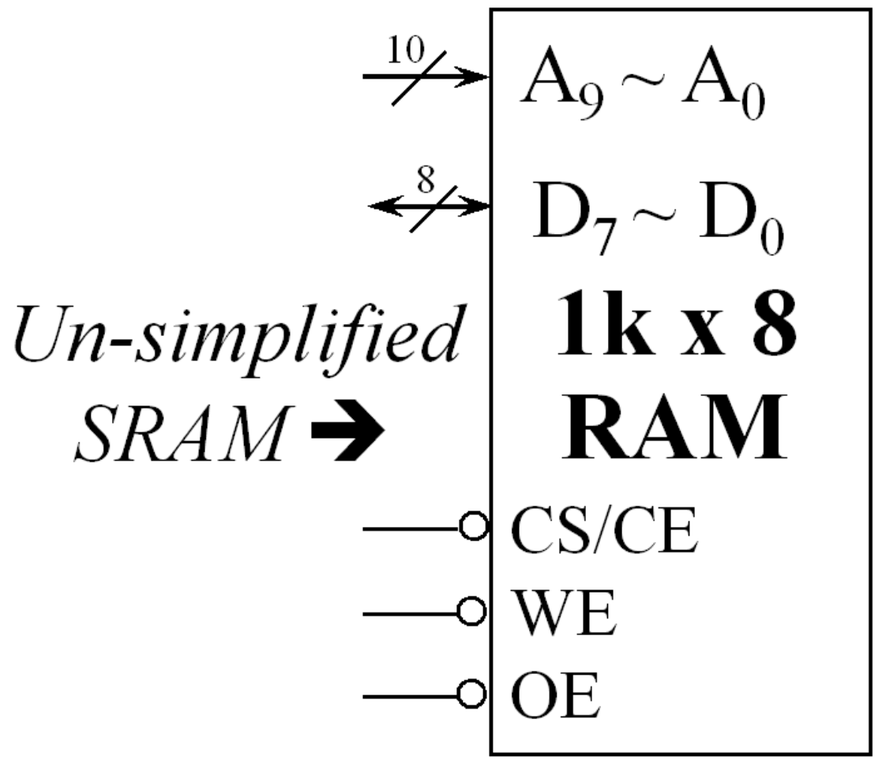
(b) Operations and control

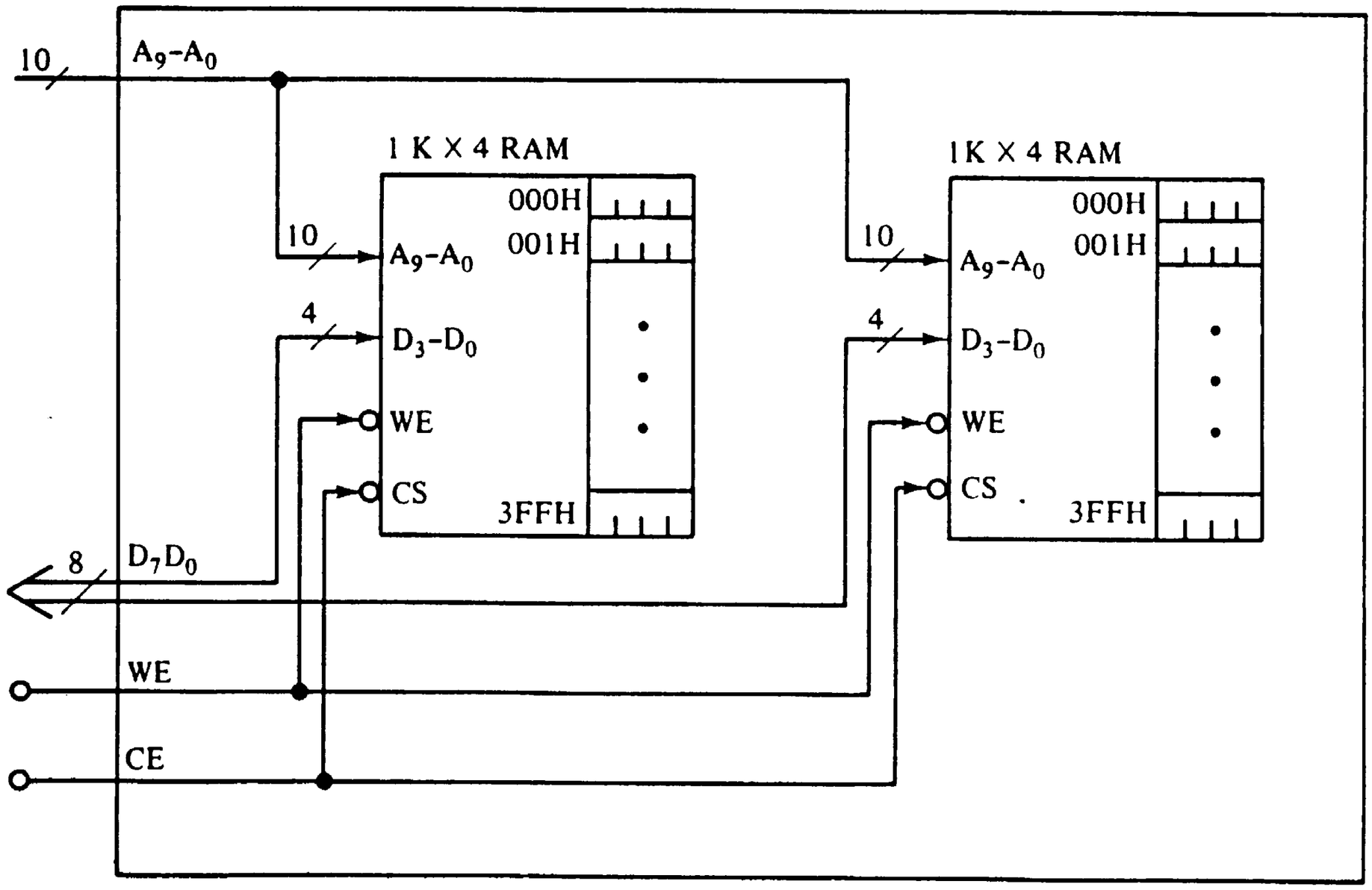
Figure 6.23 Typical commercially available 1K × 4 RAM.

- Sometimes block diagrams for SRAM are simplified, removing OE(L).
  - > Since WE(L) has higher priority than OE(L), OE(L) can be always true, i.e., GND.
  - > In this case, if WE is true, writing to SRAM; otherwise reading.



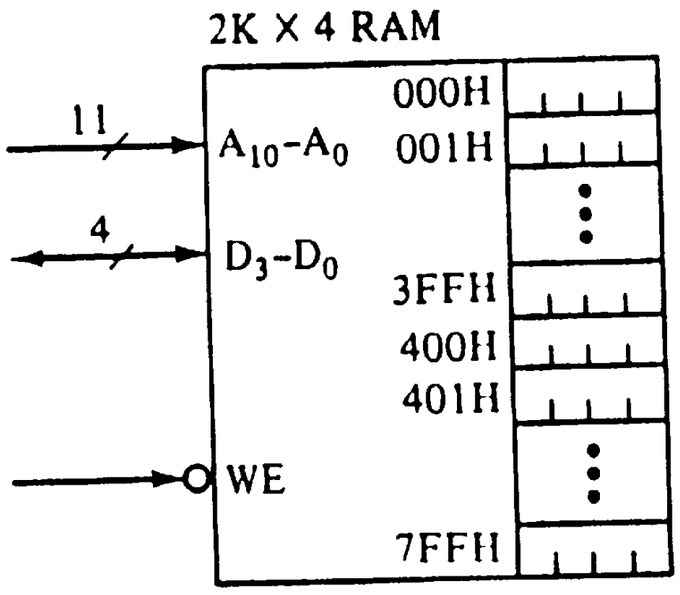
(a) Block diagram of a 1K X 8 RAM



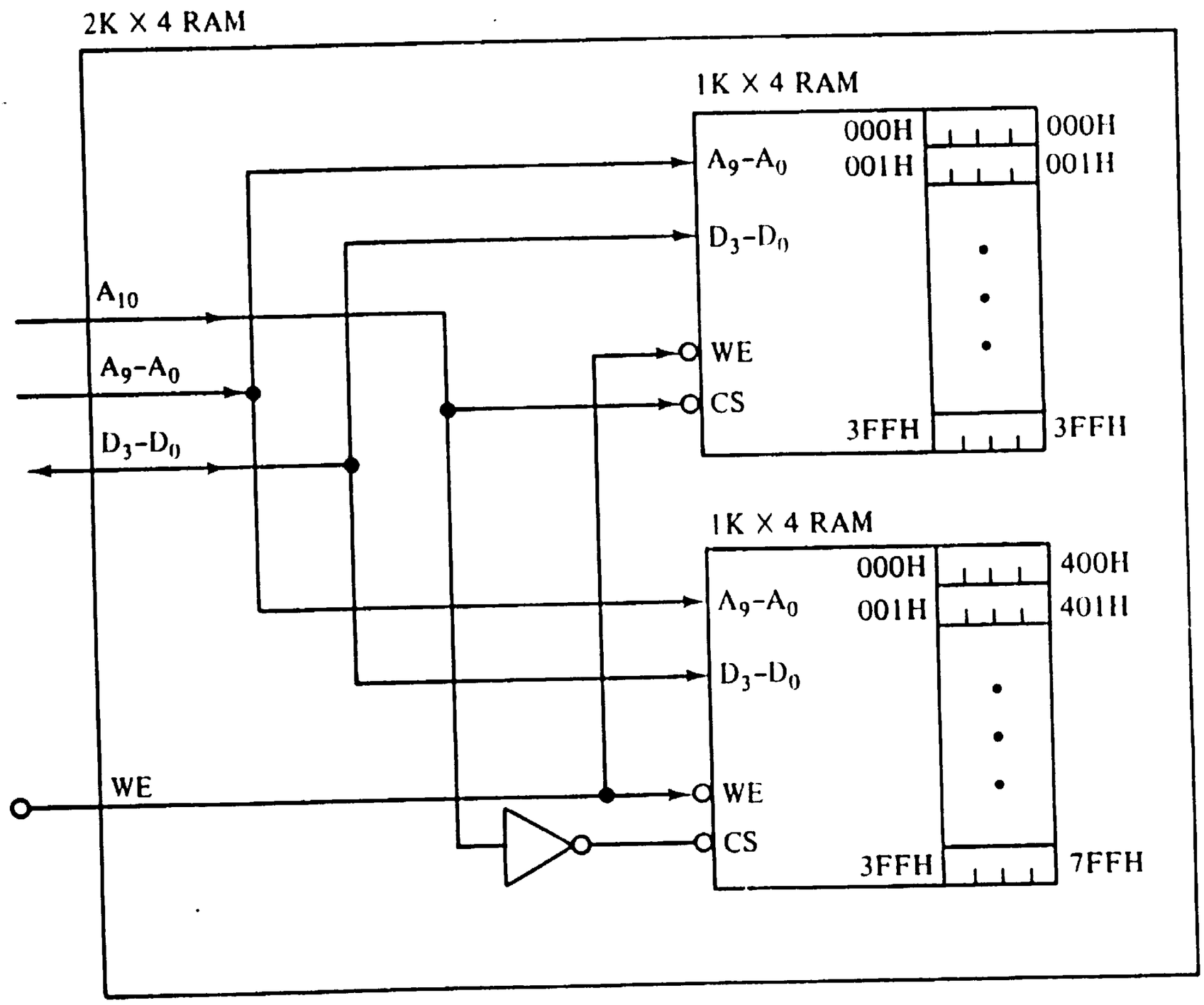


(b) Realization with two 1K X 4 RAMs

Figure 6.24 Realization of a 1K × 8 RAM.

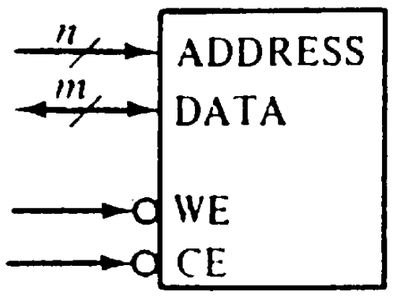


(a) Block diagram of a 2K X 4 RAM

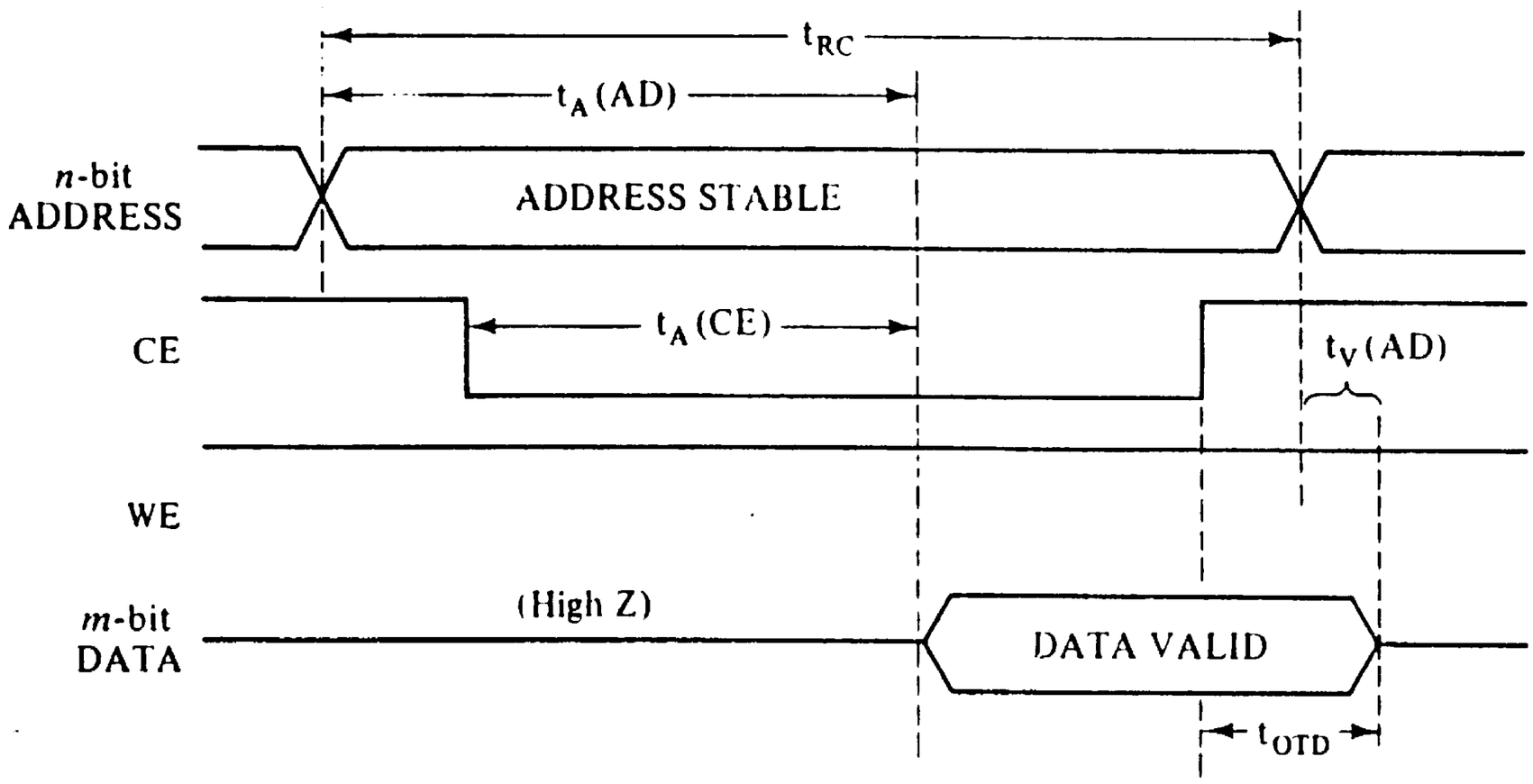


(b) Realization with two 1K X 4 RAMs

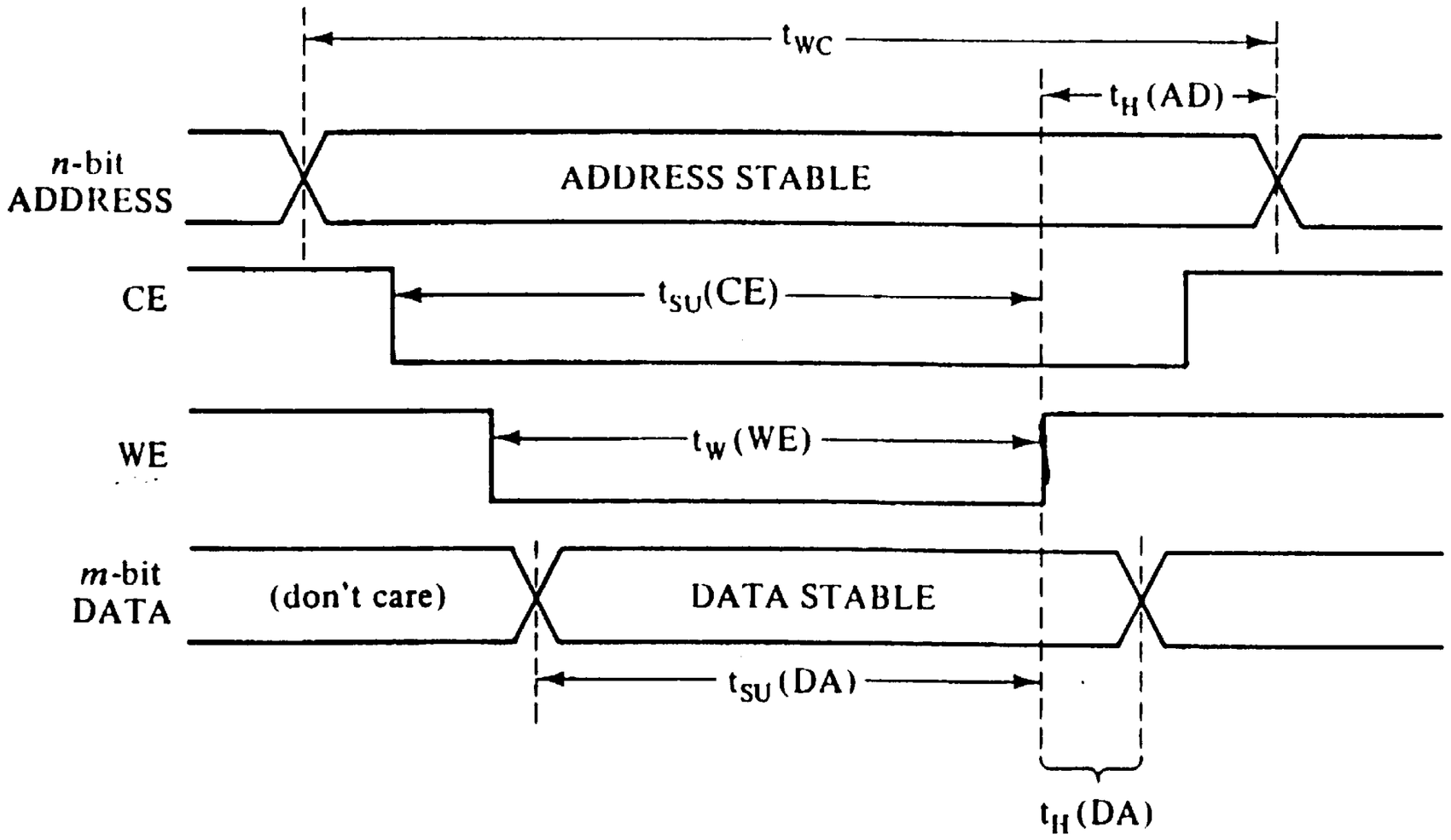
Figure 6.25 Realization of a 2K × 4 RAM.



(a) Block diagram of a RAM

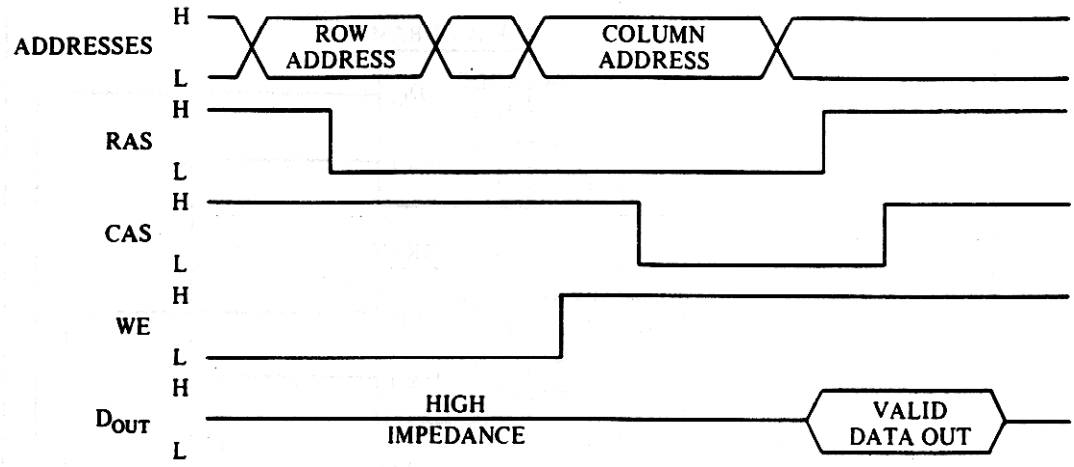


(b) Timing diagram for a memory read cycle

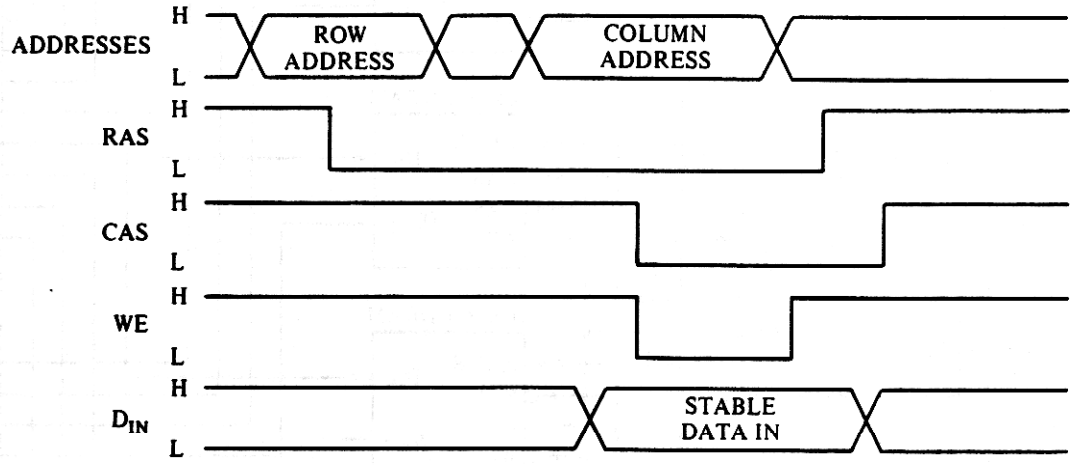


(c) Timing diagram for a memory write cycle

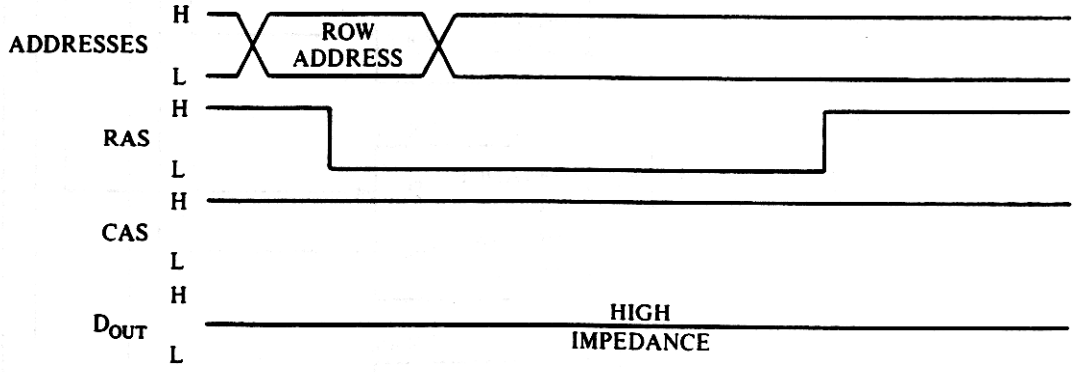
Figure 6.26 Memory read and memory write cycles.



(a) Read cycle

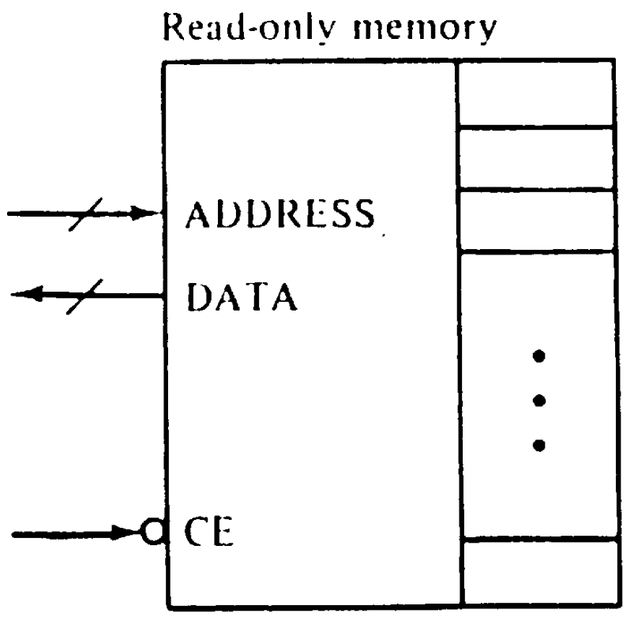


(b) Write cycle



(c) RAS-only refresh cycle

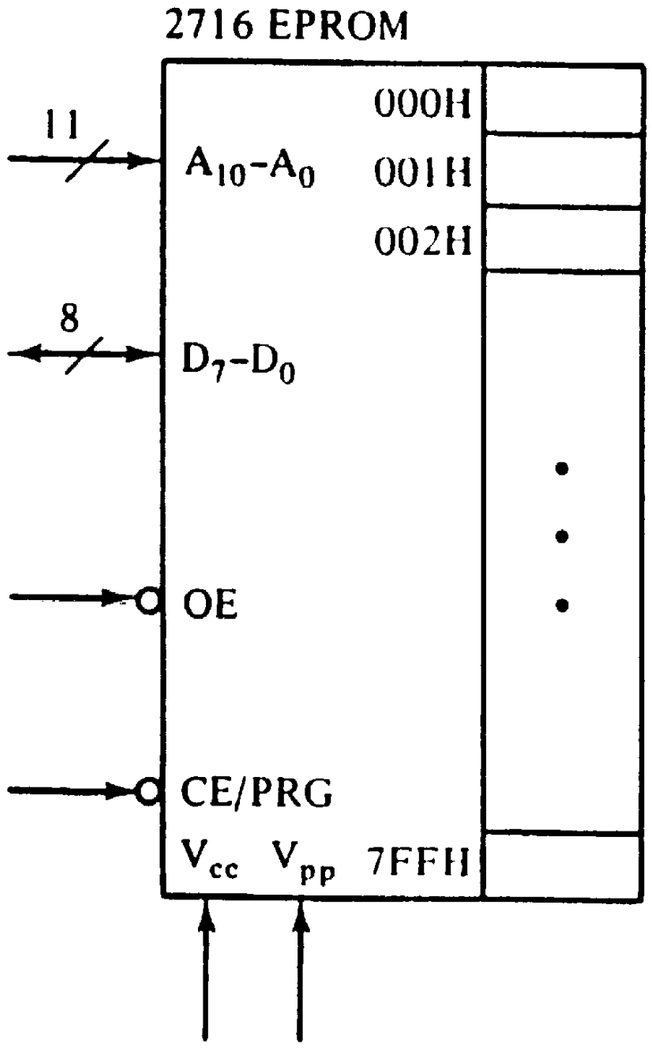
Figure 6.31 Basic operations for a dynamic RAM.



Operation	CE
Disable memory	0
Read	1

Where 0: false
1: true

Figure 6.27 A model of a read-only memory under normal operation.

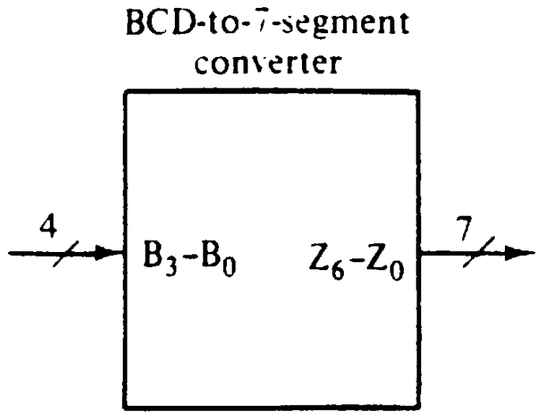


(a) Block diagram of the 2716 EPROM

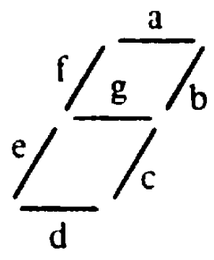
Operation	CE/PRG	OE	V_{pp}	V_{cc}	Outputs
Read	L	L	+5 V	+5 V	D_7-D_0 OUT
Standby	H	X	+5 V	+5 V	High Z
Program	Pulsed L → H	H	+25 V	+5 V	D_7-D_0 IN
Program verify	L	L	+25 V	+5 V	D_7-D_0 OUT
Program inhibit	L	H	+25 V	+5 V	High Z

(b) Table of operations

Figure 6.29 The 2716 EPROM.



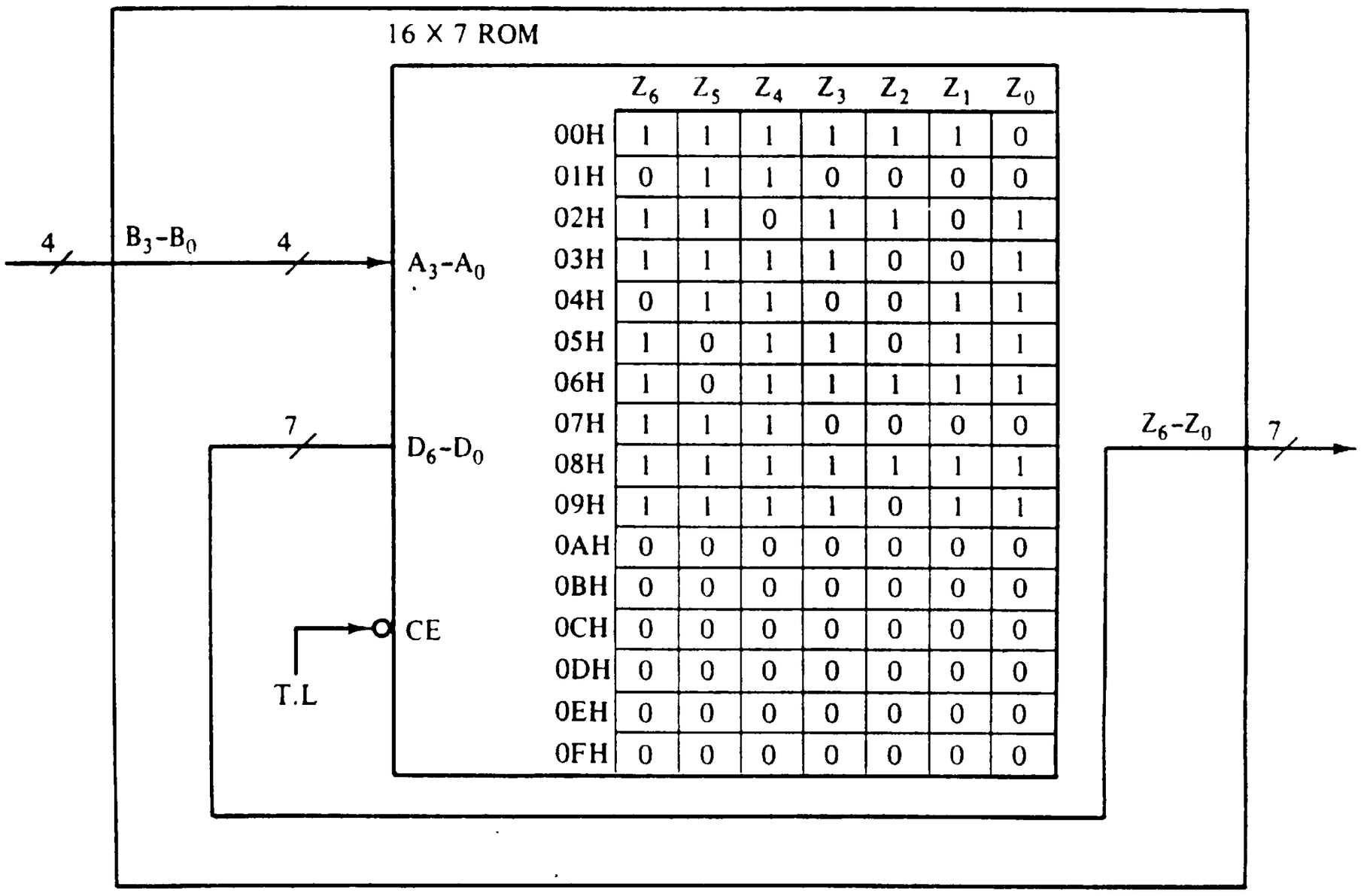
Where Z_6 = a
Z_5 = b
Z_4 = c
Z_3 = d
Z_2 = e
Z_1 = f
Z_0 = g



(a) Problem definition

B_3	B_2	B_1	B_0	(a) Z_6	(b) Z_5	(c) Z_4	(d) Z_3	(e) Z_2	(f) Z_1	(g) Z_0
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

(b) Truth table



	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0
00H	1	1	1	1	1	1	0
01H	0	1	1	0	0	0	0
02H	1	1	0	1	1	0	1
03H	1	1	1	1	0	0	1
04H	0	1	1	0	0	1	1
05H	1	0	1	1	0	1	1
06H	1	0	1	1	1	1	1
07H	1	1	1	0	0	0	0
08H	1	1	1	1	1	1	1
09H	1	1	1	1	0	1	1
0AH	0	0	0	0	0	0	0
0BH	0	0	0	0	0	0	0
0CH	0	0	0	0	0	0	0
0DH	0	0	0	0	0	0	0
0EH	0	0	0	0	0	0	0
0FH	0	0	0	0	0	0	0

(c) ROM realization

Figure 6.28 ROM realization of a BCD-to-7-segment converter.