Figure 6.21 Models of memories.
Figure 6.22 Static RAM.

(a) A model of static RAM

<table>
<thead>
<tr>
<th>Operation</th>
<th>CE</th>
<th>WE</th>
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<tbody>
<tr>
<td>Disable RAM</td>
<td>F(H)</td>
<td>X</td>
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<tr>
<td>Read</td>
<td>T(L)</td>
<td>F(H)</td>
</tr>
<tr>
<td>Write</td>
<td>T(L)</td>
<td>T(L)</td>
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Where F: false
T: true
X: don't care
L: low
H: high

(b) Operations
Figure 6.23  Typical commercially available 1K × 4 RAM.
Figure 6.24 Realization of a 1K × 8 RAM.
Figure 6.25  Realization of a $2K \times 4$ RAM.
Figure 6.26 Memory read and memory write cycles.
Figure 6.31  Basic operations for a dynamic RAM.
Figure 6.27 A model of a read-only memory under normal operation.
Figure 6.29  The 2716 EPROM.
**BCD-to-7-segment converter**

\[
\begin{array}{c}
4 \\
B_3-B_0 \\
Z_6-Z_0
\end{array}
\]

Where
- \( Z_6 = a \)
- \( Z_5 = b \)
- \( Z_4 = c \)
- \( Z_3 = d \)
- \( Z_2 = e \)
- \( Z_1 = f \)
- \( Z_0 = g \)

(a) Problem definition

(b) Truth table

<table>
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<tr>
<th>B_3</th>
<th>B_2</th>
<th>B_1</th>
<th>B_0</th>
<th>Z_6</th>
<th>Z_5</th>
<th>Z_4</th>
<th>Z_3</th>
<th>Z_2</th>
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(c) ROM realization

**Figure 6.28** ROM realization of a BCD-to-7-segment converter.