

- 6.1. What are the advantages of using LSI circuit elements in a digital circuit as compared to using MSI and SSI circuit elements?
- 6.2. A 16-bit ALU is to be realized by interconnecting four 74'181 ALUs.
 (a) Draw the circuit diagram.
 (b) Given that the propagation delay for a 74'181 to perform an add operation is $t_p(181ADD)$, how long does it take your ALU to perform a 16-bit add operation? Explain.
 (c) Given that the propagation delay for a 74'181 to perform a logic operation is $t_p(181LOG)$, how long does it take your ALU to perform a 16-bit logic operation? Explain.
- 6.3. Using a 74'181 and any additional logic that is required, design and realize the simplified ALU shown in block diagram form in Fig. 6.33. This ALU produces an output F that is the result of some operation on the inputs A and B. The particular operation depends on the control word SEL, as follows:

SEL	Operation	Definition
0	Add	$F \leftarrow A \text{ plus } B$
1	Subtract	$F \leftarrow A \text{ minus } B$
2	Increment	$F \leftarrow A \text{ plus } 1$
3	Decrement	$F \leftarrow A \text{ minus } 1$
4	Complement	$F \leftarrow \text{NOT } A$
5	OR	$F \leftarrow A + B$
6	XOR	$F \leftarrow A \oplus B$

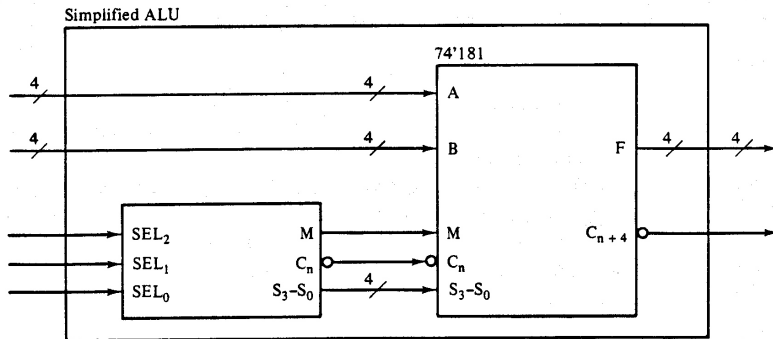


Figure 6.33 Simplified ALU for Problem 6.3.

- 6.4. Repeat Problem 6.3 using the block diagram of the simplified ALU shown in Fig. 6.34 and also the active-low view of the 74'181.

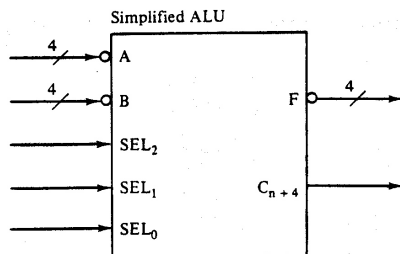


Figure 6.34 Simplified ALU for Problem 6.4.

6.5. For the chain of full adders shown in Fig. 6.2, what is the logic equation for the look-ahead carry circuit for C_2 ?

6.6. The following 2-bit numbers A and B are to be added:

Stage	N	$N - 1$	$N - 2$	$N - 3$	$N - 4$	$N - 5$	$N - 6$...
A	0	1	0	0	1	0	1	...
B	1	0	0	1	1	1	0	...

Find the values of the carry-outs produced by the following stages: (a) $N - 4$, (b) $N - 2$, (c) $N - 3$, (d) $N - 1$, and (e) $N - 5$. Explain your answers.

6.7. Convert the ripple adder circuit shown in Fig. 6.2 into a 4-bit adder with look-ahead carry circuitry, using a 74'182 and any additional logic that is required. (*Hint*: The carry-in of each adder stage will be generated by the 74'182.)

6.8. Determine the propagation delay required by an add operation for the 64-bit ALU with multilevel look-ahead carry structure shown in Fig. 6.7. Assume the following delay values:

$$\begin{aligned}
 t_p(181PG) &= 33 \text{ ns to produce G and P} \\
 t_p(181ADD) &= 27 \text{ ns to perform an add operation} \\
 t_p(182PG) &= 25 \text{ ns to produce the } P_i \text{ and } G_i \\
 t_p(182C_{xyz}) &= 26 \text{ ns to produce } C_{n+x}, C_{n+y}, \text{ and } C_{n+z}
 \end{aligned}$$

6.9. Transform the logic diagram of Fig. 6.35 into a PLA circuit diagram similar to the one shown in Fig. 6.10(b).

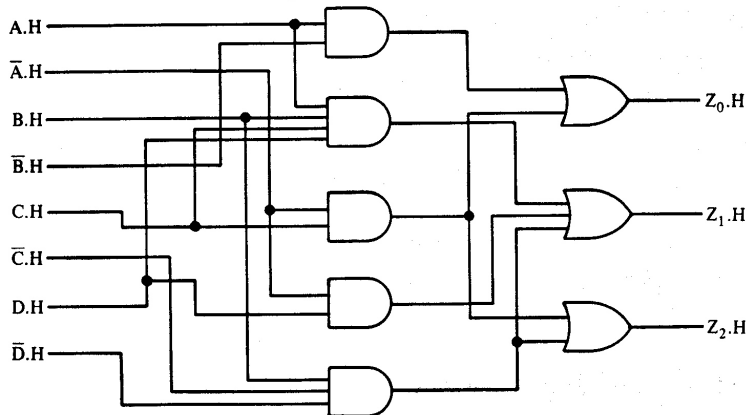


Figure 6.35 Logic diagram for Problem 6.9.

6.10. Given the truth table of Fig. 6.36 for the combinational circuit shown in block diagram form, realize the combinational circuit with a PLA that is similar to the one shown in Fig. 6.10(b) (i.e., one with four inputs, four outputs, and supporting eight product terms).

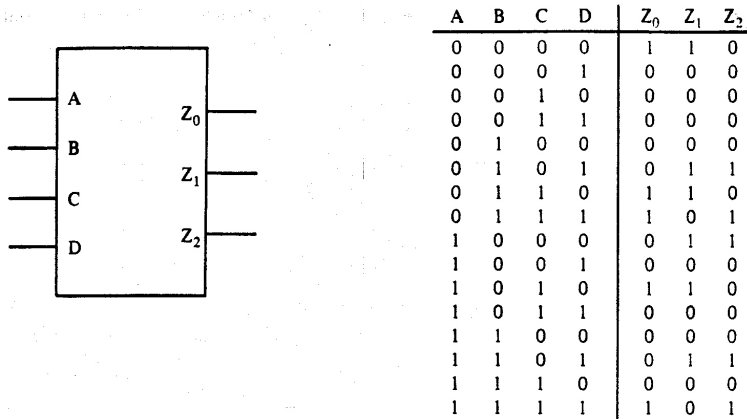


Figure 6.36 Block diagram and truth table for Problem 6.10.

6.11. Repeat Problem 6.10 for the block diagram and truth table shown in Fig. 6.37.

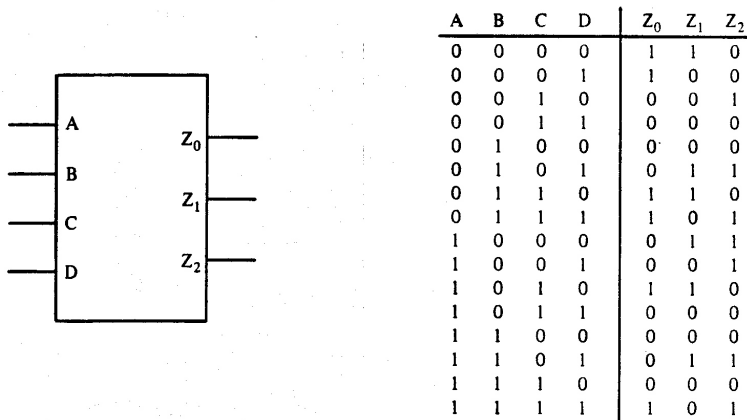


Figure 6.37 Block diagram and truth table for Problem 6.11.

- 6.12. Given the programmed PLA of Fig. 6.38 with functions similar to those of the 82S100 FPLA,
- What are the logic/voltage assignments (i.e., active-high or active-low) for the inputs A, B, C, D, and CE and for the outputs Z₀, Z₁, and Z₂?
 - Draw the mixed-logic block diagram for the corresponding combinational circuit.
 - Determine the logic equations for Z₀, Z₁, and Z₂.

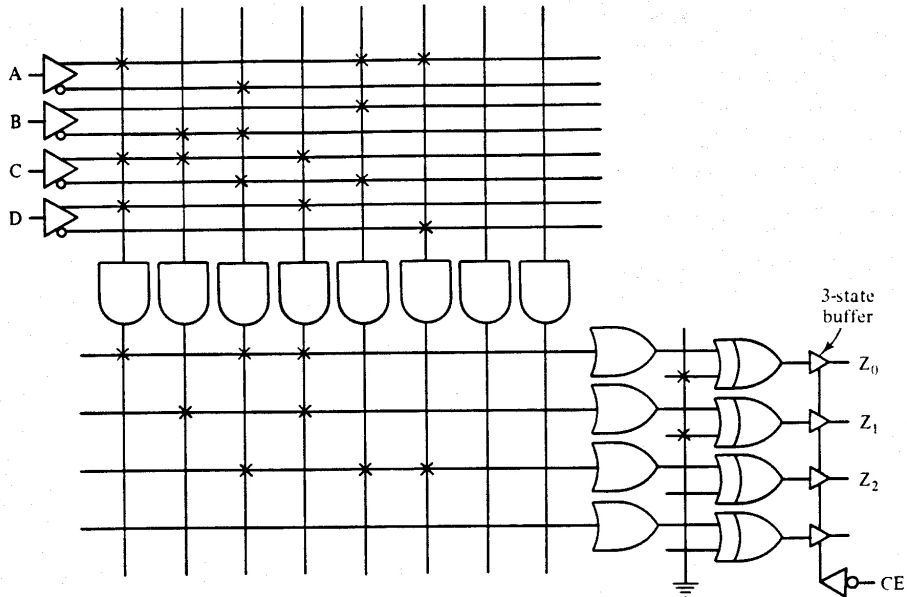


Figure 6.38 Programmed PLA for Problem 6.12.

- 6.13. What is the main difference between a PLA and a PAL?
- 6.14. Using the same PAL16L8, realize the following logic equations and have the realizations based on the following assignments:

Inputs: X_1 .H is assigned to pin 2, X_2 .H is assigned to pin 3, S_1 .H is assigned to pin 17, and S_2 .H is assigned to pin 16.

Outputs: Z_1 .L is assigned to pin 19, Z_2 .L is assigned to pin 18, Z_3 .L is assigned to pin 12, and Z_4 .H is assigned to pin 13.

All the other pins are not to be used unless specified otherwise.

(a) $Z_1 = S_2 \cdot X_1$ (Hint: Pin 16 needs to be programmed as an input.)

(b) $Z_2 = S_1 + S_1 \cdot \overline{X_2}$

(c) $Z_3 = X_2 \cdot (S_2 + S_1 \cdot \overline{X_1})$ (Hint: You can use pin 11 also if necessary.)

(d) $Z_4 = X_1 + X_2$ (Hint: Since Z_4 is active-high, you may need to use DeMorgan's laws.)

- 6.15. Using a PAL16L8, realize a BCD-to-7-segment decoder similar to the one shown in Fig. 6.28. However, the outputs a, b, c, d, e, f, and g are to be active-low.
- 6.16. Using a PAL16R4, realize a 4-bit decade counter with a synchronous CLEAR input. Compare your realization with the one obtained in Problem 5.26.
- 6.17. Draw block diagrams corresponding to the following static RAM module specifications. Specify the number of address lines and data lines.
- (a) 64×4 bits (b) 4096×8 bits (c) $64K \times 8$ bits

- 6.18. What is the capacity of a static RAM module that has
 (a) Seven address lines and eight data lines?
 (b) Fourteen address lines and four data lines?
 (c) Ten address lines and sixteen data lines?
- 6.19. Realize the $2K \times 8$ RAM module of Fig. 6.39 by using four $1K \times 4$ RAMs, as shown in Fig. 6.23, and an inverter.

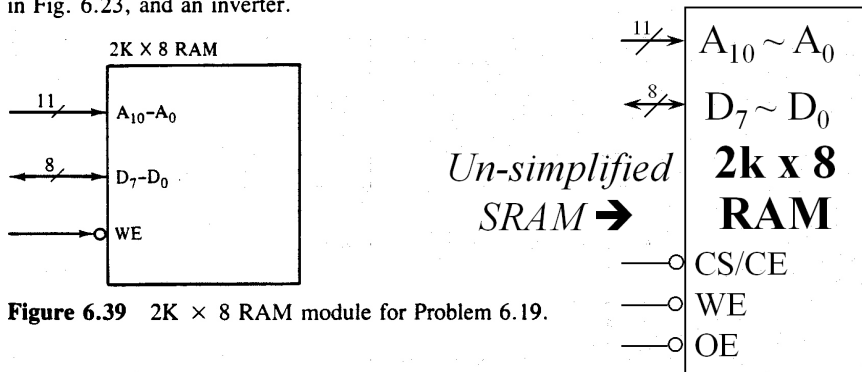


Figure 6.39 $2K \times 8$ RAM module for Problem 6.19.

- 6.20. Realize the $4K \times 4$ RAM module of Fig. 6.40 by using four $1K \times 4$ RAMs, as shown in Fig. 6.23, and a 4-to-2 decoder.

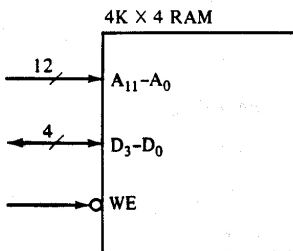


Figure 6.40 $4K \times 4$ RAM module for Problem 6.20.

- 6.21. Realize the $2K \times 4$ RAM module with chip-select input of Fig. 6.41 by using $1K \times 4$ RAMs, as shown in Fig. 6.23, and any additional logic that is necessary.

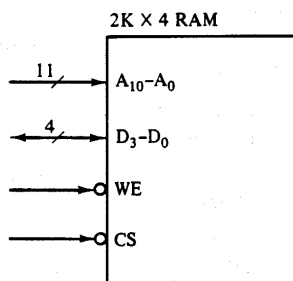


Figure 6.41 $2K \times 4$ RAM module for Problem 6.21.

- 6.22. Realize the memory module of Fig. 6.42 by using a $1K \times 4$ RAM, as shown in Fig. 6.23, and any additional logic that is necessary. Note that the bidirectional data lines of the $1K \times 4$ RAM become two sets of data lines, DIN and DOUT. (Hint: Use three-state buffers.)

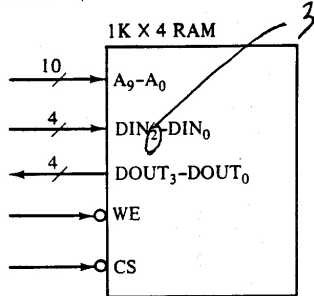


Figure 6.42 Memory module for Problem 6.22.

- 6.23. The static RAM chip shown in Fig. 6.26(a) has the following timing parameter values:

$$\begin{aligned} t_{RC} &= 100 \text{ ns minimum} \\ t_A(AD) &= 100 \text{ ns minimum} \\ t_A(CE) &= 75 \text{ ns minimum} \end{aligned}$$

At $t = 0$ s, a valid address is applied and the WE signal is set to false (H).

- (a) If the chip-enable signal (CE) is applied at $t = 10$ ns, then when is the time t at which the data first becomes valid?
 (b) If the chip-enable signal (CE) is applied at $t = 50$ ns, then when is the time t at which the data first becomes valid?
- 6.24. The static RAM chip shown in Fig. 6.26(a) has the following timing parameters:

$$\begin{aligned} t_{WC} &= 100 \text{ ns minimum} \\ t_{SU}(CE) &= 70 \text{ ns minimum} \\ t_W(WE) &= 100 \text{ ns minimum} \\ t_{SU}(DA) &= 70 \text{ ns minimum} \end{aligned}$$

At $t = 0$ s, a valid address is applied and the WE signal is set to true (L).

- (a) If CE and the data are applied at $t = 0$ s, then the WE signal must remain true (L) until a time t_x to ensure a valid write operation. What is this time t_x ?
 (b) If CE is applied at $t = 50$ ns and the data is applied at $t = 0$ s, then what is this time t_x ?
 (c) If CE is applied at $t = 0$ s and the data is applied at $t = 50$ ns, then what is this time t_x ?
- 6.25. Discuss the similarities and differences among ROMs, PROMs, and EPROMs.
- 6.26. The hardware multiplier of Fig. 6.43 can multiply two 4-bit numbers (MCAND and MPLIER) and produce an 8-bit product (PRODUCT).
- (a) Derive the truth table for this circuit. Use don't cares when convenient.
 (b) If a ROM is used to realize this circuit, what must be the ROM capacity?
 (c) Draw a block diagram of the ROM realization, specifying all connections to the address and data lines.
 (d) What are the contents of the ROM? Explain in words.

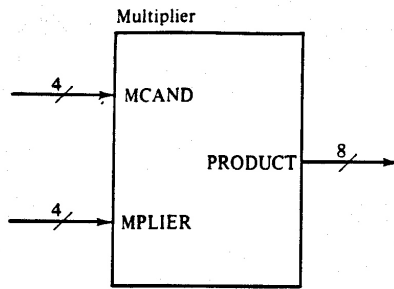


Figure 6.43 Multiplier for Problem 6.26.

- 6.27. Use a ROM to realize the four logic functions $Z_{1.L}$, $Z_{2.L}$, $Z_{3.L}$, and $Z_{4.H}$ specified in Problem 6.14 as follows:
- Draw a block diagram design of the ROM realization, specifying all connections to the address and data lines.
 - Specify in hexadecimal the contents of the ROM.
 - Explain what an active-low output does to the corresponding contents of the ROM.
- 6.28. Consider a PLA with 12 inputs (actually 12 inputs and 12 complements), 8 outputs, and 64 AND gates. Can it be used to realize the following combinational circuits?
- A circuit with eight inputs and six outputs.
 - A circuit with six inputs and eight outputs.
- In each case answer yes, no, or maybe, and explain your answer.
- 6.29. Can you implement the logic equations of the following combinational circuits with a 128×8 ROM?
- A circuit with eight inputs and six outputs.
 - A circuit with six inputs and eight outputs.
- In each case answer yes, no, or maybe, and explain your answer.
- 6.30. Construct the memory module of Fig. 6.44 that provides $6K \times 8$ bits of EPROM and $2K \times 8$ bits of RAM. [Hint: Use three 2716 EPROMs and two $1K \times 8$ RAM modules (see Fig. 6.24), a 2-to-4 decoder, and any additional logic that is necessary.]

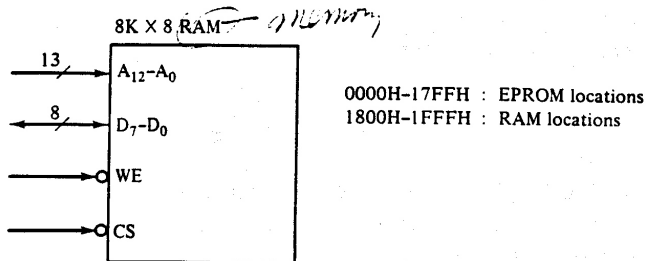


Figure 6.44 Memory module for Problem 6.30.

- 6.31. Discuss the advantages and disadvantages of using static RAMs versus dynamic RAMs in a digital circuit.
- 6.32. Consider the dynamic RAM of Fig. 6.45 that functions similarly to the one shown in Fig. 6.30(b).
- What is the capacity of this DRAM?

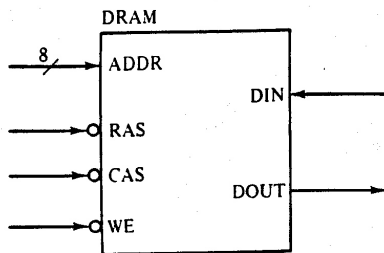


Figure 6.45 Dynamic RAM for Problem 6.32.

- (b) Explain in words the sequence of steps (in terms of signals and order of events) that are required to perform a memory read operation.
- (c) Explain in words the sequence of steps that are required to perform a memory write operation.
- (d) Explain in words the sequence of steps that are required to perform a memory refresh operation.
- 6.33. Construct the $16K \times 4$ memory module of Fig. 6.46 by using four $16K \times 1$ dynamic RAMs [as shown in Fig. 6.30(b)], a DRAM controller (similar to the one shown in Fig. 6.32), and any additional logic that is needed. Note that the data lines of the memory module are bidirectional, whereas the data lines of the $16K \times 1$ dynamic RAMs are divided into DIN and DOUT. (*Hint:* Use three-state buffers.)

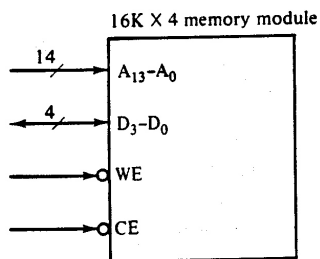


Figure 6.46 Memory module for Problem 6.33.