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- 115 minutes (plus 5 minutes for setup).
- Relevant topics include:
   > Labs 0-5 [6] (including <u>all</u> switch & LED circuits); HW 0-11; DAD usage.
- Something relatively simple.
- You will design, debug, and demo for a PI, Dr. Schwartz.
- <u>NOT</u> allowed:
  - > Labs, homework, notes, etc.
  - > Other student's info.
  - > Another computer, calculator, ...
  - > Cell phone, until your are done and ready to take the required pictures
  - > Documentation of any kind (HW, Labs, Notes, Pinouts).
  - > Pre-built circuits; anything not specifically mentioned as allowed.
  - > Access to anything else not specified.



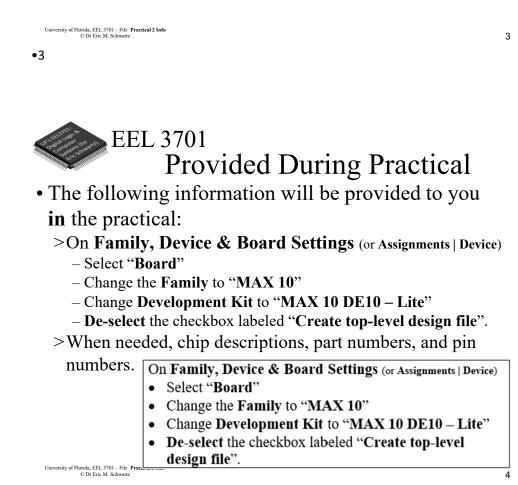
- In order to get partial credit:
  - >If you cannot demo everything, it is up to you to figure out a way to demo at least part of the requirements.
  - >Points are only awarded for items that are demoed/simulated, not for designs that are not demoed/simulated.
  - >No points are awarded for designs without demo or simulation.

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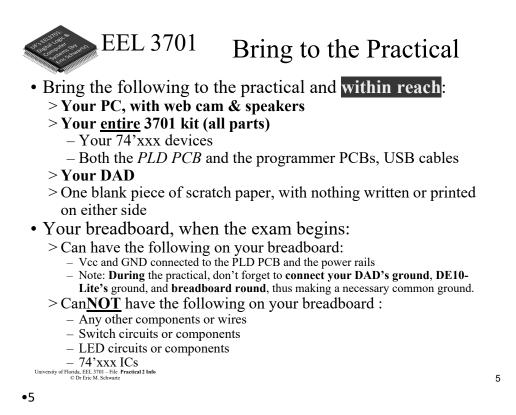


• Prior to the practical, a PI (probably <u>NOT</u> your lab PI), will send you a Zoom link to use for the practical.



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EEL 3701 Losing Internet Connection

• If you ever have WiFi or other internet connection problems just before or when your practical begins, use your **phone** to connect to Zoom.

>Zoom chat with the relevant PI.

- Describe the issue and continue to try to get back in!
- The PI will contact Dr. Schwartz.

>As an emergency backup (if your internet goes out), you should learn how to setup your phone as a WiFi hotspot.

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- If you are having problems with Honorlock, contact Honorlock and keep trying!
- Also send a Zoom chat message to the PI. >The PI will contact Dr. Schwartz.

EEL 3701 Honorlock Room Scan, **if Requested** 

• The room scan should be thorough and take about one minute. See <u>Honorlock: Proper Room Scan</u> (on the front page of our website).

>Be sure to how your desk, computer monitor, walls, floor near your computer, and ceiling.

• In addition to the complete room scan, show each of the following:

>Both sides of scratch paper

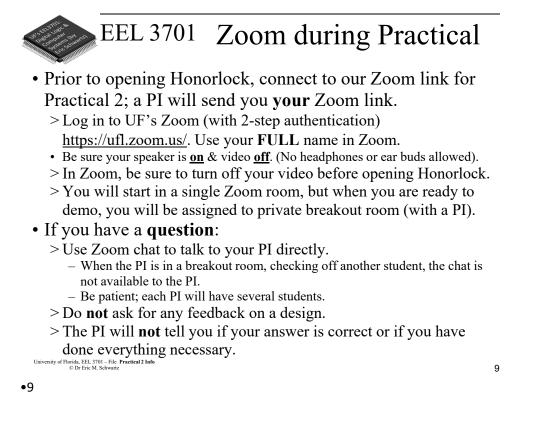
>Your breadboard (containing nothing not allowed)

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# EEL 3701 Honorlock ID Scan Extras

- After your Honorlock ID scan, show the following to your camera.
  - >Both sides of your scratch paper.
  - >Your breadboard (containing nothing not allowed).
- You will scan and submit images of this paper with CamScanner or equivalent as specified later in this document.

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### • **DURING** the exam

- >Use of MS-Word (or similar) and email is <u>NOT</u> allowed.
- >No physical phone connection to your computer is allowed.
- >No printer/scanner is allowed.
- Be sure to **view** the file on your phone **before** submission to assure that it is **complete and clear**.
- Bring 1 completely blank piece of paper and pens/pencils.

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Paper Submission at EEL 3701 **End of Practical** 

- Only after you are completed the rest of the exam (or when 5 minutes are remaining), do the following. >Archive your work in Quartus.
  - Upload the Quartus archive to your Canvas/Honorlock quiz.
  - >Use your cell phone and CamScanner (or similar) to create a SINGLE PDF file.
    - After picking up your phone, **no more writing/work** is allowed!
    - Take a clear picture of your breadboard.
    - Take a clear picture of each utilized side of your scratch paper.
      The scratch paper must include the switch/LED legends.
    - All of this should be in a **SINGLE PDF** file. View the file on your phone before submission to assure that it is complete.
    - Upload this **SINGLE** file to the *Practical 2 Phone* Camvas assignment.

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EEL 3701

# Integrity

- After touching your phone or archiving Quartus, **no more writing/work** is allowed!
- Once you start scanning your paper/breadboard or start archiving you Quartus project, you are no longer allowed to make any changes (including the following):
  - >Your circuit design on your breadboard.
  - >Your Quartus design, simulation, or PLD program.
  - >Your scratch paper.
- No more work is allowed, other than the required submission of the two files.

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## EEL 3701 Honorlock During Practical

- In Honorlock, you must share your computer screen, video, and audio with the proctoring PI at all times. Do **NOT** close Honorlock until after your demo.
- If you are finished before the time is up, let the PI know, and when the PI has time, they will let you demo.
  - > Tell the PI you are ready by sending **READY** in the Zoom chat.
  - > The PI will instruct you to close Honorlock and you will perform the required demo.
- If you are not finished until the deadline, the assignment will automatically close when time is up. It is therefore **critical** that you upload your files before time is up!

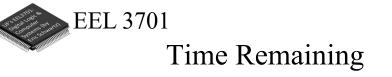
> If you do not, then you will **earn a zero** on the Practical.

• When demoing, you will also share your screen and your camera with Zoom.

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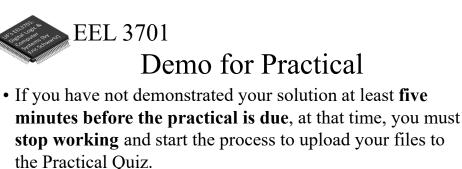
- Keep you speakers on so that you can hear any announcement that the PI makes.
- The PI will **VERBALLY** tell you when 5 minutes are remaining (and also a few other times, like 37 minutes and 10 minutes remaining).

• You will have only **ONE** chance to demo your work

- > If you think you are ready, read the question AGAIN to be sure that you completed <u>ALL</u> parts of the Practical.
- > Be prepared to run your design, as instructed, with your DAD connected as specified.
- >Before closing Honorlock, upload the required files to the Practical Quiz.
- ><u>After</u> you have uploaded your files, notify your PI by sending the message **READY** in the Zoom chat. Do <u>NOT</u> leave the Zoom meeting.

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> Failure to upload your files before the end of the practical will result in a **grade of zero**.

• After completing your uploads, continue in Honorlock and do **not** leave the Zoom meeting.

You <u>must NOT</u> leave the Zoom meeting until you demo something (or to tell your PI that you are giving up); if you do give up without a demo, you will earn a zero.

> Once you leave Zoom, you will not be able to reenter the Zoom Practical.

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## Practical 2 Preview

- Something like this (a VHDL Syntax Example) will be available to you **in** the practical.
- Also available, PLD device family, device & board settings.

```
VHDL Syntax Example
library ieee;
use ieee.std_logic_1164.all;
```

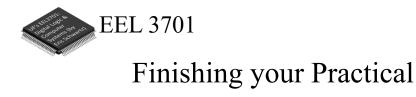
end behav;

C	n Family, Device & Board Settings (or Assignments   Device)	
•	Select "Board"	
•	Change the Family to "MAX 10"	
•	Change Development Kit to "MAX 10 DE10 – Lite"	
•	De-select the checkbox labeled "Create top-level	
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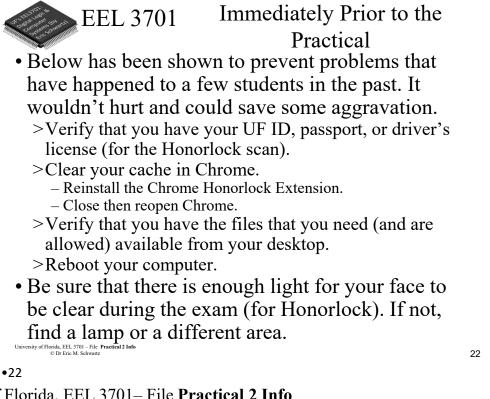


• After you have demonstrated your Practical solution, close Zoom.

>Your are done!

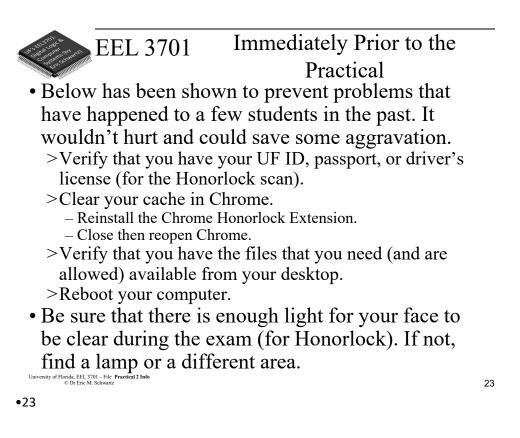
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The End!

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