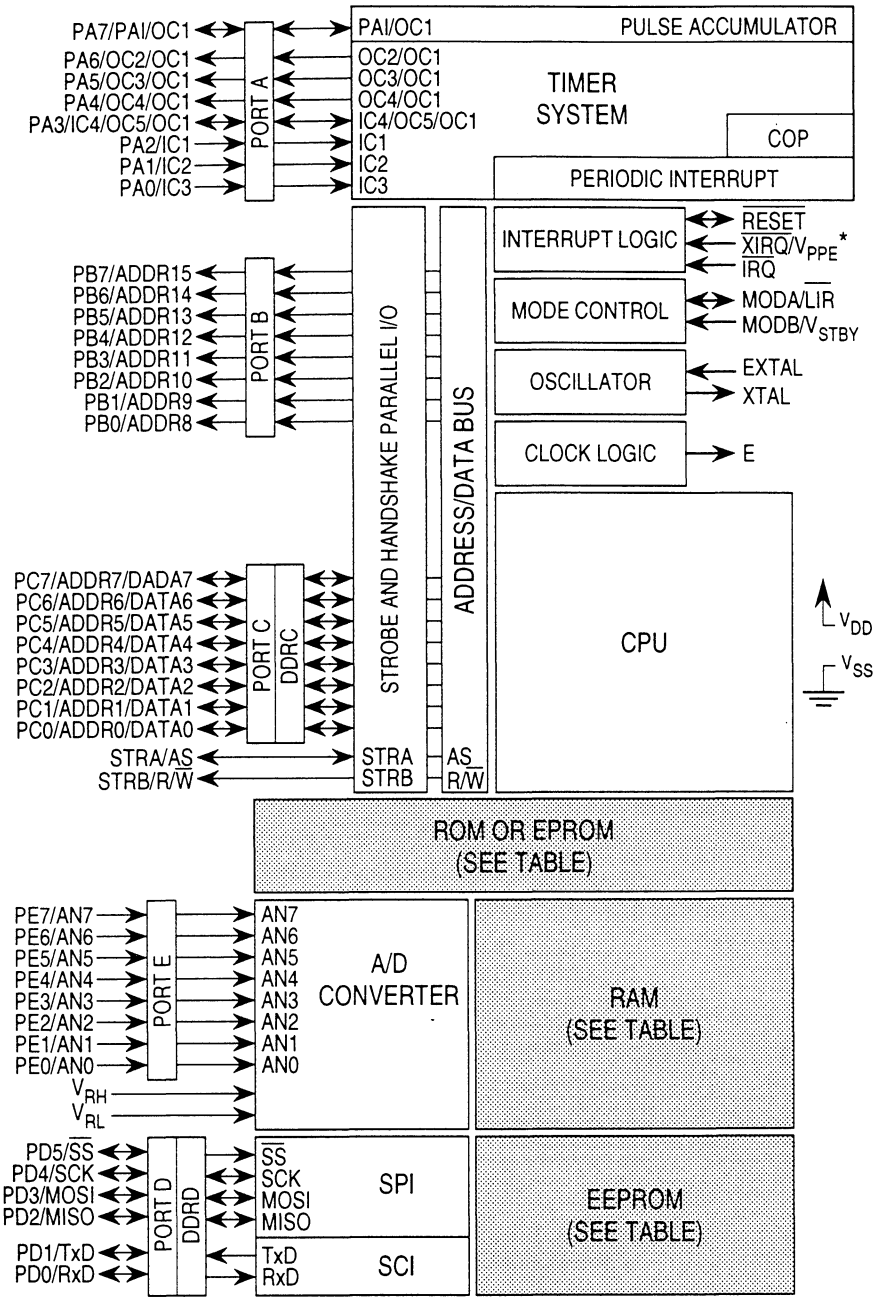
MC68HC11ERG/AD

HC11

M68HC11 E SERIES

PROGRAMMING REFERENCE GUIDE

Block Diagram



DEVICE	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E8	512	12K	—	—
MC68HC11E9	512	12K	—	512
MC68HC711E9	512	—	12K	512
MC68HC11E20	768	20K	—	512
MC68HC711E20	768	—	20K	512
MC68HC811E2	256	—	—	2048

* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

PROGRAMMING MODEL
CRYSTAL DEPENDENT TIMING
INTERRUPTS

MEMORY MAP
OPCODE MAPS

INSTRUCTIONS
ADDRESSING MODES
EXECUTION TIMES
SPECIAL OPERATIONS

REGISTER AND
CONTROL BIT
ASSIGNMENTS

MECHANICAL DATA
HEX/DEC CONVERSION
ASCII CHART

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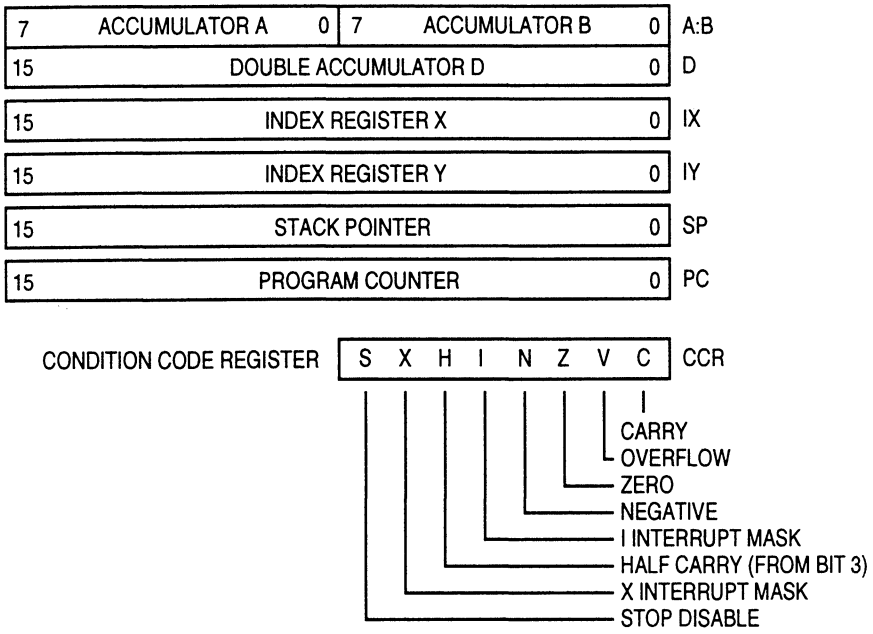
Devices Covered in This Reference Guide

Device	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E8	512	12K	—	—
MC68HC11E9	512	12K	—	512
MC68HC711E9	512	—	12K	512
MC68S711E9	512	—	12K	512
MC68HC11E20	768	20K	—	512
MC68HC711E20	768	—	20K	512
MC68HC811E2	256	—	—	2048

M68HC11 E Series Programming Model



Crystal Dependent Timer Summary

	Selected	Common XTAL Frequencies		
	Crystal	4.0 MHz	8.0 MHz	12.0 MHz
CPU Clock	(E)	1.0 MHz	2.0 MHz	3.0 MHz
Cycle Time	(1/E)	1000 ns	500 ns	333 ns
	Pulse Accumulator (in Gated Mode)			
($E/2^6$)	1 count —	64.0 µs	32.0 µs	21.330 µs
($E/2^{14}$)	overflow —	16.384 ms	8.192 ms	5.491 ms
	PR[1:0]	Main Timer Count Rates		
	0 0			
(E/1)	1 count —	1.0 µs	500 ns	333 ns
($E/2^{16}$)	overflow —	65.536 ms	32.768 ms	21.845 ms
	0 1			
(E/4)	1 count —	4.0 µs	2.0 µs	1.333 µs
($E/2^{18}$)	overflow —	262.14 ms	131.07 ms	87.381 ms
	1 0			
(E/8)	1 count —	8.0 µs	4.0 µs	2.667 µs
($E/2^{19}$)	overflow —	524.29 ms	262.14 ms	174.76 ms
	1 1			
(E/16)	1 count —	16.0 µs	8.0 µs	5.333 µs
($E/2^{20}$)	overflow —	1.049 s	524.29 ms	349.52 ms
	RTR[1:0]	Periodic (RTI) Interrupt Rates		
($E/2^{13}$)	0 0	8.192 ms	4.096 ms	2.731 ms
($E/2^{14}$)	0 1	16.384 ms	8.192 ms	5.461 ms
($E/2^{15}$)	1 0	32.768 ms	16.384 ms	10.923 ms
($E/2^{16}$)	1 1	65.536 ms	32.768 ms	21.845 ms
	CR[1:0]	COP Watchdog Timeout Rates		
($E/2^{15}$)	0 0	32.768 ms	16.384 ms	10.923 ms
($E/2^{17}$)	0 1	131.072 ms	65.536 ms	43.691 ms
($E/2^{19}$)	1 0	524.288 ms	262.14 ms	174.76 ms
($E/2^{21}$)	1 1	2.097 s	1.049 s	699.05 ms
	Timeout Tolerance			
($E/2^{15}$)	(– 0 ms/+...)	32.8 ms	16.4 ms	10.9 ms

Interrupt Vector Assignments

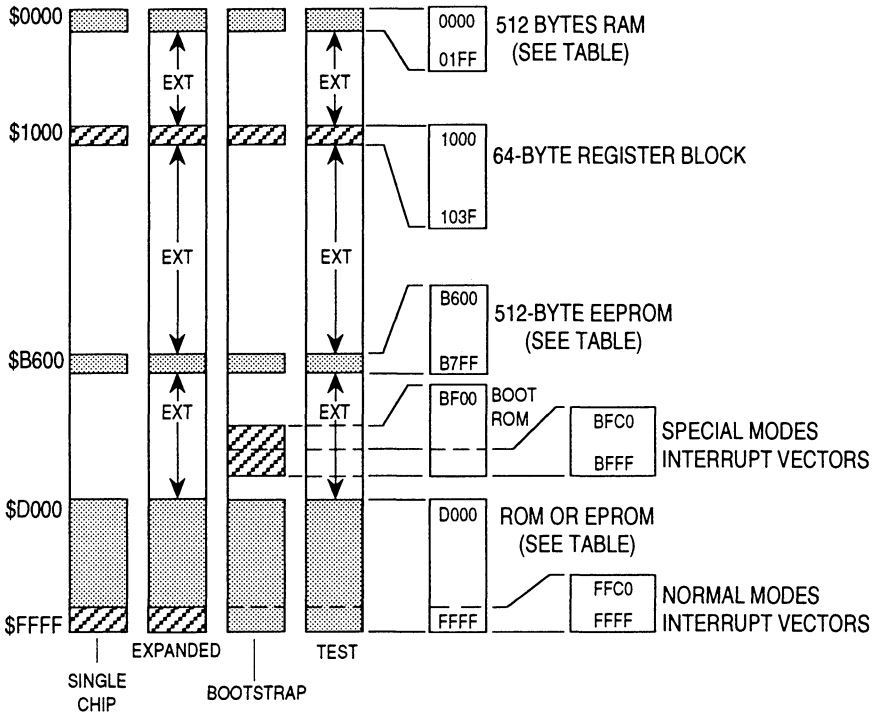
Vector Address	Interrupt Source	CCR Mask Bit	Local Mask
FFC0, C1 – FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System*	I	
	• SCI Receive Data Register Full		RIE
	• SCI Receiver Overrun		RIE
	• SCI Transmit Data Register Empty		TIE
	• SCI Transmit Complete		TCIE
	• SCI Idle Line Detect		ILIE
FFD8, D9	SPI Serial Transfer Complete	I	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I	PAII
FFDC, DD	Pulse Accumulator Overflow	I	PAOVI
FFDE, DF	Timer Overflow	I	TOI
FFE0, E1	Timer Input Capture 4/ Output Compare 5	I	I4/O5I
FFE2, E3	Timer Output Compare 4	I	OC4I
FFE4, E5	Timer Output Compare 3	I	OC3I
FFE6, E7	Timer Output Compare 2	I	OC2I
FFE8, E9	Timer Output Compare 1	I	OC1I
FFEA, EB	Timer Input Capture 3	I	IC3I
FFEC, ED	Timer Input Capture 2	I	IC2I
FFEE, EF	Timer Input Capture 1	I	IC1I
FFF0, F1	Real-Time Interrupt	I	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (External Pin)	I	None
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	X	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	Clock Monitor Fail	None	CME
FFFE, FF	$\overline{\text{RESET}}$	None	None

*Interrupts generated by SCI; read SCSR to determine source
Refer to HPRIO register to determine priority of interrupt

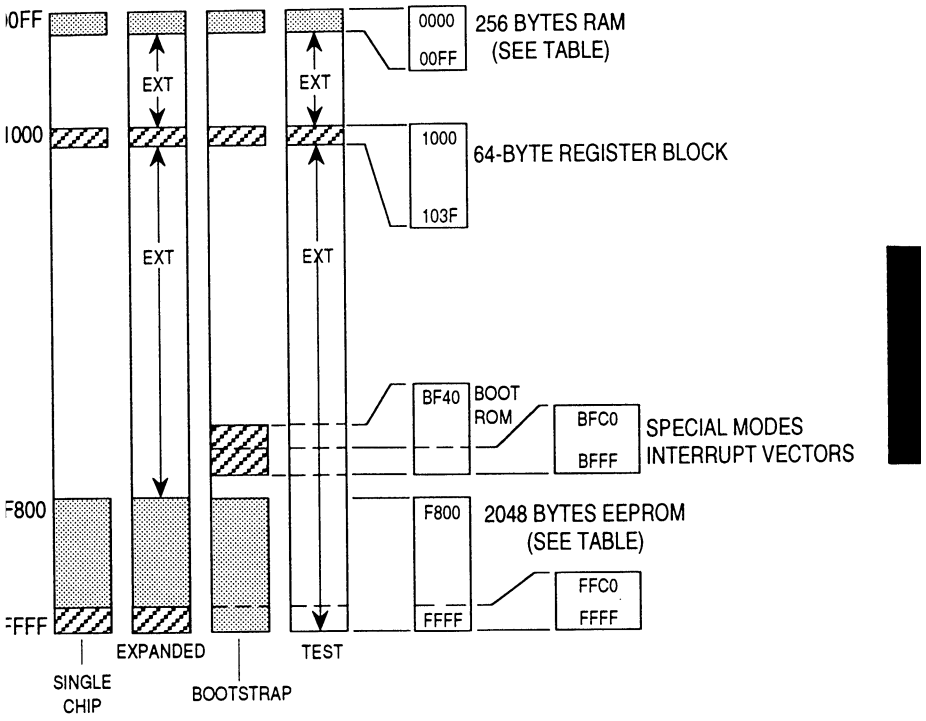
M68HC11 E Series Memory Map
(Includes MC68HC11E0, MC68HC11E1, MC68HC11E8, and MC68HC(7)11E9)

DEVICE	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E8	512	12K	—	—
MC68HC11E9	512	12K	—	512
MC68HC711E9	512	—	12K	512
MC68HC11E20*	768	20K	—	512
MC68HC711E20*	768	—	20K	512
MC68HC811E2 **	256	—	—	2048

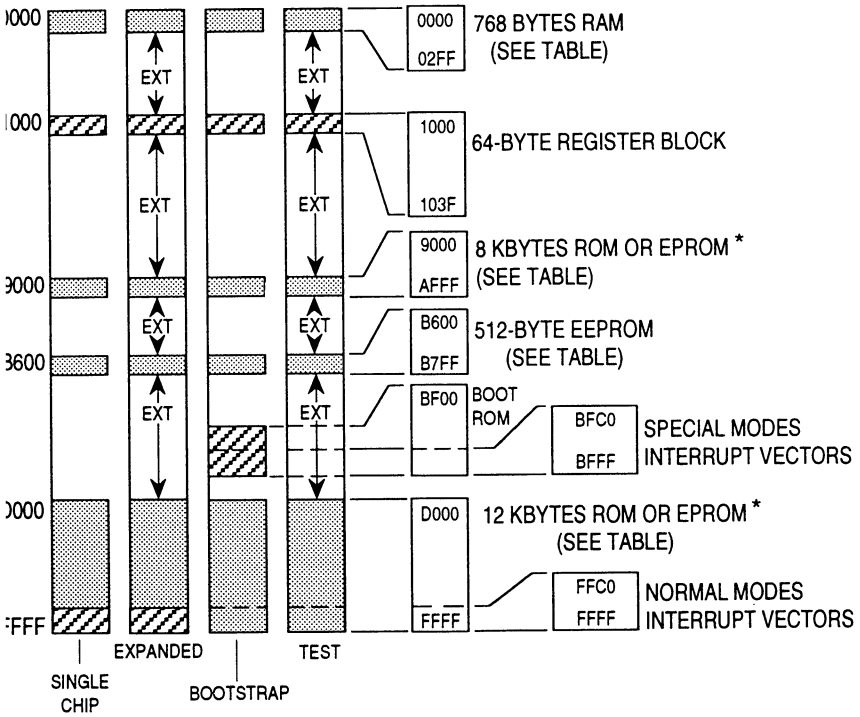
* REFER TO MC68HC(7)11E20 MEMORY MAP DIAGRAM.
** REFER TO MC68HC811E2 MEMORY MAP DIAGRAM.



MC68HC811E2 Memory Map



MC68HC(7)11E20 Memory Map



* 20 KBYTES OF ROM/EPROM ARE CONTAINED IN TWO SEGMENTS OF 8 KBYTES AND 12 KBYTES EACH.

DIR

OPCODE MAP PAGE 1

		INH	INH	REL	INH	ACCA	ACCB	IND,X	EXT	ACCA IMM	ACCA DIR	ACCA IND,X	ACCA EXT	ACCB IMM	ACCB DIR	ACCB IND,X	ACCB EXT	
MSB →		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
LSB ↓		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	TEST*	SBA	BRA	TSX	NEG				SUB								0
0001	1	NOP	CBA	BRN	INS					CMP								1
0010	2	IDIV	BRSET	BHI	PULA					SBC								2
0011	3	EDIV	BRCLR	BLS	PULB	COM				SUBD				ADDD				3
0100	4	LSRD	BSET	BCC	DES	LSR				AND								4
0101	5	ASLD	BCLR	BCS	TXS					BIT								5
0110	6	TAP	TAB	BNE	PSHA	ROR				LDA								6
0111	7	TPA	TBA	BEQ	PSHB	ASR					STA				STA			7
1000	8	INX	PAGE 2	BVC	PULX	ASL				EOR								8
1001	9	DEX	DAA	BVS	RTS	ROL				ADC								9
1010	A	CLV	PAGE 3	BPL	ABX	DEC				ORA								A
1011	B	SEV	ABA	BMI	RTI					ADD								B
1100	C	CLC	BSET	BGE	PSHX	INC				CPX				LDD				C
1101	D	SEC	BCLR	BLT	MUL	TST				BSR	JSR			PAGE 4	STD			D
1110	E	CLI	BRSET	BGT	WAI			JMP		LDS				LDX				E
1111	F	SEI	BRCLR	BLE	SWI	CLR				XGDX	STS			STOP	STX			F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

IND,X

OPCODE MAP PAGE 2 (18XX)

		INH			INH			IND,Y		ACCA IMM	ACCA DIR	ACCA IND,Y	ACCA EXT	ACCB IMM	ACCB DIR	ACCB IND,Y	ACCB EXT	
MSB → / LSB ↓		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0				TSY			NEG				SUB				SUB		0
0001	1											CMP				CMP		1
0010	2											SBC				SBC		2
0011	3							COM				SUBD				ADDD		3
0100	4							LSR				AND				AND		4
0101	5				TYS							BIT				BIT		5
0110	6							ROR				LDA				LDA		6
0111	7							ASR				STA				STA		7
1000	8	INY			PULY			ASL				EOR				EOR		8
1001	9	DEY						RDL				ADC				ADC		9
1010	A				ABY			DEC				ORA				ORA		A
1011	B											ADD				ADD		B
1100	C		BSET		PSHY			INC		CPY						LDD		C
1101	D		BCLR					TST				JSR				STD		D
1110	E		BRSET					JMP				LDS		LDY				E
1111	F		BRCLR					CLR		XGDY		STS			STY			F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

7

IND,Y

OPCODE MAP PAGE 3 (1AXX)

									ACCA				ACCB			
									IMM	DIR	IND,X	EXT			IND,X	
MSB → / LSB ↓		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0																0
0001	1																1
0010	2																2
0011	3									CPD							3
0100	4																4
0101	5																5
0110	6																6
0111	7																7
1000	8																8
1001	9																9
1010	A																A
1011	B																B
1100	C											CPY					C
1101	D																D
1110	E															LDY	E
1111	F															STY	F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

OPCODE MAP PAGE 4 (CDXX)

		ACCA								ACCB							
											IND,Y					IND,Y	
MSB → / LSB ↓		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0																0
0001	1																1
0010	2																2
0011	3											CPD					3
0100	4																4
0101	5																5
0110	6																6
0111	7																7
1000	8																8
1001	9																9
1010	A																A
1011	B																B
1100	C											CPX					C
1101	D																D
1110	E															LDX	E
1111	F															STX	F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Simple Branches		
Mnemonic	**Opcode**	**Cycles**
BRA	20	3
BRN	21	3
BSR	8D	7

Simple Conditional Branches				
	True		**False**	
Test	**Instruction**	**Opcode**	**Instruction**	**Opcode**
N = 1	BMI	2B	BPL	2A
Z = 1	BEQ	27	BNE	26
V = 1	BVS	29	BVC	28
C = 1	BCS	25	BCC	24

Signed Conditional Branches				
	True		**False**	
Test	**Instruction**	**Opcode**	**Instruction**	**Opcode**
r > m	BGT	2E	BLE	2F
r ≥ m	BGE	2C	BLT	2D
r = m	BEQ	27	BNE	26
r ≤ m	BLE	2F	BGT	2E
r < m	BLT	2D	BGE	2C

Unsigned Conditional Branches				
	True		**False**	
Test	**Instruction**	**Opcode**	**Instruction**	**Opcode**
r > m	BHI	22	BLS	23
r ≥ m	BHS/BCC	24	BLO/BCS	25
r = m	BEQ	27	BNE	26
r ≤ m	BLS	23	BHI	22
r < m	BLO/BCS	25	BHS/BCC	24

Bit Manipulation Branches
BRCLR — Branch if all selected bits are clear (opcode) (operand addr) (mask) (rel offset) M • mm = 0? M = operand in memory; mm = mask
BRSET — Branch if all selected bits are set (opcode) (operand addr) (rel offset) $(\overline{M})$ • mm = 0? M = operand in memory; mm = mask

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
00		TEST	INH	—
01		NOP	INH	2
02		IDIV	INH	41
03		FDIV	INH	41
04		LSRD	INH	3
05		ASLD/LSLD	INH	3
06		TAP	INH	2
07		TPA	INH	2
08		INX	INH	3
09		DEX	INH	3
0A		CLV	INH	2
0B		SEV	INH	2
0C		CLC	INH	2
0D		SEC	INH	2
0E		CLI	INH	2
0F		SEI	INH	2
10		SBA	INH	2
11		CBA	INH	2
12	dd mm rr	BRSET (opr) (msk) (rel)	DIR	6
13	dd mm rr	BRCLR (opr) (msk) (rel)	DIR	6
14	dd mm	BSET (opr) (msk)	DIR	6
15	dd mm	BCLR (opr) (msk)	DIR	6
16		TAB	INH	2
17		TBA	INH	2
18		(Page 2 Switch)		
19		DAA	INH	2
1A		(Page 3 Switch)		
1B		ABA	INH	2
1C	ff mm	BSET (opr) (msk)	IND,X	7
1D	ff mm	BCLR (opr) (msk)	IND,X	7
1E	ff mm rr	BRSET (opr) (msk) (rel)	IND,X	7
1F	ff mm rr	BRCLR (opr) (msk) (rel)	IND,X	7

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
20	rr	BRA (rel)	REL	3
21	rr	BRN (rel)	REL	3
22	rr	BHI (rel)	REL	3
23	rr	BLS (rel)	REL	3
24	rr	BCC/BHS (rel)	REL	3
25	rr	BCS/BLO (rel)	REL	3
26	rr	BNE (rel)	REL	3
27	rr	BEQ (rel)	REL	3
28	rr	BVC (rel)	REL	3
29	rr	BVS (rel)	REL	3
2A	rr	BPL (rel)	REL	3
2B	rr	BMI (rel)	REL	3
2C	rr	BGE (rel)	REL	3
2D	rr	BLT (rel)	REL	3
2E	rr	BGT (rel)	REL	3
2F	rr	BLE (rel)	REL	3
30		TSX	INH	3
31		INS	INH	3
32		PULA	INH	4
33		PULB	INH	4
34		DES	INH	3
35		TXS	INH	3
36		PSHA	INH	3
37		PSHB	INH	3
38		PULX	INH	5
39		RTS	INH	5
3A		ABX	INH	3
3B		RTI	INH	12
3C		PSHX	INH	4
3D		MUL	INH	10
3E		WAI	INH	14
3F		SWI	INH	14
40		NEGA	INH	2
43		COMA	INH	2
44		LSRA	INH	2
46		RORA	INH	2
47		ASRA	INH	2
48		ASLA/LSLA	INH	2
49		ROLA	INH	2
4A		DECA	INH	2
4C		INCA	INH	2
4D		TSTA	INH	2
4F		CLRA	INH	2
50		NEGB	INH	2

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
53		COMB	INH	2
54		LSRB	INH	2
56		RORB	INH	2
57		ASRB/ASLB	INH	2
58		LSLB	INH	2
59		ROLB	INH	2
5A		DECB	INH	2
5C		INCB	INH	2
5D		TSTB	INH	2
5F		CLRB	INH	2
60	ff	NEG (opr)	IND,X	6
63	ff	COM (opr)	IND,X	6
64	ff	LSR (opr)	IND,X	6
66	ff	ROR (opr)	IND,X	6
67	ff	ASR (opr)	IND,X	6
68	ff	ASL/LSL (opr)	IND,X	6
69	ff	ROL (opr)	IND,X	6
6A	ff	DEC (opr)	IND,X	6
6C	ff	INC (opr)	IND,X	6
6D	ff	TST (opr)	IND,X	6
6E	ff	JMP (opr)	IND,X	3
6F	ff	CLR (opr)	IND,X	6
70	hh ll	NEG (opr)	EXT	6
73	hh ll	COM (opr)	EXT	6
74	hh ll	LSR (opr)	EXT	6
76	hh ll	ROR (opr)	EXT	6
77	hh ll	ASR (opr)	EXT	6
78	hh ll	ASL/LSL (opr)	EXT	6
79	hh ll	ROL (opr)	EXT	6
7A	hh ll	DEC (opr)	EXT	6
7C	hh ll	INC (opr)	EXT	6
7D	hh ll	TST (opr)	EXT	6
7E	hh ll	JMP (opr)	EXT	3
7F	hh ll	CLR (opr)	EXT	6
80	ii	SUBA (opr)	IMM	2
81	ii	CMPA (opr)	IMM	2
82	ii	SBCA (opr)	IMM	2
83	jj kk	SUBD (opr)	IMM	4
84	ii	ANDA (opr)	IMM	2
85	ii	BITA (opr)	IMM	2
86	ii	LDAA (opr)	IMM	2
88	ii	EORA (opr)	IMM	2
89	ii	ADCA (opr)	IMM	2
8A	ii	ORAA (opr)	IMM	2

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
8B	ii	ADDA (opr)	IMM	2
8C	jj kk	CPX (opr)	IMM	4
8D	rr	BSR (rel)	REL	6
8E	jj kk	LDS (opr)	IMM	3
8F		XGDX	INH	3
90	dd	SUBA (opr)	DIR	3
91	dd	CMPA (opr)	DIR	3
92	dd	SBCA (opr)	DIR	3
93	dd	SUBD (opr)	DIR	5
94	dd	ANDA (opr)	DIR	3
95	dd	BITA (opr)	DIR	3
96	dd	LDAA (opr)	DIR	3
97	dd	STAA (opr)	DIR	3
98	dd	EORA (opr)	DIR	3
99	dd	ADCA (opr)	DIR	3
9A	dd	ORAA (opr)	DIR	3
9B	dd	ADDA (opr)	DIR	3
9C	dd	CPX (opr)	DIR	5
9D	dd	JSR (opr)	DIR	5
9E	dd	LDS (opr)	DIR	4
9F	dd	STS (opr)	DIR	4
A0	ff	SUBA (opr)	IND,X	4
A1	ff	CMPA (opr)	IND,X	4
A2	ff	SBCA (opr)	IND,X	4
A3	ff	SUBD (opr)	IND,X	6
A4	ff	ANDA (opr)	IND,X	4
A5	ff	BITA (opr)	IND,X	4
A6	ff	LDAA (opr)	IND,X	4
A7	ff	STAA (opr)	IND,X	4
A8	ff	EORA (opr)	IND,X	4
A9	ff	ADCA (opr)	IND,X	4
AA	ff	ORAA (opr)	IND,X	4
AB	ff	ADDA (opr)	IND,X	4
AC	ff	CPX (opr)	IND,X	6
AD	ff	JSR (opr)	IND,X	6
AE	ff	LDS (opr)	IND,X	5
AF	ff	STS (opr)	IND,X	5
B0	hh ll	SUBA (opr)	EXT	4
B1	hh ll	CMPA (opr)	EXT	4
B2	hh ll	SBCA (opr)	EXT	4
B3	hh ll	SUBD (opr)	EXT	6
B4	hh ll	ANDA (opr)	EXT	4
B5	hh ll	BITA (opr)	EXT	4
B6	hh ll	LDAA (opr)	EXT	4

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
B7	hh ll	STAA (opr)	EXT	4
B8	hh ll	EORA (opr)	EXT	4
B9	hh ll	ADCA (opr)	EXT	4
BA	hh ll	ORAA (opr)	EXT	4
BB	hh ll	ADDA (opr)	EXT	4
BC	hh ll	CPX (opr)	EXT	6
BD	hh ll	JSR (opr)	EXT	6
BE	hh ll	LDS (opr)	EXT	5
BF	hh ll	STS (opr)	EXT	5
C0	ii	SUBB (opr)	IMM	2
C1	ii	CMPB (opr)	IMM	2
C2	ii	SBCB (opr)	IMM	2
C3	jj kk	ADDD (opr)	IMM	4
C4	ii	ANDB (opr)	IMM	2
C5	ii	BITB (opr)	IMM	2
C6	ii	LDAB (opr)	IMM	2
C8	ii	EORB (opr)	IMM	2
C9	ii	ADCB (opr)	IMM	2
CA	ii	ORAB (opr)	IMM	2
CB	ii	ADDB (opr)	IMM	2
CC	jj kk	LDD (opr)	IMM	3
CD		(Page 4 Switch)		
CE	jj kk	LDX (opr)	IMM	3
CF		STOP	INH	2
D0	dd	SUBB (opr)	DIR	3
D1	dd	CMPB (opr)	DIR	3
D2	dd	SBCB (opr)	DIR	3
D3	dd	ADDD (opr)	DIR	5
D4	dd	ANDB (opr)	DIR	3
D5	dd	BITB (opr)	DIR	3
D6	dd	LDAB (opr)	DIR	3
D7	dd	STAB (opr)	DIR	3
D8	dd	EORB (opr)	DIR	3
D9	dd	ADCB (opr)	DIR	3
DA	dd	ORAB (opr)	DIR	3
DB	dd	ADDB (opr)	DIR	3
DC	dd	LDD (opr)	DIR	4
DD	dd	STD (opr)	DIR	4
DE	dd	LDX (opr)	DIR	4
DF	dd	STX (opr)	DIR	4
E0	ff	SUBB (opr)	IND,X	4
E1	ff	CMPB (opr)	IND,X	4
E2	ff	SBCB (opr)	IND,X	4
E3	ff	ADDD (opr)	IND,X	6

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
E4	ff	ANDB (opr)	IND,X	4
E5	ff	BITB (opr)	IND,X	4
E6	ff	LDAB (opr)	IND,X	4
E7	ff	STAB (opr)	IND,X	4
E8	ff	EORB (opr)	IND,X	4
E9	ff	ADCB (opr)	IND,X	4
EA	ff	ORAB (opr)	IND,X	4
EB	ff	ADDB (opr)	IND,X	4
EC	ff	LDD (opr)	IND,X	5
ED	ff	STD (opr)	IND,X	5
EE	ff	LDX (opr)	IND,X	5
EF	ff	STX (opr)	IND,X	5
F0	hh ll	SUBB (opr)	EXT	4
F1	hh ll	CMPB (opr)	EXT	4
F2	hh ll	SBCB (opr)	EXT	4
F3	hh ll	ADDD (opr)	EXT	6
F4	hh ll	ANDB (opr)	EXT	4
F5	hh ll	BITB (opr)	EXT	4
F6	hh ll	LDAB (opr)	EXT	4
F7	hh ll	STAB (opr)	EXT	4
F8	hh ll	EORB (opr)	EXT	4
F9	hh ll	ADCB (opr)	EXT	4
FA	hh ll	ORAB (opr)	EXT	4
FB	hh ll	ADDB (opr)	EXT	4
FC	hh ll	LDD (opr)	EXT	5
FD	hh ll	STD (opr)	EXT	5
FE	hh ll	LDX (opr)	EXT	5
FF	hh ll	STX (opr)	EXT	5
18 08		INY	INH	4
18 09		DEY	INH	4
18 1C	ff mm	BSET (opr) (msk)	IND,Y	8
18 1D	ff mm	BCLR (opr) (msk)	IND,Y	8
18 1E	ff mm rr	BRSET (opr) (msk) (rel)	IND,Y	8
18 1F	ff mm rr	BRCLR (opr) (msk) (rel)	IND,Y	8
18 30		TSY	INH	4
18 35		TYS	INH	4
18 38		PULY	INH	6
18 3A		ABY	INH	4

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
18 3C		PSHY	INH	5
18 60	ff	NEG (opr)	IND,Y	7
18 63	ff	COM (opr)	IND,Y	7
18 64	ff	LSR (opr)	IND,Y	7
18 66	ff	ROR (opr)	IND,Y	7
18 67	ff	ASR (opr)	IND,Y	7
18 68	ff	ASL/LSL (opr)	IND,Y	7
18 69	ff	ROL (opr)	IND,Y	7
18 6A	ff	DEC (opr)	IND,Y	7
18 6C	ff	INC (opr)	IND,Y	7
18 6D	ff	TST (opr)	IND,Y	7
18 6E	ff	JMP (opr)	IND,Y	4
18 6F	ff	CLR (opr)	IND,Y	7
18 8C	jj kk	CPY (opr)	IMM	5
18 8F		XGDY	INH	4
18 9C	dd	CPY (opr)	DIR	6
18 A0	ff	SUBA (opr)	IND,Y	5
18 A1	ff	CMPA (opr)	IND,Y	5
18 A2	ff	SBCA (opr)	IND,Y	5
18 A3	ff	SUBD (opr)	IND,Y	7
18 A4	ff	ANDA (opr)	IND,Y	5
18 A5	ff	BITA (opr)	IND,Y	5
18 A6	ff	LDAA (opr)	IND,Y	5
18 A7	ff	STAA (opr)	IND,Y	5
18 A8	ff	EORA (opr)	IND,Y	5
18 A9	ff	ADCA (opr)	IND,Y	5
18 AA	ff	ORAA (opr)	IND,Y	5
18 AB	ff	ADDA (opr)	IND,Y	5
18 AC	ff	CPY (opr)	IND,Y	7
18 AD	ff	JSR (opr)	IND,Y	7
18 AE	ff	LDS (opr)	IND,Y	6
18 AF	ff	STS (opr)	IND,Y	6
18 BC	hh ll	CPY (opr)	EXT	7
18 CE	jj kk	LDY (opr)	IMM	4
18 DE	dd	LDY (opr)	DIR	5
18 DF	dd	STY (opr)	DIR	5
18 E0	ff	SUBB (opr)	IND,Y	5
18 E1	ff	CMPB (opr)	IND,Y	5
18 E2	ff	SBCB (opr)	IND,Y	5
18 E3	ff	ADDD (opr)	IND,Y	5
18 E4	ff	ANDB (opr)	IND,Y	5
18 E5	ff	BITB (opr)	IND,Y	5
18 E6	ff	LDAB (opr)	IND,Y	5
18 E7	ff	STAB (opr)	IND,Y	5

Opcode/Instruction Cross Reference

Opcode	Operands	Instruction	Add. Mode	Cycle
18 E8	ff	EORB (opr)	IND,Y	5
18 E9	ff	ADCB (opr)	IND,Y	5
18 EA	ff	ORAB (opr)	IND,Y	5
18 EB	ff	ADDB (opr)	IND,Y	5
18 EC	ff	LDD (opr)	IND,Y	6
18 ED	ff	STD (opr)	IND,Y	6
18 EE	ff	LDY (opr)	IND,Y	6
18 EF	ff	STY (opr)	IND,Y	6
18 FE	hh ll	LDY (opr)	EXT	6
18 FF	hh ll	STY (opr)	EXT	6
1A 83	jj kk	CPD (opr)	IMM	5
1A 93	dd	CPD (opr)	DIR	6
1A A3	ff	CPD (opr)	IND,X	7
1A AC	ff	CPY (opr)	IND,X	7
1A B3	hh ll	CPD (opr)	EXT	7
1A EE	ff	LDY (opr)	IND,X	6
1A EF	ff	STY (opr)	IND,X	6
CD A3	ff	CPD (opr)	IND,Y	7
CD AC	ff	CPX (opr)	IND,Y	7
CD EE	ff	LDX (opr)	IND,Y	6
CD EF	ff	STX (opr)	IND,Y	6

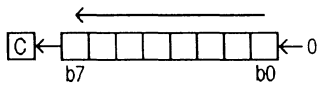
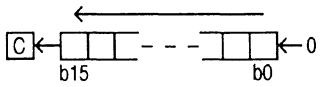
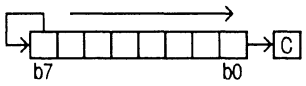
NOTES:

Operands:

- dd = 8-bit direct address $0000–$00FF. (High byte assumed to be $00.)
- ff = 8-bit positive offset $00 (0) to $FF (255) added to index.
- hh = High order byte of 16-bit extended address.
- ii = One byte of immediate data.
- jj = High order byte of 16-bit immediate data.
- kk = Low order byte of 16-bit immediate data.
- ll = Low order byte of 16-bit extended address.
- mm = 8-bit mask (set bits to be affected).
- rr = Signed relative offset $80 (–128) to $7F (+127). Offset relative to the address following the machine code offset byte.

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B → A	INH	1B		1	2	—	—	Δ	—	Δ	Δ	Δ	Δ
ABX	Add B to X	IX + 00:B → IX	INH	3A		1	3	—	—	—	—	—	—	—	—
ABY	Add B to Y	IY + 00:B → IY	INH	18 3A		2	4	—	—	—	—	—	—	—	—
ADCA (opr)	Add with Carry to A	A + M + C → A	A IMM	89	ii	2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A DIR	99	dd	2	3								
			A EXT	B9	hh ll	3	4								
			A IND,X	A9	ff	2	4								
			A IND,Y	18 A9	ff	3	5								
ADCB (opr)	Add with Carry to B	B + M + C → B	B IMM	C9	ii	2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B DIR	D9	dd	2	3								
			B EXT	F9	hh ll	3	4								
			B IND,X	E9	ff	2	4								
			B IND,Y	18 E9	ff	3	5								
ADDA (opr)	Add Memory to A	A + M → A	A IMM	8B	ii	2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A DIR	9B	dd	2	3								
			A EXT	BB	hh ll	3	4								
			A IND,X	AB	ff	2	4								
			A IND,Y	18 AB	ff	3	5								

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
ADDB (opr)	Add Memory to B	B + M → B	B IMM	CB	ii	2	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B DIR	DB	dd	2	3								
			B EXT	FB	hh ll	3	4								
			B IND,X	EB	ff	2	4								
			B IND,Y	18 EB	ff	3	5								
ADDD (opr)	Add 16-Bit to D	D + M:M + 1 → D	IMM	C3	jj kk	3	4	—	—	—	—	Δ	Δ	Δ	Δ
			DIR	D3	dd	2	5								
			EXT	F3	hh ll	3	6								
			IND,X	E3	ff	2	6								
			IND,Y	18 E3	ff	3	7								
ANDA (opr)	AND A with Memory	A • M → A	A IMM	84	ii	2	2	—	—	—	—	Δ	Δ	0	—
			A DIR	94	dd	2	3								
			A EXT	B4	hh ll	3	4								
			A IND,X	A4	ff	2	4								
			A IND,Y	18 A4	ff	3	5								
ANDB (opr)	AND B with Memory	B • M → B	B IMM	C4	ii	2	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D4	dd	2	3								
			B EXT	F4	hh ll	3	4								
			B IND,X	E4	ff	2	4								
			B IND,Y	18 E4	ff	3	5								

ASL	(opr)	Arithmetic Shift Left			EXT IND,X IND,Y A INH B INH	78 68 18 68 48 58	hh ll ff ff		3 2 3 1 1	6 6 7 2 2	—	—	—	—	Δ	Δ	Δ	Δ
ASLD		Arithmetic Shift Left Double			INH	05			1	3	—	—	—	—	Δ	Δ	Δ	Δ
ASR	(opr)	Arithmetic Shift Right			EXT IND,X IND,Y A INH B INH	77 67 18 67 47 57	hh ll ff ff		3 2 3 1 1	6 6 7 2 2	—	—	—	—	Δ	Δ	Δ	Δ
BCC	(rel)	Branch if Carry Clear	? C = 0		REL	24	rr		2	3	—	—	—	—	—	—	—	—
BCLR	(opr) (msk)	Clear Bit(s)	M • (mm) → M		DIR IND,X IND,Y	15 1D 18 1D	dd mm ff mm ff mm		3 3 4	6 7 8	—	—	—	—	Δ	Δ	0	—
BCS	(rel)	Branch if Carry Set	? C = 1		REL	25	rr		2	3	—	—	—	—	—	—	—	—
BEQ	(rel)	Branch if = Zero	? Z = 1		REL	27	rr		2	3	—	—	—	—	—	—	—	—
BGE	(rel)	Branch if ≥ Zero	? N ⊕ V = 0		REL	2C	rr		2	3	—	—	—	—	—	—	—	—
BGT	(rel)	Branch if > Zero	? Z + (N ⊕ V) = 0		REL	2E	rr		2	3	—	—	—	—	—	—	—	—
BHI	(rel)	Branch if Higher	? C + Z = 0		REL	22	rr		2	3	—	—	—	—	—	—	—	—
BHS	(rel)	Branch if Higher or Same	? C = 0		REL	24	rr		2	3	—	—	—	—	—	—	—	—

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
BITA (opr)	Bit(s) Test A with Memory	A • M	A IMM	85	ii	2	2	—	—	—	—	Δ	Δ	0	—
			A DIR	95	dd	2	3								
			A EXT	B5	hh ll	3	4								
			A IND,X	A5	ff	2	4								
			A IND,Y	18 A5	ff	3	5								
BITB (opr)	Bit(s) Test B with Memory	B • M	B IMM	C5	ii	2	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D5	dd	2	3								
			B EXT	F5	hh ll	3	4								
			B IND,X	E5	ff	2	4								
			B IND,Y	18 E5	ff	3	5								
BLE (rel)	Branch if ≤ Zero	? Z + (N ⊕ V) = 1	REL	2F	rr	2	3	—	—	—	—	—	—	—	—
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	2	3	—	—	—	—	—	—	—	—
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	2	3	—	—	—	—	—	—	—	—
BLT (rel)	Branch if < Zero	? N ⊕ V = 1	REL	2D	rr	2	3	—	—	—	—	—	—	—	—
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	2	3	—	—	—	—	—	—	—	—
BNE (rel)	Branch if Not = Zero	? Z = 0	REL	26	rr	2	3	—	—	—	—	—	—	—	—
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	2	3	—	—	—	—	—	—	—	—
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	2	3	—	—	—	—	—	—	—	—

BRCLR	(opr) (msk) (rel)	Branch if Bit(s) Clear	? M • mm = 0		DIR IND,X IND,Y	13 1F 18 1F	dd ff ff	mm mm mm	rr rr rr	4 4 5	6 7 8	—	—	—	—	—	—	—	—
BRN	(rel)	Branch Never	? 1 = 0		REL	21	rr			2	3	—	—	—	—	—	—	—	—
BRSET	(opr) (msk) (rel)	Branch if Bit(s) Set	? (M) • mm = 0		DIR IND,X IND,Y	12 1E 18 1E	dd ff ff	mm mm mm	rr rr rr	4 4 5	6 7 8	—	—	—	—	—	—	—	—
BSET	(opr) (msk)	Set Bit(s)	M + mm → M		DIR IND,X IND,Y	14 1C 18 1C	dd ff ff	mm mm mm		3 3 4	6 7 8	—	—	—	—	Δ	Δ	0	—
BSR	(rel)	Branch to Subroutine	See Special Ops		REL	8D	rr			2	6	—	—	—	—	—	—	—	—
BVC	(rel)	Branch if Overflow Clear	? V = 0		REL	28	rr			2	3	—	—	—	—	—	—	—	—
BVS	(rel)	Branch if Overflow Set	? V = 1		REL	29	rr			2	3	—	—	—	—	—	—	—	—
CBA		Compare A to B	A – B		INH	11				1	2	—	—	—	—	Δ	Δ	Δ	Δ
CLC		Clear Carry Bit	0 → C		INH	0C				1	2	—	—	—	—	—	—	—	0
CLI		Clear Interrupt Mask	0 → I		INH	0E				1	2	—	—	—	0	—	—	—	—
CLR	(opr)	Clear Memory Byte	0 → M		EXT IND,X IND,Y	7F 6F 18 6F	hh ff ff	ll		3 2 3	6 6 7	—	—	—	—	0	1	0	0
CLRA		Clear Accumulator A	0 → A	A	INH	4F				1	2	—	—	—	—	0	1	0	0

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
CLRB	Clear Accumulator B	0 → B	B INH	5F		1	2	—	—	—	—	0	1	0	0
CLV	Clear Overflow Flag	0 → V	INH	0A		1	2	—	—	—	—	—	—	0	—
CMPA (opr)	Compare A to Memory	A – M	A IMM	81	ii	2	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	91	dd	2	3								
			A EXT	B1	hh ll	3	4								
			A IND,X	A1	ff	2	4								
			A IND,Y	18 A1	ff	3	5								
CMPB (opr)	Compare B to Memory	B – M	B IMM	C1	ii	2	2	—	—	—	—	Δ	Δ	Δ	Δ
			B DIR	D1	dd	2	3								
			B EXT	F1	hh ll	3	4								
			B IND,X	E1	ff	2	4								
			B IND,Y	18 E1	ff	3	5								
COM (opr)	1's Complement Memory Byte	$FF – M → M	EXT	73	hh ll	3	6	—	—	—	—	Δ	Δ	0	1
			IND,X	63	ff	2	6								
			IND,Y	18 63	ff	3	7								
COMA	1's Complement A	$FF – A → A	A INH	43		1	2	—	—	—	—	Δ	Δ	0	1
COMB	1's Complement B	$FF – B → B	B INH	53		1	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M:M + 1	IMM	1A 83	jj kk	4	5	—	—	—	—	Δ	Δ	Δ	Δ
			DIR	1A 93	dd	3	6								
			EXT	1A B3	hh ll	4	7								
			IND,X	1A A3	ff	3	7								
			IND,Y	CD A3	ff	3	7								

CPX (opr)	Compare X to Memory 16-Bit	IX – M:M + 1		IMM DIR EXT IND,X IND,Y	8C 9C BC AC CD AC	jj kk dd hh ll ff ff		3 2 3 2 3	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
CPY (opr)	Compare Y to Memory 16-Bit	IY – M:M + 1		IMM DIR EXT IND,X IND,Y	18 8C 18 9C 18 BC 1A AC 18 AC	jj kk dd hh ll ff ff		4 3 4 3 3	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
DAA	Decimal Adjust A	Adjust Sum to BCD		INH	19			1	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 → M		EXT IND,X IND,Y	7A 6A 18 6A	hh ll ff ff		3 2 3	6 6 7	—	—	—	—	Δ	Δ	Δ	—
DECA	Decrement Accumulator A	A – 1 → A	A	INH	4A			1	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 → B	B	INH	5A			1	2	—	—	—	—	Δ	Δ	Δ	—
DES	Decrement Stack Pointer	SP – 1 → SP		INH	34			1	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 → IX		INH	09			1	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 → IY		INH	18 09			2	4	—	—	—	—	—	Δ	—	—

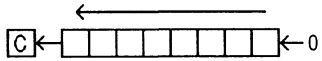
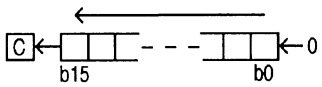
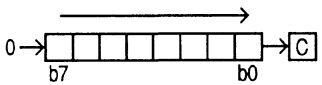
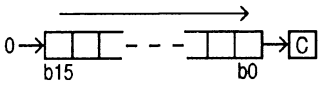
[redacted]

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
EORA (opr)	Exclusive OR A with Memory	A ⊕ M → A	A IMM	88	ii	2	2	—	—	—	—	Δ	Δ	0	—
			A DIR	98	dd	2	3								
			A EXT	B8	hh ll	3	4								
			A IND,X	A8	ff	2	4								
			A IND,Y	18 A8	ff	3	5								
EORB (opr)	Exclusive OR B with Memory	B ⊕ M → B	B IMM	C8	ii	2	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D8	dd	2	3								
			B EXT	F8	hh ll	3	4								
			B IND,X	E8	ff	2	4								
			B IND,Y	18 E8	ff	3	5								
FDIV	Fractional Divide 16 by 16	D/IX → IX; r → D	INH	03		1	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D/IX → IX; r → D	INH	02		1	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 → M	EXT	7C	hh ll	3	6	—	—	—	—	Δ	Δ	Δ	—
			IND,X	6C	ff	2	6								
			IND,Y	18 6C	ff	3	7								
INCA	Increment Accumulator A	A + 1 → A	A INH	4C		1	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	B + 1 → B	B INH	5C		1	2	—	—	—	—	Δ	Δ	Δ	—

INS		Increment Stack Pointer	SP + 1 → SP		INH	31		1	3	—	—	—	—	—	—	—	—
INX		Increment Index Register X	IX + 1 → IX		INH	08		1	3	—	—	—	—	—	Δ	—	—
INY		Increment Index Register Y	IY + 1 → IY		INH	18 08		2	4	—	—	—	—	—	Δ	—	—
JMP	(opr)	Jump	See Special Ops		EXT	7E	hh ll	3	3	—	—	—	—	—	—	—	—
					IND,X	6E	ff	2	3								
					IND,Y	18 6E	ff	3	4								
JSR	(opr)	Jump to Subroutine	See Special Ops		DIR	9D	dd	2	5	—	—	—	—	—	—	—	—
					EXT	BD	hh ll	3	6								
					IND,X	AD	ff	2	6								
					IND,Y	18 AD	ff	3	7								
LDAA	(opr)	Load Accumulator A	M → A	A	IMM	86	ii	2	2	—	—	—	—	Δ	Δ	0	—
				A	DIR	96	dd	2	3								
				A	EXT	B6	hh ll	3	4								
				A	IND,X	A6	ff	2	4								
				A	IND,Y	18 A6	ff	3	5								
LDAB	(opr)	Load Accumulator B	M → B	B	IMM	C6	ii	2	2	—	—	—	—	Δ	Δ	0	—
				B	DIR	D6	dd	2	3								
				B	EXT	F6	hh ll	3	4								
				B	IND,X	E6	ff	2	4								
				B	IND,Y	18 E6	ff	3	5								

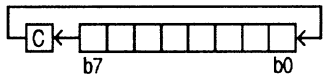
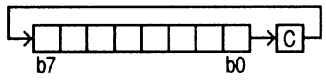
[redacted]

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
LDD (opr)	Load Double Accumulator D	M → A, M + 1 → B	IMM	CC	jj kk	3	3	—	—	—	—	Δ	Δ	0	—
			DIR	DC	dd	2	4								
			EXT	FC	hh ll	3	5								
			IND,X	EC	ff	2	5								
			IND,Y	18 EC	ff	3	6								
LDS (opr)	Load Stack Pointer	M:M + 1 → SP	IMM	8E	jj kk	3	3	—	—	—	—	Δ	Δ	0	—
			DIR	9E	dd	2	4								
			EXT	BE	hh ll	3	5								
			IND,X	AE	ff	2	5								
			IND,Y	18 AE	ff	3	6								
LDX (opr)	Load Index Register X	M:M + 1 → IX	IMM	CE	jj kk	3	3	—	—	—	—	Δ	Δ	0	—
			DIR	DE	dd	2	4								
			EXT	FE	hh ll	3	5								
			IND,X	EE	ff	2	5								
			IND,Y	CD EE	ff	3	6								
LDY (opr)	Load Index Register Y	M:M + 1 → IY	IMM	18 CE	jj kk	4	4	—	—	—	—	Δ	Δ	0	—
			DIR	18 DE	dd	3	5								
			EXT	18 FE	hh ll	4	6								
			IND,X	1A EE	ff	3	6								
			IND,Y	18 EE	ff	3	6								

LSL (opr)	Logical Shift Left			EXT IND,X IND,Y A INH B INH	78 68 18 68 48 58	hh ll ff ff		3 2 3 1 1	6 6 7 2 2	—	—	—	—	Δ	Δ	Δ	Δ
LSLD	Logical Shift Left Double			INH	05			1	3	—	—	—	—	Δ	Δ	Δ	Δ
LSR (opr)	Logical Shift Right			EXT IND,X IND,Y A INH B INH	74 64 18 64 44 54	hh ll ff ff		3 2 3 1 1	6 6 7 2 2	—	—	—	—	0	Δ	Δ	Δ
LSRD	Logical Shift Right Double			INH	04			1	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A × B → D		INH	3D			1	10	—	—	—	—	—	—	—	Δ
NEG (opr)	2's Complement Memory Byte	0 – M → M		EXT IND,X IND,Y	70 60 18 60	hh ll ff ff		3 2 3	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
NEGA	2's Complement A	0 – A → A	A	INH	40			1	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	2's Complement B	0 – B → B	B	INH	50			1	2	—	—	—	—	Δ	Δ	Δ	Δ
NOP	No Operation	No Operation		INH	01			1	2	—	—	—	—	—	—	—	—

[redacted]

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
ORAA (opr)	OR Accumulator A (Inclusive)	A + M → A	A IMM	8A	ii	2	2	—	—	—	—	Δ	Δ	0	—
			A DIR	9A	dd	2	3								
			A EXT	BA	hh ll	3	4								
			A IND,X	AA	ff	2	4								
			A IND,Y	18 AA	ff	3	5								
ORAB (opr)	OR Accumulator B (Inclusive)	B + M → B	B IMM	CA	ii	2	2	—	—	—	—	Δ	Δ	0	—
			B DIR	DA	dd	2	3								
			B EXT	FA	hh ll	3	4								
			B IND,X	EA	ff	2	4								
			B IND,Y	18 EA	ff	3	5								
PSHA	Push A onto Stack	A ↑ Stk, SP = SP – 1	A INH	36		1	3	—	—	—	—	—	—	—	—
PSHB	Push B onto Stack	B ↑ Stk, SP = SP – 1	B INH	37		1	3	—	—	—	—	—	—	—	—
PSHX	Push X onto Stack (Lo First)	IX ↑ Stk, SP = SP – 2	INH	3C		1	4	—	—	—	—	—	—	—	—
PSHY	Push Y onto Stack (Lo First)	IY ↑Stk, SP = SP – 2	INH	18 3C		2	5	—	—	—	—	—	—	—	—
PULA	Pull A from Stack	SP = SP + 1, A ↓ Stk	A INH	32		1	4	—	—	—	—	—	—	—	—
PULB	Pull B from Stack	SP = SP + 1, B ↓ Stk	B INH	33		1	4	—	—	—	—	—	—	—	—
PULX	Pull X from Stack (Hi First)	SP = SP + 2, IX ↓ Stk	INH	38		1	5	—	—	—	—	—	—	—	—

PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY ↓ Stk		INH	18 38		2	6	—	—	—	—	—	—	—	—
ROL (opr)	Rotate Left			EXT	79	hh ll	3	6	—	—	—	—	Δ	Δ	Δ	Δ
				IND,X	69	ff	2	6								
				IND,Y	18 69	ff	3	7								
			A	INH	49		1	2								
			B	INH	59		1	2								
ROR (opr)	Rotate Right			EXT	76	hh ll	3	6	—	—	—	—	Δ	Δ	Δ	Δ
				IND,X	66	ff	2	6								
				IND,Y	18 66	ff	3	7								
			A	INH	46		1	2								
			B	INH	56		1	2								
RTI	Return from Interrupt	See Special Ops		INH	3B		1	12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	Return from Subroutine	See Special Ops		INH	39		1	5	—	—	—	—	—	—	—	—
SBA	Subtract B from A	A – B → A		INH	10		1	2	—	—	—	—	Δ	Δ	Δ	Δ
SBCA (opr)	Subtract with Carry from A	A – M – C → A	A	IMM	82	ii	2	2	—	—	—	—	Δ	Δ	Δ	Δ
			A	DIR	92	dd	2	3								
			A	EXT	B2	hh ll	3	4								
			A	IND,X	A2	ff	2	4								
			A	IND,Y	18 A2	ff	3	5								
SBCB (opr)	Subtract with Carry from B	B – M – C → B	B	IMM	C2	ii	2	2	—	—	—	—	Δ	Δ	Δ	Δ
			B	DIR	D2	dd	2	3								
			B	EXT	F2	hh ll	3	4								
			B	IND,X	E2	ff	2	4								
			B	IND,Y	18 E2	ff	3	5								

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
SEC	Set Carry	1 → C	INH	0D		1	2	—	—	—	—	—	—	—	1
SEI	Set Interrupt Mask	1 → I	INH	0F		1	2	—	—	—	1	—	—	—	—
SEV	Set Overflow Flag	1 → V	INH	0B		1	2	—	—	—	—	—	—	1	—
STAA (opr)	Store Accumulator A	A → M	A DIR	97	dd	2	3	—	—	—	—	Δ	Δ	0	—
			A EXT	B7	hh ll	3	4								
			A IND,X	A7	ff	2	4								
			A IND,Y	18 A7	ff	3	5								
STAB (opr)	Store Accumulator B	B → M	B DIR	D7	dd	2	3	—	—	—	—	Δ	Δ	0	—
			B EXT	F7	hh ll	3	4								
			B IND,X	E7	ff	2	4								
			B IND,Y	18 E7	ff	3	5								
STD (opr)	Store Accumulator D	A → M, B → M + 1	DIR	DD	dd	2	4	—	—	—	—	Δ	Δ	0	—
			EXT	FD	hh ll	3	5								
			IND,X	ED	ff	2	5								
			IND,Y	18 ED	ff	3	6								
STOP	Stop Internal Clocks		INH	CF		1	2	—	—	—	—	—	—	—	—
STS (opr)	Store Stack Pointer	SP → M:M + 1	DIR	9F	dd	2	4	—	—	—	—	Δ	Δ	0	—
			EXT	BF	hh ll	3	5								
			IND,X	AF	ff	2	5								
			IND,Y	18 AF	ff	3	6								

STX (opr)	Store Index Register X	IX → M:M + 1		DIR	DF	dd		2	4	—	—	—	—	Δ	Δ	0	—
				EXT	FF	hh	ll	3	5								
				IND,X	EF	ff		2	5								
				IND,Y	CD EF	ff		3	6								
STY (opr)	Store Index Register Y	IY → M:M + 1		DIR	18 DF	dd		3	5	—	—	—	—	Δ	Δ	0	—
				EXT	18 FF	hh	ll	4	6								
				IND,X	1A EF	ff		3	6								
				IND,Y	18 EF	ff		3	6								
SUBA (opr)	Subtract Memory from A	A – M → A	A	IMM	80	ii		2	2	—	—	—	—	Δ	Δ	Δ	Δ
			A	DIR	90	dd		2	3								
			A	EXT	B0	hh	ll	3	4								
			A	IND,X	A0	ff		2	4								
			A	IND,Y	18 A0	ff		3	5								
SUBB (opr)	Subtract Memory from B	B – M → B	B	IMM	C0	ii		2	2	—	—	—	—	Δ	Δ	Δ	Δ
			B	DIR	D0	dd		2	3								
			B	EXT	F0	hh	ll	3	4								
			B	IND,X	E0	ff		2	4								
			B	IND,Y	18 E0	ff		3	5								
SUBD (opr)	Subtract Memory from D	D – M:M + 1 → D		IMM	83	jj	kk	3	4	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	93	dd		2	5								
				EXT	B3	hh	ll	3	6								
				IND,X	A3	ff		2	6								
				IND,Y	18 A3	ff		3	7								
SWI	Software Interrupt	See Special Ops		INH	3F			1	14	—	—	—	1	—	—	—	—
TAB	Transfer A to B	A → B		INH	16			1	2	—	—	—	—	Δ	Δ	0	—
TAP	Transfer A to CCR	A → CCR		INH	06			1	2	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ

Source Forms	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Bytes	Cycles	Condition Codes S	X	H	I	N	Z	V	C
TBA	Transfer B to A	B → A	INH	17		1	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00		1	*	—	—	—	—	—	—	—	—
TPA	Transfer CC Register to A	CCR → A	INH	07		1	2	—	—	—	—	—	—	—	—
TST (opr)	Test for Zero or Minus	M – 0	EXT IND,X IND,Y	7D 6D 18 6D	hh ll ff ff	3 2 3	6 6 7	—	—	—	—	Δ	Δ	0	0
TSTA		A – 0	A INH	4D		1	2	—	—	—	—	Δ	Δ	0	0
TSTB		B – 0	B INH	5D		1	2	—	—	—	—	Δ	Δ	0	0
TSX	Transfer Stack Pointer to X	SP + 1 → IX	INH	30		1	3	—	—	—	—	—	—	—	—
TSY	Transfer Stack Pointer to Y	SP + 1 → IY	INH	18 30		2	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX – 1 → SP	INH	35		1	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY – 1 → SP	INH	18 35		2	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs and WAIT	INH	3E		1	**	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX → D, D → IX	INH	8F		1	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY → D, D → IY	INH	18 8F		2	4	—	—	—	—	—	—	—	—

NOTES:

Cycle:

*	=	Infinity or until reset occurs
**	=	12 cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MCU E-clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (total = 14 + n).

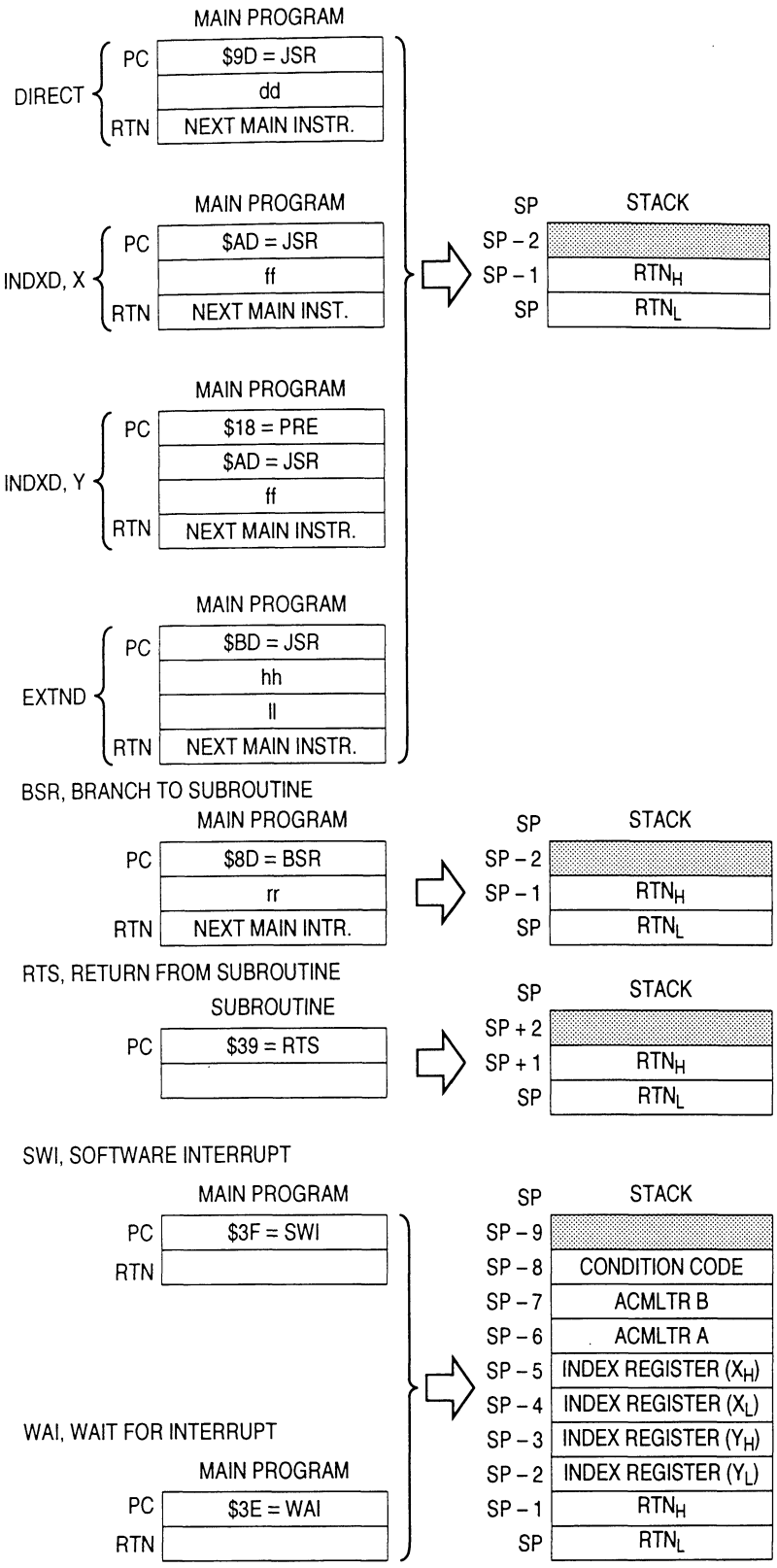
Operands:

dd	=	8-bit direct address $0000–$00FF. (High byte assumed to be $00.)
ff	=	8-bit positive offset $00 (0) to $FF (255) added to index.
hh	=	High order byte of 16-bit extended address.
ii	=	One byte of immediate data.
jj	=	High order byte of 16-bit immediate data.
kk	=	Low order byte of 16-bit immediate data.
ll	=	Low order byte of 16-bit extended address.
mm	=	8-bit mask (set bits to be affected).
rr	=	Signed relative offset $80 (–128) to $7F (+ 127). Offset relative to the address following the machine code offset byte.

Condition Codes:

—	=	Bit not changed
0	=	Always cleared (logic 0).
1	=	Always set (logic 1).
Δ	=	Bit cleared or set depending on operation.
↓	=	Bit may be cleared, cannot become set.

Special Operations



BSR, BRANCH TO SUBROUTINE

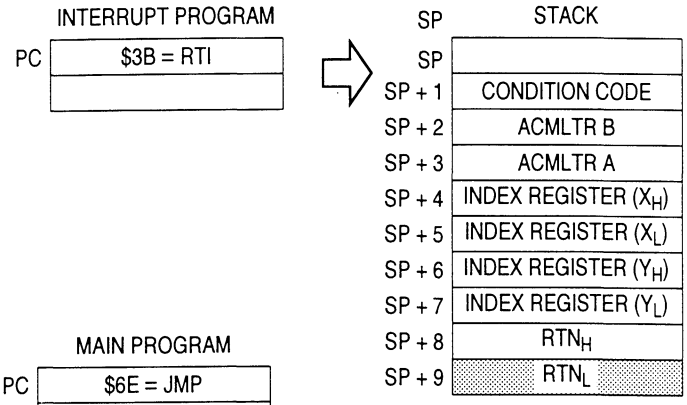
RTS, RETURN FROM SUBROUTINE

SWI, SOFTWARE INTERRUPT

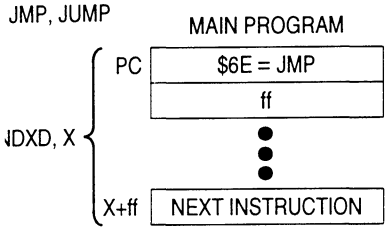
WAI, WAIT FOR INTERRUPT

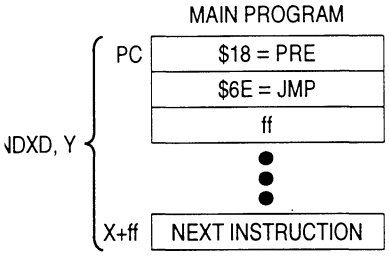
Special Operations

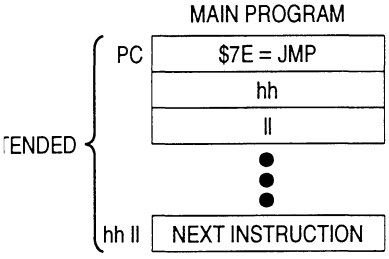
RTI, RETURN FROM INTERRUPT



JMP, JUMP







EGEND

RTN = Address of next instruction in main program to be executed upon return from subroutine

RTN_H = Most significant byte of return address

RTN_L = Least significant byte of return address

▒ = Stack pointer location after execution

dd = 8-Bit direct address ($0000–$00FF) (high byte assumed to be $00)

ff = 8-Bit positive offset $00 (0) to $FF (256) (is added to index)

hh = High order byte of 16-bit extended address

ll = Low order byte of 16-bit extended address

rr = Signed relative offset $80 (–128) to $7F (+127) (offset relative to the address following the machine code offset byte)

M68HC11 E Series Registers (1 of 2)

The 128-byte register block can be remapped to any 4K boundary.

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001									Reserved
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006									Reserved
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	—	—	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	—	—	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (Hi)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Lo)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (Hi)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Lo)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (Hi)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Lo)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (Hi)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Lo)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (Hi)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Lo)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (Hi)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Lo)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (Hi)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Lo)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (Hi)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Lo)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (Hi)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Lo)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2

M68HC11 E Series Registers (2 of 2)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	—	—	—	—	TFLG2
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	—	MODF	—	—	—	—	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	SCP2[1]	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	—	M	WAKE	—	—	—	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	—	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	—	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035	—	—	—	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$1036	MBE	—	ELAT	EXCOL	EXROW	T1	T0	PGM	EPROG[2]
$1037									Reserved
$1038									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	—	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	ELAT[3]	BYTE	ROW	ERASE	EELAT	EPGM	PPROG
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	—	OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1
$103F	EE3[4]	EE2[4]	EE1[4]	EE0[4]	NOSEC	NOCOP	ROMON[5]	EEON	CONFIG

1. MC68HC(7)11E20 only
2. MC68HC711E20 only
3. MC68HC711E9 and MC68S711E9 only
4. MC68HC811E2 only
5. Not applicable to MC68HC811E2. For devices with disabled ROM array (MC68HC11E0, MC68HC11E1, MC68L11E0, or MC68L11E1) this bit must never be set to one.

ADCTL

A/D Control/Status

	Bit 7	6	5	4	3	2	1	Bit 0
$1030	CCF	—	SCAN	MULT	CD	CC	CB	CA
RESET:	1	0	1	1	1	1	1	1

CCF — Conversions Complete Flag
This bit is set after an A/D conversion cycle and cleared when ADCTL is written.
Bit 6 — Not implemented; always reads zero
SCAN — Continuous Scan Control
0 = Do four conversions and stop
1 = Convert four channels in selected group continuously
MULT — Multiple-Channel/Single-Channel Control
0 = Convert single channel selected
1 = Convert four channels in selected group
CD:CA — Channel Select D through A

Channel Select Control Bits CD:CA	Channel Signal	Result in ADRx if MULT = 1	Result in ADRx if MULT = 0
0 0 0 0	AD0	ADR1	ADR[4:1]
0 0 0 1	AD1	ADR2	ADR[4:1]
0 0 1 0	AD2	ADR3	ADR[4:1]
0 0 1 1	AD3	ADR4	ADR[4:1]
0 1 0 0	AD4	ADR1	ADR[4:1]
0 1 0 1	AD5	ADR2	ADR[4:1]
0 1 1 0	AD6	ADR3	ADR[4:1]
0 1 1 1	AD7	ADR4	ADR[4:1]
1 0 X X	Reserved	—	—
1 1 0 0	V_{RH}*	ADR1	ADR[4:1]
1 1 0 1	V_{RL}*	ADR2	ADR[4:1]
1 1 1 0	(V_{RH})/2*	ADR3	ADR[4:1]
1 1 1 1	Test/Reserved*	ADR4	ADR[4:1]

*Used for factory testing only

ADR1–ADR4

A/D Results

$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
%[1]	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts[2]	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195
Volts[3]	1.65	8.25	0.4125	0.2063	0.1031	0.0516	0.0258	0.0129

1. % of V_{RH}–V_{RL} 2. Voltages for V_{RL} = 0; V_{RH} = 5.0 V
3. Voltages for V_{RL} = 0; V_{RH} = 3.3 V

Baud Rate Control Register

	Bit 7	6	5	4	3	2	1	Bit 0
$102B	TCLR	SCP2	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)
SCP[2:0] — SCI Baud Rate Prescaler Selects
SCP2 applies to the MC68HC(7)11E20 only. When SCP2 = 1, SCP[1:0] must equal zeros. Any other values for SCP[1:0] are not decoded in the prescaler and the results are unpredictable.

SCP			Divide	Crystal Frequency				
2	1	0	Internal Clock By	4.0 MHz	4.9152 MHz	8.0 MHz	8.3886 MHz	12.0 MHz
0	0	0	1	62500	76800	125000	131072	187500
0	0	1	3	20833	25600	41667	43691	62500
0	1	0	4	15625	19200	31250	32768	46875
0	1	1	13	4800	5907	9600	10082	14423
1	0	0	39	1602	1969	3205	3361	4808

Shaded areas apply to MC68HC(7)11E20 only

RCKB — SCI Baud Rate Clock Check (TEST)
SCR[2:0] — SCI Baud Rate Selects
Selects receiver and transmitter bit rate based on output from baud rate prescaler stage. Refer to SCI baud rate generator block diagram.

SCR [2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table) 131072	76800	32768	19200	4800
0 0 0	1	131072	76800	32768	19200	4800
0 0 1	2	65536	38400	16384	9600	2400
0 1 0	4	32768	19200	8192	4800	1200
0 1 1	8	16384	9600	4096	2400	600
1 0 0	16	8192	4800	2048	1200	300
1 0 1	32	4096	2400	1024	600	150
1 1 0	64	2048	1200	512	300	75
1 1 1	128	1024	600	256	150	37.5

BPROT

Block Protect

	Bit 7	6	5	4	3	2	1	Bit 0
$1035	—	—	—	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET:	0	0	0	1	1	1	1	1

PTCON — Protect for CONFIG

0 = CONFIG register can be programmed or erased normally.

1 = CONFIG register cannot be programmed or erased.

BPRT[3:0] — Block Protect Bits for EEPROM

Block protect register bits can be written to zero (protection disabled) only once within 64 cycles of a reset in normal modes, or at any time in special modes. Block protect register bits can be written to one (protection enabled) at any time.

0 = Protection disabled for associated block

1 = Protection enabled for associated block

Bit Name	Block Protected	Block Size
BPRT0	$B600–$B61F	32 Bytes
BPRT1	$B620–$B65F	64 Bytes
BPRT2	$B660–$B6DF	128 Bytes
BPRT3	$B6E0–$B7FF	288 Bytes

MC68HC811E2 Only

Bit Name	Block Protected	Block Size
BPRT0	$X800–$X9FF*	512 Bytes
BPRT1	$XA00–$XBFF*	512 Bytes
BPRT2	$XC00–$XDFF*	512 Bytes
BPRT3	$XE00–$XFFF*	512 Bytes

*X is determined by value of EE[3:0] in CONFIG (MC68HC811E2 only). Refer to CONFIG register for MC68HC811E2.

CFORC

Timer Compare Force

	Bit 7	6	5	4	3	2	1	Bit 0
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—
RESET:	0	0	0	0	0	0	0	0

FOC[5:1] — Force Output Compare

Write ones to force compare(s)

0 = Not affected

1 = Output x action occurs.

Bits [2:0] — Not implemented; always read zero

Security Disable, COP, ROM Mapping, EEPROM Enables

	Bit 7	6	5	4	3	2	1	Bit 0
$103F	—	—	—	—	NOSEC	NOCOP	ROMON	EEON
RESETS:								
S. Chip:	0	0	0	0	U	U	1	U
Boot:	0	0	0	0	U	U(L)	U	U
Exp.:	0	0	0	0	1	U	U	U
Test:	0	0	0	0	1	U(L)	U	U

MC68HC811E2 Only

	Bit 7	6	5	4	3	2	1	Bit 0
$103F	EE3	EE2	EE1	EE0	NOSEC	NOCOP	—	EEON
RESETS:								
S. Chip:	1	1	1	1	U	U	1	1
Boot:	1	1	1	1	U	U(L)	1	1
Exp.:	U	U	U	U	1	U	1	U
Test:	U	U	U	U	1	U(L)	1	0

U indicates a previously programmed and unaffected bit. U(L) indicates that the bit resets to the logic level held in latch prior to reset but function of COP is controlled by DISR in TEST1 register.

EE[3:0] — EEPROM Map Position (MC68HC811E2 only)
EE[3:0] determine the upper four bits of EEPROM address, positioning EEPROM at the selected 4-Kbyte boundary. In single-chip and boot modes, these bits are set to ones during reset and EEPROM is mapped to top of memory. Not implemented in other E-series devices; always read zero.

EE[3:0]	EEPROM Location
0 0 0 0	$0800–$0FFF
0 0 0 1	$1800–$1FFF
0 0 1 0	$2800–$2FFF
0 0 1 1	$3800–$3FFF
0 1 0 0	$4800–$4FFF
0 1 0 1	$5800–$5FFF
0 1 1 0	$6800–$6FFF
0 1 1 1	$7800–$7FFF
1 0 0 0	$8800–$8FFF
1 0 0 1	$9800–$9FFF
1 0 1 0	$A800–$AFFF
1 0 1 1	$B800–$BFFF
1 1 0 0	$C800–$CFFF
1 1 0 1	$D800–$DFFF
1 1 1 0	$E800–$EFFF
1 1 1 1	$F800–$FFFF

NOSEC — Security Mode Disable

The security feature, a mask option, protects the contents of RAM and EEPROM by restricting the operation of a protected device to single-chip mode. Attempted operation in any other mode while the device is protected forces erasure of all RAM and EEPROM contents. This option must be specified before manufacture. An enhanced security feature that protects EPROM also is available in MC68S711E9.

0 = RAM/EEPROM security mode enabled
1 = RAM/EEPROM security mode disabled

NOCOP — COP System Disable

Resets to programmed value

0 = COP enabled (forces reset on timeout)
1 = COP disabled (does not force reset on timeout)

ROMON — ROM/EPROM Enable

In single-chip mode ROMON is forced to one out of reset. ROMON does not apply to MC68HC811E2. For devices with disabled ROM arrays (the MC68HC11E0, MC68HC11E1, MC68L11E0, or MC68L11E1) ROMON must never be set to one.

0 = ROM/EPROM removed from the memory map
1 = ROM/EPROM present in the memory map

EEON — EEPROM Enable

0 = EEPROM is removed from the memory map
1 = EEPROM is present in the memory map

COPRST

Arm/Reset COP Timer Circuitry

	Bit 7	6	5	4	3	2	1	Bit 0
$103A	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

DDRC

Data Direction Register for Port C

	Bit 7	6	5	4	3	2	1	Bit 0
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C

0 = Input
1 = Output

In handshake output mode, DDRC bits select the three-stated output option (DDCx = 1).

DDRD

Data Direction Register for Port D

	Bit 7	6	5	4	3	2	1	Bit 0
$1009	—	—	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

Bits [7:6] — Not implemented; always read zero
DDD[5:0] — Data Direction for Port D
0 = Input
1 = Output

EPROG

EPROM Programming Control

	Bit 7	6	5	4	3	2	1	Bit 0
$1036	MBE	—	ELAT	EXCOL	EXROW	T1	T0	PGM
RESET:	0	0	0	0	0	0	0	0

NOTE

EPROG is present only on the MC68HC711E20.

MBE — Multiple-Byte Programming Enable
When multiple-byte programming is enabled, address bit 5 is considered a don't care so that bytes with address bit 5 = 0 and address bit 5 = 1 both get programmed. MBE can be read in any mode and always reads zero in normal modes. MBE can only be written in special modes.
0 = EPROM array configured for normal programming
1 = Program two bytes with the same data
Bit 6 — Not implemented; always reads zero
ELAT — EPROM Latch Control
When ELAT = 1, writes to EPROM cause address and data to be latched and the EPROM cannot be read. ELAT can be read any time. ELAT can be written any time except when PGM = 1; then the write to ELAT will be disabled.
0 = EPROM address/data bus configured for normal reads
1 = EPROM address/data bus configured for programming
EXCOL — Select Extra Columns
0 = User array selected
1 = User array disabled; extra columns accessed at bits [7:0]. Addresses use bits [13:5] and bits [4:0] are don't care. EXCOL can only be read in special modes and always returns zero in normal modes. EXCOL can be written in special modes only.
EXROW — Select Extra Rows
0 = User array selected
1 = User array is disabled and two extra rows are available. Addresses use bits [7:0] and bits [13:8] are don't care. EXROW can only be read in special modes and always returns zero in normal modes. EXROW can be written in special modes only.

T[1:0] — EPROM Test Mode Select Bits

T1	T2	Function Selected
0	0	Normal Mode
0	1	Reserved
1	0	Gate Stress
1	1	Drain Stress

These bits allow selection of either gate stress or drain stress test modes. They can be read only in special modes and always read zero in normal modes. T[1:0] can only be written in special modes.

PGM — EPROM Programming Voltage Enable

0 = Programming voltage to EPROM array disconnected

1 = Programming voltage to EPROM array connected

Can be read any time and can only be written when ELAT = 1.

HPRIO

Highest Priority I-Bit Interrupt and Miscellaneous

	Bit 7	6	5	4	3	2	1	Bit 0
$103C	RBOOT*	SMOD*	MDA*	IRVNE*	PSEL3	PSEL2	PSEL1	PSEL0
RESETS:								
Single-Chip	0	0	0	0	0	1	1	0
Expanded	0	0	1	0	0	1	1	0
Bootstrap	1	1	0	0	0	1	1	0
Special Test	0	1	1	1	0	1	1	0

*Reset state depends on mode selected at reset.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set to one (bootstrap or special test mode). Can only be written in special modes.

0 = Bootloader ROM disabled and not in map

1 = Bootloader ROM enabled and in map at $BE00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

The initial value of SMOD is the **inverse** of the logic level present on the MODB pin at the rising edge of reset. The initial value of MDA equals the logic level present on the MODA pin at the rising edge of reset. These two bits can be read at any time. They can be written anytime in special modes. MDA can only be written once in normal modes. SMOD cannot be set once it has been cleared.

Inputs			Latched at Reset	
MODB	MODA	Mode	SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded	0	1
0	0	Bootstrap	1	0
0	1	Special Test	1	1

IRVNE — Internal Read Visibility/Not E (IRV in MC68HC811E2)

IRVNE can be written once in any mode. In expanded modes, IRVNE determines whether IRV is on or off. In special test mode, IRVNE is reset to one. In all other modes, IRVNE is reset to zero. For MC68HC811E2, this bit controls only internal read visibility function and has no meaning or effect in single-chip modes.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out the external data bus.

In single-chip modes this bit determines whether the E clock drives out from the chip.

0 = E is driven out from the chip.

1 = E pin is driven low. Refer to the following table.

NOTE

When IRV function is used, care must be taken to ensure that bus conflicts do not occur. Data can be driven onto the bus even though the R/$\overline{W}$ line indicates a high-impedance state on data bus pins.

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only	IRVNE Can Be Written
Single Chip	0	On	Off	E	Once
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	E	Once
Special Test	1	On	On	IRV	Once

PSEL[3:0] — Priority Select Bit 3 through Bit 0

Can be written only while bit I in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit-related sources.

PSEL[3:0]				Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{IRQ}$)
0	1	1	0	$\overline{IRQ}$ (External Pin)
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5/Input Capture 4

INIT

RAM and Register Mapping

	Bit 7	6	5	4	3	2	1	Bit 0
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	1

RAM[3:0] — Internal RAM Map Position
Determine the upper four bits of RAM address. At reset RAM is mapped to $0000.

REG[3:0] — 64-Byte Register Block Map Position
Determine upper four bits of register space address. At reset registers are mapped to $1000.

RAM[3:0]	Address	REG[3:0]	Address
0000	$0000–$0XFF	0000	$0000–$003F
0001	$1000–$1XFF	0001	$1000–$103F
0010	$2000–$2XFF	0010	$2000–$203F
0011	$3000–$3XFF	0011	$3000–$303F
0100	$4000–$4XFF	0100	$4000–$403F
0101	$5000–$5XFF	0101	$5000–$503F
0110	$6000–$6XFF	0110	$6000–$603F
0111	$7000–$7XFF	0111	$7000–$703F
1000	$8000–$8XFF	1000	$8000–$803F
1001	$9000–$9XFF	1001	$9000–$903F
1010	$A000–$AXFF	1010	$A000–$A03F
1011	$B000–$BXFF	1011	$B000–$B03F
1100	$C000–$CXFF	1100	$C000–$C03F
1101	$D000–$DXFF	1101	$D000–$D03F
1110	$E000–$EXFF	1110	$E000–$E03F
1111	$F000–$FXFF	1111	$F000–$F03F

NOTE

Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

OC1D

Output Compare 1 Data

	Bit 7	6	5	4	3	2	1	Bit 0
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0] — Not implemented; always read zero

OC1M

Output Compare 1 Mask

	Bit 7	6	5	4	3	2	1	Bit 0
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—
RESET:	0	0	0	0	0	0	0	0

OC1M[7:3] — Output Compare Masks
0 = OC1 disabled.
1 = OC1 enabled to control the corresponding pin of port A
Bits [2:0] — Not implemented; always read zero

OPTION

System Configuration Options

	Bit 7	6	5	4	3	2	1	Bit 0
$1039	ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

ADPU — A/D Power-Up
0 = A/D powered down
1 = A/D powered up
CSEL — Clock Select
0 = A/D and EEPROM charge pumps use system E clock
1 = A/D and EEPROM charge pumps use internal RC oscillator
IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
0 = Low level recognition
1 = Falling edge recognition
DLY — Enable Oscillator Start-Up Delay on Exit from STOP
0 = No stabilization delay on exit from STOP
1 = Stabilization delay enabled on exit from STOP
CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset
Bit 2 — Not implemented; always reads zero
CR[1:0] — COP Timer Rate Select

CR [1:0]	Divide E/2^{15} By	XTAL = 4.0 MHz Timeout –0 ms, +32.8 ms	XTAL = 8.0 MHz Timeout –0 ms, +16.4 ms	XTAL = 12.0 MHz Timeout –0 ms, +10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.072 ms	65.536 ms	43.691 ms
1 0	16	524.288 ms	262.140 ms	174.76 ms
1 1	64	2.097 s	1.049 s	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

PACNT

Pulse Accumulator Counter

	Bit 7	6	5	4	3	2	1	Bit 0
$1027	Bit 7	6	5	4	3	2	1	Bit 0

Can be read and written, unaffected by reset.

PACTL

Pulse Accumulator Control

	Bit 7	6	5	4	3	2	1	Bit 0
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
- 0 = Input only
- 1 = Output

PAEN — Pulse Accumulator System Enable
- 0 = Pulse Accumulator disabled
- 1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
- 0 = Event counter
- 1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

PAMOD	PEDGE	Action on Clock
0	0	PAI falling edge increments counter.
0	1	PAI rising edge increments counter.
1	0	A zero on PAI inhibits counting.
1	1	A one on PAI inhibits counting.

DDRA3 — Data Direction for Port A Bit 3
Overridden if an output compare function is configured to control the PA3 pin.
- 0 = Input
- 1 = Output

I4/O5 — Input Capture 4/Output Compare 5
Configure TI4/O5 for input capture or output compare
- 0 = OC5 enabled
- 1 = IC4 enabled

RTR[1:0] — Real-Time Interrupt (RTI) Rate

RTR [1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz	XTAL = 12.0 MHz
0 0	2^{13}	8.192 ms	4.096 ms	2.731 ms
0 1	2^{14}	16.384 ms	8.192 ms	5.461 ms
1 0	2^{15}	32.768 ms	16.384 ms	10.923 ms
1 1	2^{16}	65.536 ms	32.768 ms	21.845 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

Parallel I/O Control

	Bit 7	6	5	4	3	2	1	Bit 0
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
RESET:	0	0	0	0	0	U	1	1

STAF — Strobe A Interrupt Status Flag
STAF is set when the selected edge occurs on Strobe A and cleared by reading PIOC with STAF set followed by a PORTCL read (simple strobed or full input handshake mode) or PORTCL write (output handshake mode).
0 = No Active Edge Detected
1 = Selected Active Edge Detected

STAI — Strobe A Interrupt Enable Mask
0 = STAF does not request interrupt
1 = STAF requests interrupt

CWOM — Port C Wired-OR Mode (affects all eight port C pins)
0 = Port C outputs are normal CMOS outputs
1 = Port C outputs are open-drain outputs

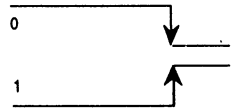
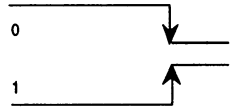
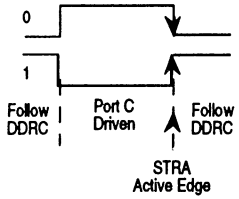
HNDS — Handshake Mode
0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshake Select
HNDS must be set to one for this bit to have meaning.
0 = Input handshake
1 = Output handshake

PLS — Pulse/Interlocked Handshake Operation
HNDS must be set to one for this bit to have meaning. Once activated, strobe B stays active until the selected edge of strobe A is detected when interlocked handshake is selected.
0 = Interlocked handshake
1 = Pulsed handshake (Strobe B pulses high for two E-clock cycles.)

EGA — Active Edge for Strobe A
0 = STRA falling edge selected
1 = STRA rising edge selected

INVB — Invert Strobe B
0 = Active level is logic zero
1 = Active level is logic one

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port C	Port B
Simple strobed mode	Read PIOC with STAF =1, then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to port B
Full input handshake	Read PIOC with STAF =1, then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full output handshake	Read PIOC with STAF =1, then write to PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level, follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

PORTA

Port A Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	I	0	0	0	I	I	I	I
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

NOTE

I/O pins configured as high-impedance inputs have port data that is indeterminate. The contents of the corresponding latches are dependent upon the electrical state of the pins during reset. This is indicated by an "I" in the port description.

PORTB

Port B Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	0	0	0	0	0	0	0	0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Expan. or Test:	ADDR 15	ADDR 14	ADDR 13	ADDR 12	ADDR 11	ADDR 10	ADDR 9	ADDR 8

PORTC

Port C Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	I	I	I	I	I	I	I	I
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Expan. or Test:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

PORTCL

Port C Latched Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
RESET:	I	I	I	I	I	I	I	I

PORTD

Port D Data

	Bit 7	6	5	4	3	2	1	Bit 0
$1008	—	—	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	I	I	I	I	I	I
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	SDO/ MOSI	SDI/ MISO	TxD	RxD

PORTE

Port E Data

	Bit 7	6	5	4	3	2	1	Bit 0
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	I	I	I	I	I	I	I	I
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

PPROG

EEPROM Programming Control

	Bit 7	6	5	4	3	2	1	Bit 0
$103B	ODD	EVEN	ELAT	BYTE	ROW	ERASE	EELAT	EPGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)
EVEN — Program Even Rows in Half of EEPROM (TEST)
ELAT — EPROM/OTPROM Latch Control
Implemented on MC68HC711E9 and MC68S711E9 only.
0 = EPROM/OTPROM address and data bus configured for normal reads and cannot be programmed
1 = EPROM/OTPROM address and data bus configured for programming and cannot be read
BYTE — Byte/Other EEPROM Erase Mode
0 = Row or bulk erase mode used
1 = Erase only one byte of EEPROM
ROW — Row/All EEPROM Erase Mode
(Only valid when BYTE = 0)
0 = Erase all of EEPROM
1 = Erase only one 16-byte row of EEPROM

BYTE	ROW	Action
0	0	Bulk Erase (All Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM
0 = Normal read or program mode
1 = Erase mode
EELAT — EEPROM Latch Control
0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing
EPGM — EPROM/EEPROM Programming Voltage Enable
0 = Programming voltage to array disconnected (EEPROM only on MC68HC(7)11E20)
1 = Programming voltage to array connected (EEPROM only on MC68HC(7)11E20)

SCCR1

SCI Control 1

	Bit 7	6	5	4	3	2	1	Bit 0
$102C	R8	T8	—	M	WAKE	—	—	—
RESET:	I	I	0	0	0	0	0	0

R8 — Receive Data Bit 8
0 = SCI receiver configured for 8-bit data characters.
1 = If M bit is set, R8 stores the ninth data bit in the receive data character.
T8 — Transmit Data Bit 8
0 = SCI transmitter configured for 8-bit data characters.
1 = If M bit is set, R8 stores the ninth data bit in the transmit data character.
Bit 5 — Not implemented; always reads zero
M — Mode (Select Character Format)
0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit
WAKE — Wakeup by Address Mark/Idle
0 = Wakeup by IDLE line recognition
1 = Wakeup by address mark (most significant data bit set)
Bits [2:0] — Not implemented; always read zero

SCCR2

SCI Control 2

	Bit 7	6	5	4	3	2	1	Bit 0
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
- 0 = TDRE interrupts disabled
- 1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
- 0 = TC interrupts disabled
- 1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
- 0 = RDRF and OR interrupts disabled
- 1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
- 0 = IDLE interrupts disabled
- 1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
- 0 = Transmitter disabled
- 1 = Transmitter enabled

RE — Receiver Enable
- 0 = Receiver disabled
- 1 = Receiver enabled

RWU — Receiver Wakeup Control
- 0 = Normal SCI receiver
- 1 = Wakeup enabled and receiver interrupts inhibited

SBK — Send Break
- 0 = Break generator off
- 1 = Break codes generated as long as SBK = 1

SCDR

SCI Data Register

	Bit 7	6	5	4	3	2	1	Bit 0
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	I	I	I	I	I	I	I	I

R[7:0]/T[7:0] — Receiver/Transmitter Data Bits [7:0]
Receive and transmit are double buffered. Reads access the receive data buffer, and writes access the transmit data buffer. When the M bit in SCCR1 is set, R8 and T8 in SCCR1 store the ninth bit in receive and transmit data characters.

SCI Status Register

	Bit 7	6	5	4	3	2	1	Bit 0
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	—
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag
This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR1 with TDRE set and then writing to SCDR.
0 = SCDR busy
1 = SCDR empty

TC — Transmit Complete Flag
This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR1 with TC set and then writing to SCDR.
0 = Transmitter busy
1 = Transmitter idle

RDRF — Receive Data Register Full Flag
This flag is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR1 with RDRF set and then reading SCDR.
0 = SCDR empty
1 = SCDR full

IDLE — Idle Line Detected Flag
This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR1 with IDLE set and then reading SCDR.
0 = RxD line is active
1 = RxD line is idle

OR — Overrun Error Flag
OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR1 with OR set and then reading SCDR.
0 = No overrun
1 = Overrun detected

NF — Noise Error Flag
NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR1 with NF set and then reading SCDR.
0 = Unanimous decision
1 = Noise detected

FE — Framing Error
FE is set when a zero is detected where a stop bit was expected. Clear the FE flag by reading SCSR1 with FE set and then reading SCDR.
0 = Stop bit detected
1 = Zero detected

Bit 0 — Not implemented; always reads zero

SPCR

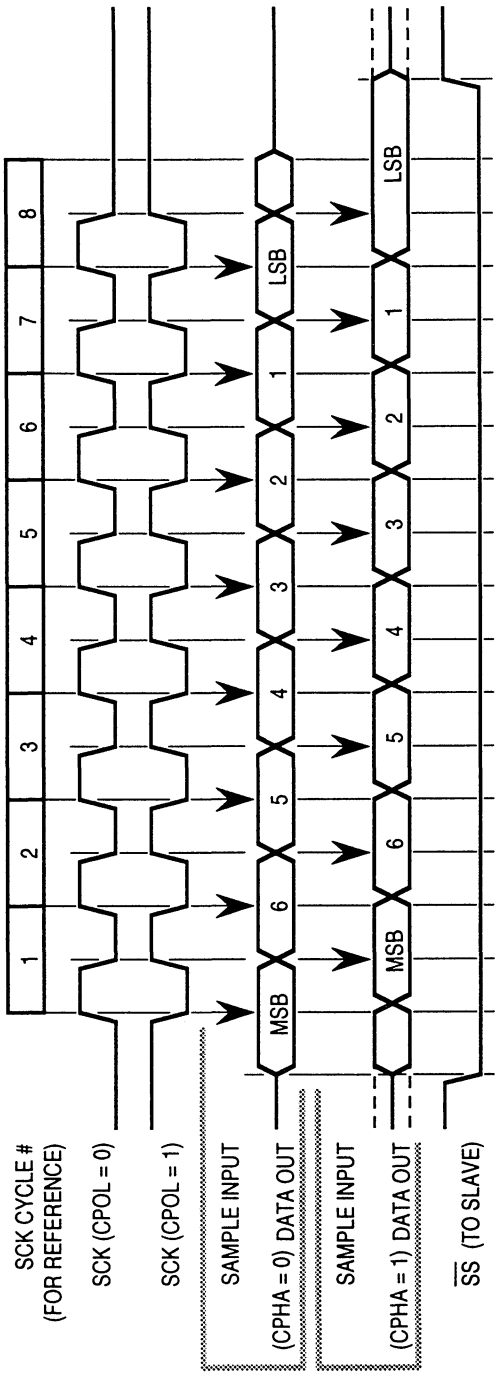
Serial Peripheral Control

	Bit 7	6	5	4	3	2	1	Bit 0
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
0 = SPI interrupts disabled
1 = SPI interrupts enabled
SPE — Serial Peripheral System Enable
0 = SPI off
1 = SPI on
DWOM — Port D Wired-OR Mode Option for Port D Pins PD[5:0]
0 = Normal CMOS outputs
1 = Open-drain outputs
MSTR — Master Mode Select
0 = Slave mode
1 = Master mode
CPOL, CPHA — Clock Polarity, Clock Phase
(Refer to SPI Transfer Format.)
SPR[1:0] — SPI Clock Rate Selects

SPR[1:0]	Divide E Clock By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

SPI Transfer Format



SPDR

SPI Data

	Bit 7	6	5	4	3	2	1	Bit 0
$102A	Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

SPSR

SPI Status Register

	Bit 7	6	5	4	3	2	1	Bit 0
$1029	SPIF	WCOL	—	MODF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag
This flag is set when an SPI transfer is complete (after eight SCK cycles in a data transfer). Clear this flag by reading SPSR (with SPIF = 1), then access SPDR.
0 = No SPI transfer complete or SPI transfer still in progress
1 = SPI transfer complete

WCOL — Write Collision
This flag is set if the MCU tries to write data into SPDR while an SPI data transfer is in progress. Clear this flag by reading SPSR (with WCOL = 1), then access SPDR.
0 = No write collision error
1 = SPDR written while SPI transfer in progress

Bit 5 — Not implemented; always reads zero

MODF — Mode Fault (Mode fault terminates SPI operation)
MODF is set when $\overline{SS}$ is pulled low while MSTR = 1. Clear this flag by reading SPCR with MODF set, then write to SPCR.
0 = No mode fault error
1 = $\overline{SS}$ pulled low in master mode

Bits [3:0] — Not implemented; always read zero

TCNT

Timer Count

$100E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$100F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000. In normal modes, TCNT is a read-only register.

TCTL1

Timer Control 1

	Bit 7	6	5	4	3	2	1	Bit 0
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM[2:5] — Output Mode
OL[2:5] — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

TCTL2

Timer Control 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TEST1

Factory Test

	Bit 7	6	5	4	3	2	1	Bit 0
$103E	TILOP	—	OCCR	CBYP	DISR	FCM	FCOP	TCON
RESET:	0	0	0	0	—	0	0	0

TILOP —Test Illegal Opcode (Test modes only)
Bit 6 — Not implemented; always reads zero
OCCR — Output Condition Code Register to Timer Port (Test modes only)
CBYP — Timer Divider Chain Bypass (Test modes only)
DISR — Disable Resets from COP and Clock Monitor (Special modes only (SMOD = 1))
FCM — Force Clock Monitor Failure (Test modes only)
FCOP — Force COP Watchdog Failure (Test modes only)
TCON — Test Configuration (Test modes only)

TFLG1

Timer Interrupt Flag 1

	Bit 7	6	5	4	3	2	1	Bit 0
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value.

I4/O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TFLG2

Timer Interrupt Flag 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1025	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
The RTIF status bit is automatically set to one at the end of every RTI period. To clear RTIF, write a byte to TFLG2 with bit 6 set.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits [3:0] — Not implemented; always read zero

TI4/O5

Timer Input Capture 4/Output Compare 5

$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TI4/O5**
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

The TI4/O5 register pair resets to ones ($FFFF).

Timer Input Capture

$1010	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC1**
$1011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1012	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC2**
$1013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1014	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC3**
$1015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset

TMSK1

Timer Interrupt Mask 1

	Bit 7	6	5	4	3	2	1	Bit 0
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable
If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

I4/O5I — Input Capture 4/Output Compare 5 Interrupt Enable
When I4/O5 in PACTL is one, I4/O5I is the input capture 4 interrupt enable bit. When I4/O5 in PACTL is zero, I4/O5I is the output compare 5 interrupt enable bit.

IC1I–IC3I — Input Capture x Interrupt Enable
If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

TMSK2

Timer Interrupt Mask 2

	Bit 7	6	5	4	3	2	1	Bit 0
$1024	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts enabled
1 = Interrupt requested when TOF is set to one

RTII — Real-Time Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF is set to one.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF is set to one

PAII — Pulse Accumulator Input Edge Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF is set to one

Bits [3:2] — Not implemented; always read zero

PR[1:0] — Timer Prescaler Select
In normal modes, PR1 and PR0 can only be written once, and the write must occur within 64 cycles after reset.

PR[1:0]	Prescaler
0 0	÷1
0 1	÷4
1 0	÷8
1 1	÷16

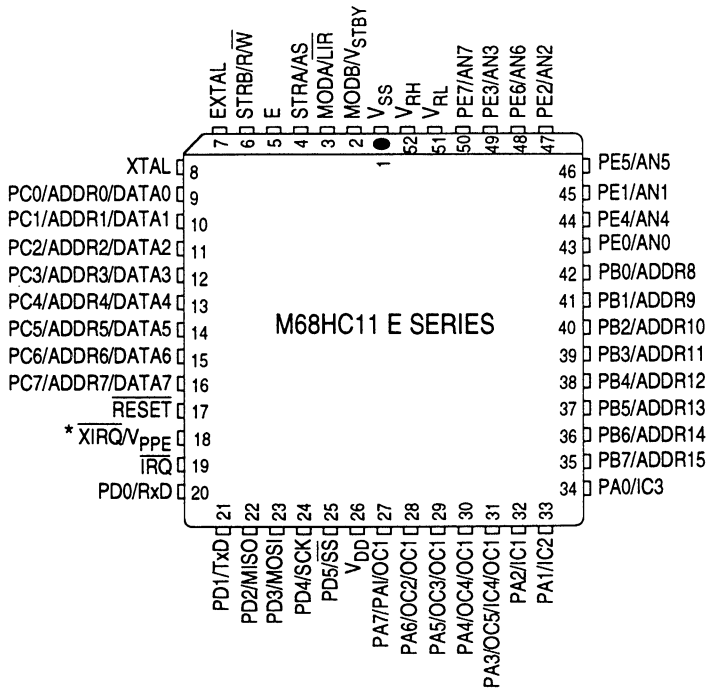
TOC1–TOC4

Timer Output Compare

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC1**
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC2**
$1019	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101A	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC3**
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC4**
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low	

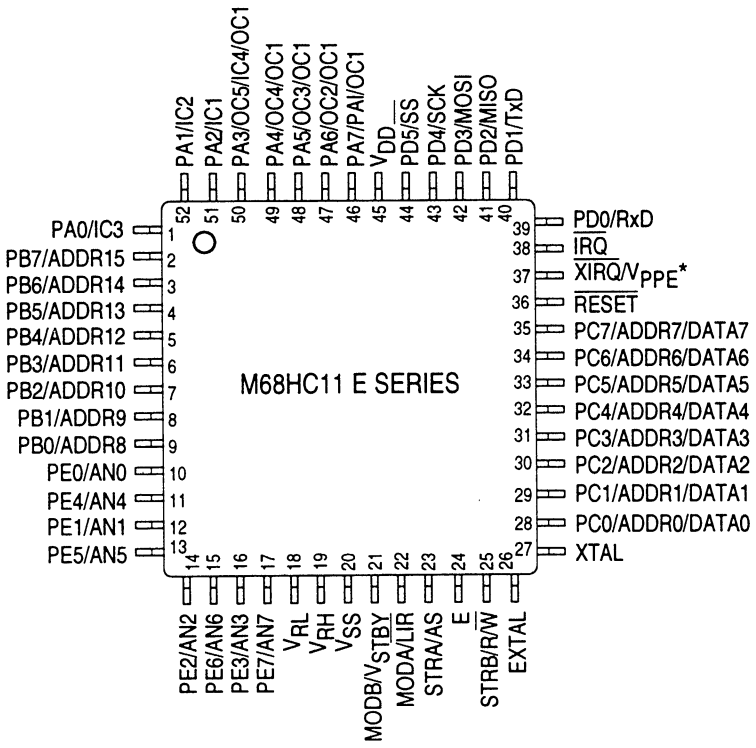
All TOCx register pairs reset to ones ($FFFF).

M68HC11 E Series Pin Assignments
52-Pin PLCC/CLCC



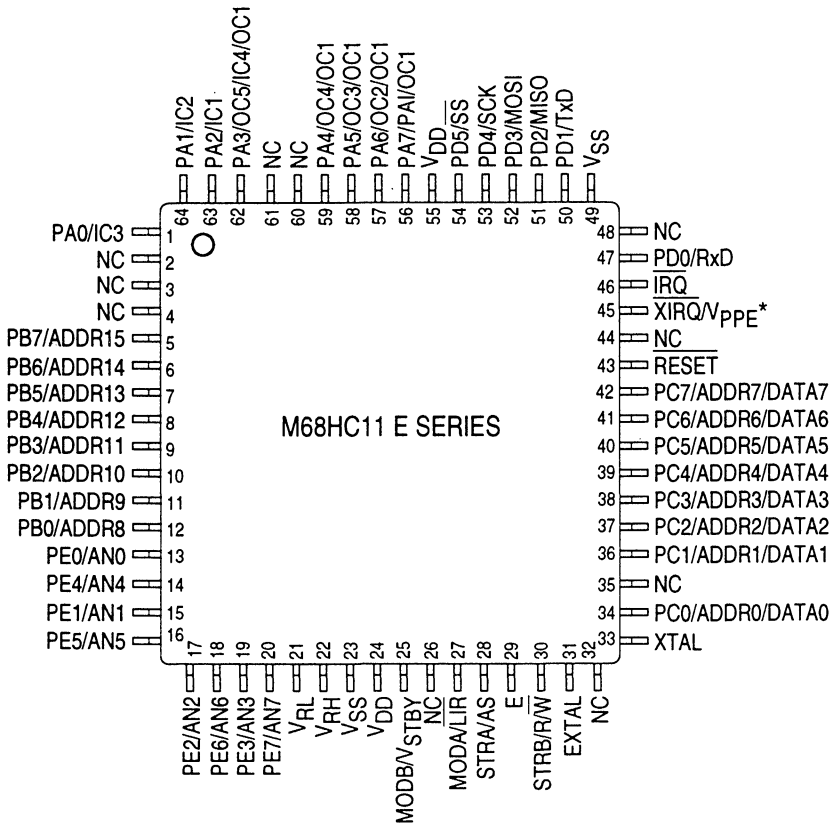
* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

M68HC11 E Series Pin Assignments
52-Pin TQFP



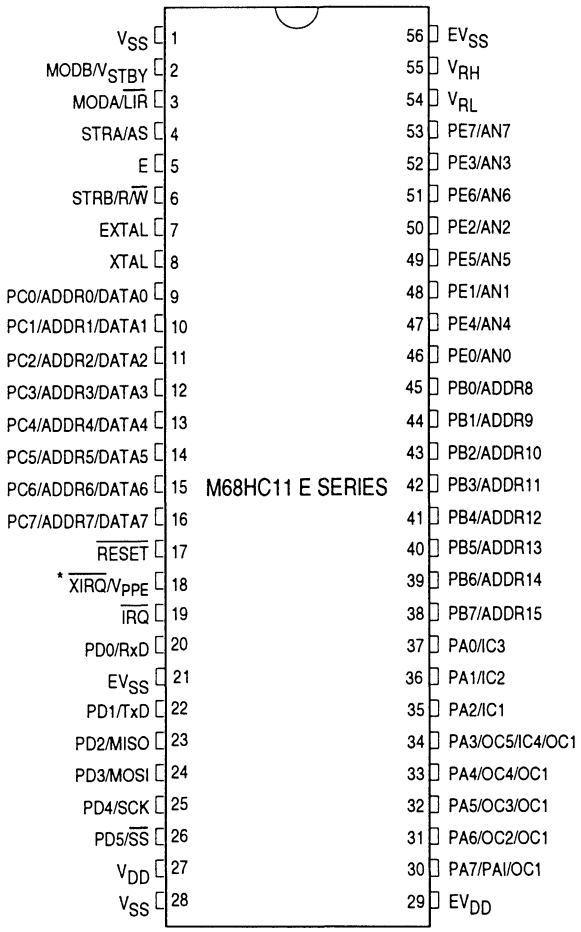
* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

M68HC11 E Series Pin Assignments
64-Pin QFP



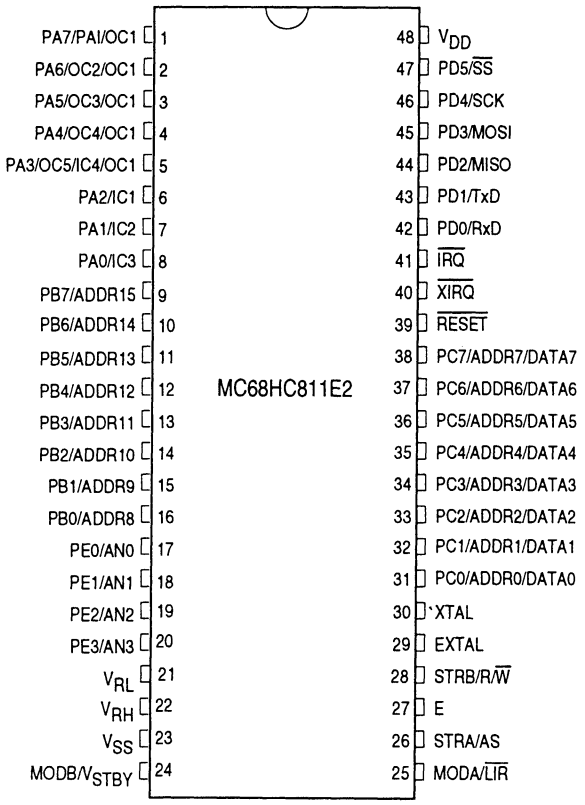
* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

M68HC11 E Series Pin Assignments
56-Pin SDIP



* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

M68HC11 E Series Pin Assignments
48-Pin DIP (MC68HC811E2)



Hexadecimal and Decimal Conversion

How to Use:

Conversion to Decimal: Find the decimal weights for corresponding hexadecimal characters beginning with the least significant character. The sum of the decimal weights is the decimal value of the hexadecimal number.

Conversion to Hexadecimal: Find the highest decimal value in the table which is lower than or equal to the decimal number to be converted. The corresponding hexadecimal character is the most significant. Subtract the decimal value found from the decimal number to be converted. With the difference, repeat the process to find subsequent hexadecimal characters.

15 Byte 8				7 Byte 0			
15 Char 12		11 Char 8		7 Char 4		3 Char 0	
Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15

ASCII CHARACTER SET (7-Bit Code)								
MS Digit / LS Digit	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P		p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	'	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

PROGRAMMING MODEL
CRYSTAL DEPENDENT TIMING
INTERRUPTS

MEMORY MAP
OPCODE MAPS

INSTRUCTIONS
ADDRESSING MODES
EXECUTION TIMES
SPECIAL OPERATIONS

REGISTER AND
CONTROL BIT
ASSIGNMENTS

MECHANICAL DATA
HEX/DEC CONVERSION
ASCII CHART

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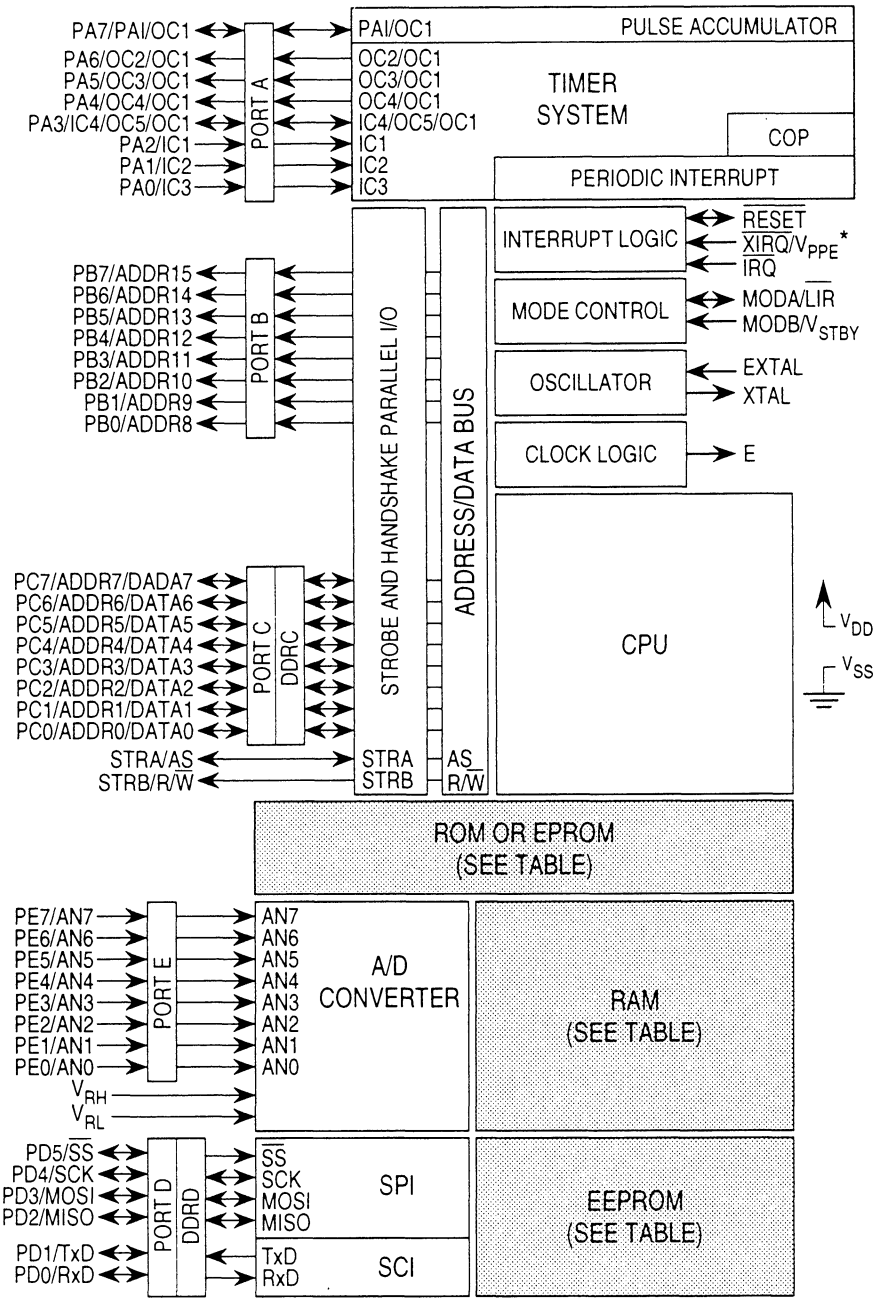
ASCII CHART

Block Diagram



DEVICE	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	—	—	—
MC68HC11E1	512	—	—	512
MC68HC11E8	512	12K	—	—
MC68HC11E9	512	12K	—	512
MC68HC711E9	512	—	12K	512
MC68HC11E20	768	20K	—	512
MC68HC711E20	768	—	20K	512
MC68HC811E2	256	—	—	2048

* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

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