

Exam 1

Last Name, First Name

[6%] 1. Do the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(2%) a) Determine the unsigned binary, octal, hexadecimal, and BCD representations of the number 170_{10} .

$$\begin{array}{r} 2 \overline{) 170} \\ \underline{2 \overline{) 85} 0} \\ 2 \overline{) 42} 1 \\ \underline{2 \overline{) 21} 0} \\ 2 \overline{) 10} 1 \\ \underline{2 \overline{) 5} 0} \\ 2 \overline{) 2} 1 \\ \underline{2 \overline{) 1} 0} \\ 0 \ 1 \end{array}$$

Binary: 10101010
Octal: 10_A10_A010 = 252
Hex: 1010_A1010 = AA
BCD: 0001_A0111_A0000

(2%) b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -85_{10} .

Same as above after the 1st division
 $85 = 1010101$
for 8 bits 01010101

Signed Mag: 1_A1010101
1's Comp: 1010_A1010
2's Comp: 1010_A1011

(2%) c) What is $170_{10} - 85_{10}$ in 8-bit 2's complement? Remember that you must **show all work**.

($170_{10} - 85_{10}$)₂: 01010101

$$\begin{array}{r} 170 \quad 1010_A1010 \\ + (-85) \quad 1010_A1011 \\ \hline + 85 \quad 0101_A0101 \end{array}$$

Exam 1

Last Name, First Name

[10%] 2. Answer the following questions given the below **truth table** with inputs A, B and C and output f.

A	B	C	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(2%) a) Write the corresponding **minterm** (i.e., **canonical** sum of products CSOP) ~~or~~ **maxterm** (i.e., **canonical** product of sums CPOS) equation for f (one or the other, but not both).

minterm (CSOP) $f = \bar{A} \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C} + A \cdot B \cdot C$

maxterm (CPOS) $f = (\bar{A} + B + C) \cdot (A + \bar{B} + \bar{C}) \cdot (A + \bar{B} + C) \cdot (A + B + \bar{C})$

Which did you write above? (circle one): Minterms (CSOP) Maxterm (CPOS)

(1%) b) Completely fill in the K-map (to the right) with 1's and 0's (no blanks).

(2%) c) With the K-map to the right, find the minimum sum of products (MSOP) solution. (Label each grouping with the appropriate expression and then write the total equation. Use proper lexical ordering; i.e., /A before A, A before B, & D₃ before D₂.)

		AB			
		00	01	11	10
C	0	1	0	1	0
	1	0	0	1	1

$f_{MSOP} = \bar{A} \cdot \bar{B} \cdot \bar{C} + A \cdot B + A \cdot C$

(3%) d) Completely fill in the K-map (to the right) with 1's and 0's (no blanks) and find the minimum product of sums (MPOS) solution. **Note:** The order of the signals in the K-map has been changes! (**BC** is on top)

		BC			
		00	01	11	10
A	0	1	0	0	0
	1	0	1	1	1

$f_{MPOS} = (\bar{A} + B + C) \cdot (A + \bar{B}) \cdot (A + \bar{C})$

(1%) e) Are f_{MSOP} and f_{MPOS} equivalent expressions? Why?

Circle One: Yes (equivalent) No (not equivalent)
*Same truth table (with no don't cares used)
 You can also prove algebraically that they are equivalent!*

(1%) f) Which solutions is less costly (in gates) and why? **Circle One:** MSOP MPOS **NEITHER**

MSOP: 3 ANDs, 3 NOTs, 1 OR
MPOS: 3 ORs, 3 NOTs, 1 AND

Exam 1

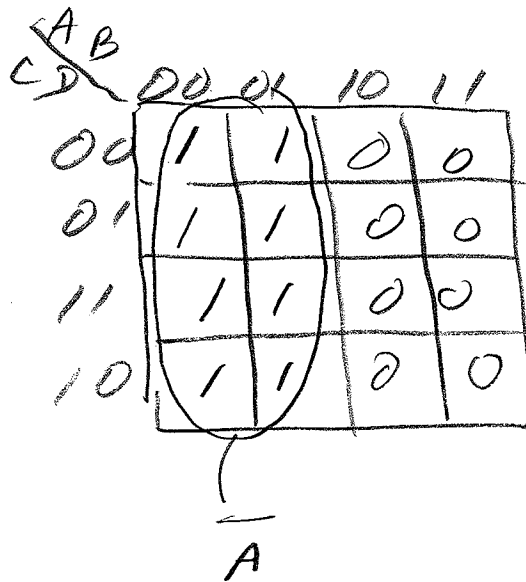
 Last Name, First Name

[10%] 3. Using any technique you desire, simplify the following equation. Give the result as a minimum sum of products (MSOP). **Show all work!**

$$Z = \overline{A}(B + C) + A/C + A/B(D + C D)$$

$$Z = \overline{A}B + \overline{A}C + \overline{A}\overline{C} + \overline{A}\overline{B}\overline{D} + \overline{A}\overline{B}\overline{C}D$$

0 1 0 1 0 0 0 0 0 0 0 0 1



$Z_{MSOP} = \overline{A}$

Exam 1

 Last Name, First Name

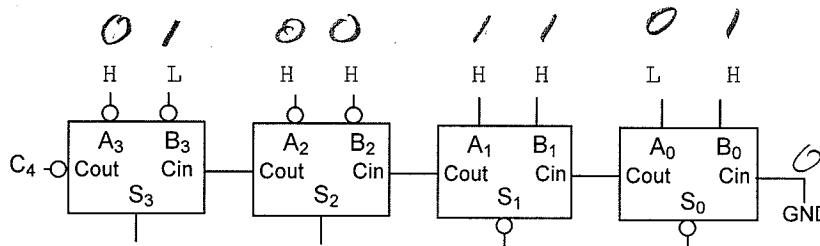
[9%] 4. **Logic vs. voltage** using adders.

A 4-bit adder will add two 4-bit numbers: $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$; and produce a 4-bit sum $S_3S_2S_1S_0$ and a carry-out C_4 . For example:

If $A_3A_2A_1A_0 = 1001$
 $B_3B_2B_1B_0 = 1100$
 Then $S_3S_2S_1S_0 = 0101$, with $C_4 = 1$

The above example is to help you review how the adder works. It is **not** a part of the test.

The following 4-bit adder has signals $A_3, B_3, A_2, B_2, S_1,$ and S_0 and C_4 assigned to active low. All other signals are assigned active high.



(a) We applied the above **VOLTAGE** values to add two binary numbers. What two binary numbers are we trying to add?

$A_3 = \underline{0}$ (0 or 1) $A_2 = \underline{0}$ (0 or 1) $A_1 = \underline{1}$ (0 or 1) $A_0 = \underline{0}$ (0 or 1)

$B_3 = \underline{1}$ (0 or 1) $B_2 = \underline{0}$ (0 or 1) $B_1 = \underline{1}$ (0 or 1) $B_0 = \underline{1}$ (0 or 1)

(b) What **VOLTAGE** values (i.e., high H or low L) do you expect for $S_3S_2S_1S_0$ and C_4 ?

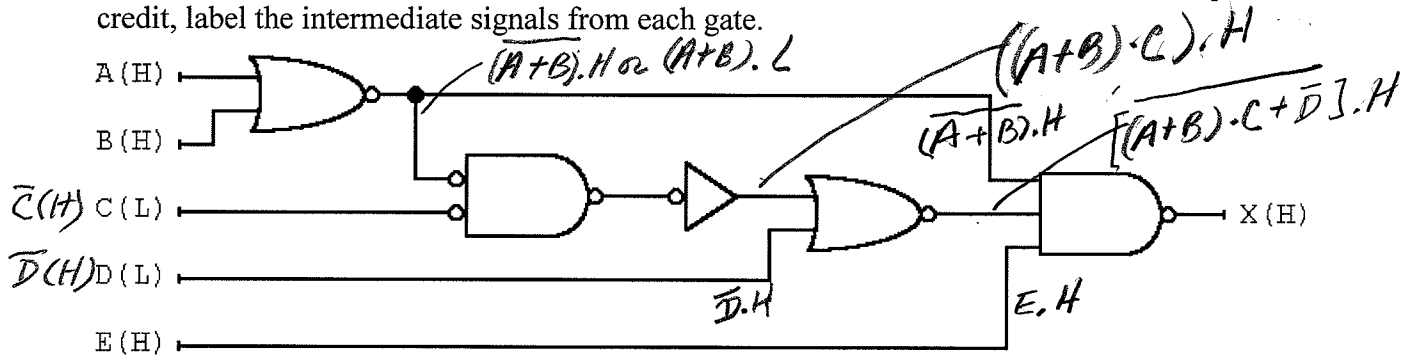
$S_3 = \underline{H}$ (H or L) $S_2 = \underline{H}$ (H or L) $S_1 = \underline{H}$ (H or L) $S_0 = \underline{L}$ (H or L)

$C_4 = \underline{H}$ (H or L)

Exam 1

Last Name, First Name

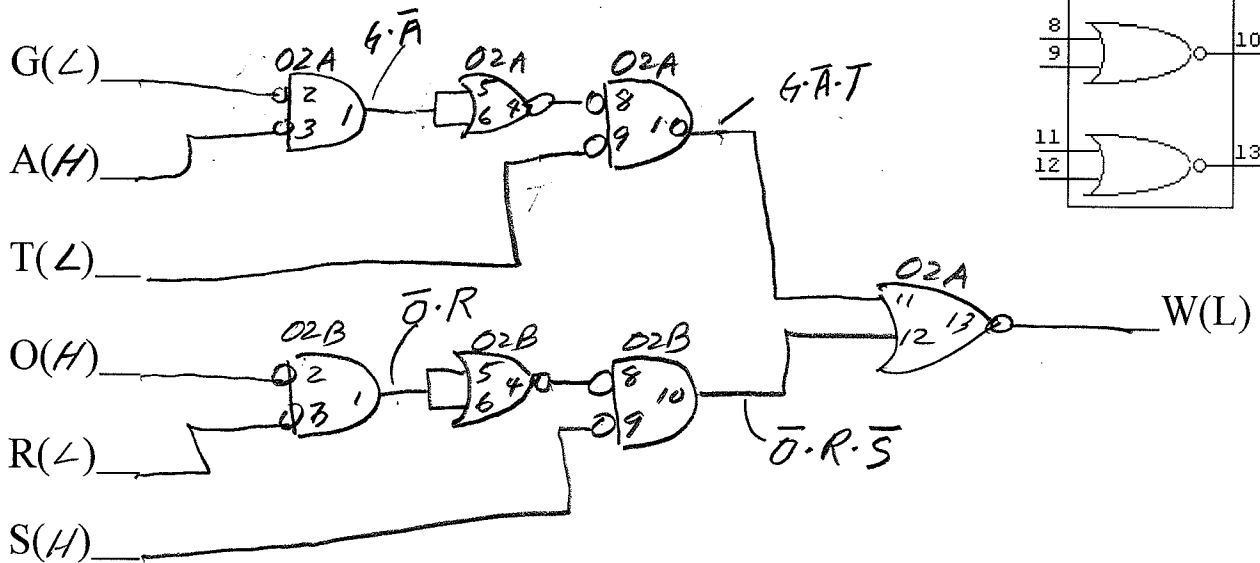
- [7%] 5. Determine the equation **directly** implemented with this mixed-logic circuit. Do **not** minimize the equation. It is **not** necessary to put the equation in lexical order. For partial credit, label the intermediate signals from each gate.



$$X = \overline{(A+B)} \cdot ((A+B) \cdot C + \bar{D}) \cdot E$$

- [10%] 6. Directly implement the below equation with a mixed-logic circuit diagram. Use only gates available on 74'02 chips. (Use the appropriate mixed-logic symbols). **Label** all gates and **pin numbers** as you should be doing in lab. Pick whatever activation levels you want for the inputs, but make the output W active-low.

$$W = (G * \bar{A} * T) + (\bar{O} * R * \bar{S})$$

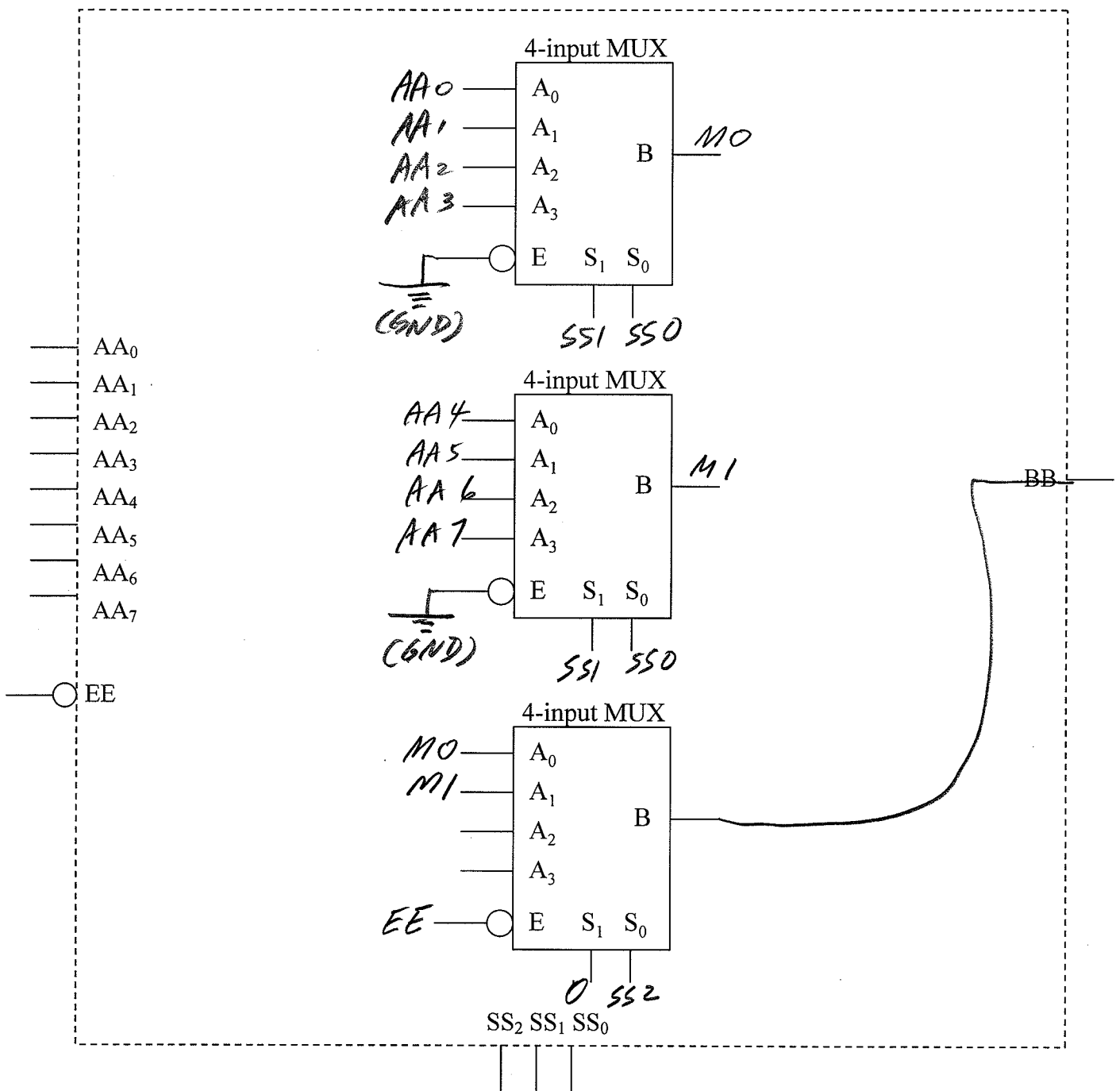


Exam 1

Last Name, First Name

- [12%] 7. Create an equivalent 8-input multiplexer using 4-input multiplexers (see truth table), and using the **minimum number of components**. You can use additional gates if necessary. However, each gate counts as a component. A 4-input MUX also counts as one component.

E	S ₁	S ₀	A ₃	A ₂	A ₁	A ₀	B
0	*	*	X	X	X	X	Hi-Z
1	0	0	X	X	X	0	0
1	0	0	X	X	X	1	1
1	0	1	X	X	0	X	0
1	0	1	X	X	1	X	1
...



Exam 1

Last Name, First Name

[12%] 8. Implementation of Logic with Decoders

Given the following 2 logic equations and activation levels for the signals, implement them with the following decoder and any number of 3-input OR gates (**ONLY**).

- For maximum credit, use the minimum number of gates.
- Just draw the gates. You don't have to label them (e.g., like 7411)
- Note the * is the AND operator and /A is "NOT A".
- All signals are active high, except Z2, which is active low.



$$Z1 = \overline{A} \cdot \overline{B} \cdot C + A \cdot \overline{B} \cdot C + \overline{A} \cdot B$$

000 101 010

A, B, C, at Z1

$$Z2 = (\overline{A+B+C}) \cdot (A+B)$$

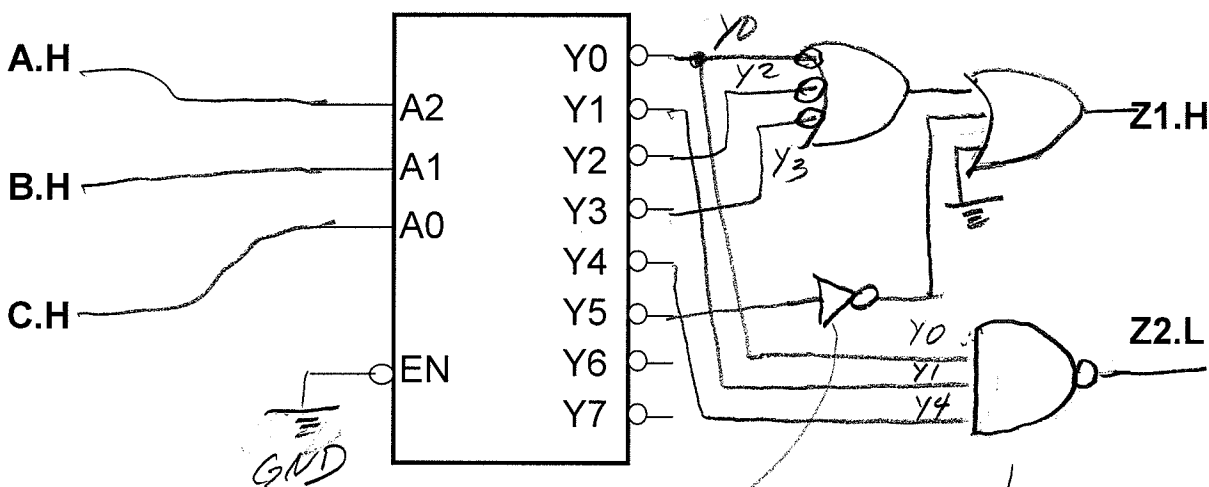
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$$= \overline{A \cdot B \cdot C} \cdot \overline{A \cdot B}$$

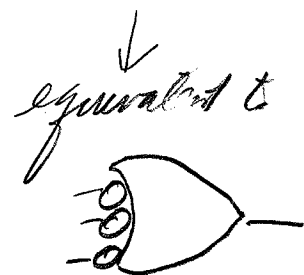
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de Morgan's law

3-to-8 decoder



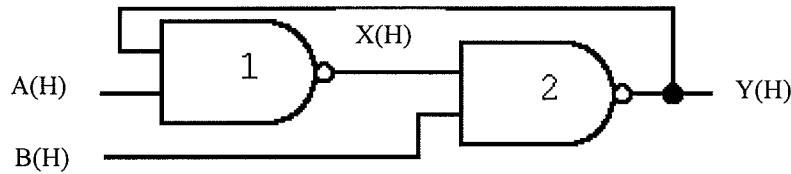
For partial credit, show work here:



Exam 1

 Last Name, First Name

- [8%] 9. Given the following simple circuit consisting of two NAND gates, derive the next state **voltage** table (use L and H) for the device. In other words, given each combination of voltage values for A, B, and X, what are the values for X and Y **after the circuit becomes stable**?



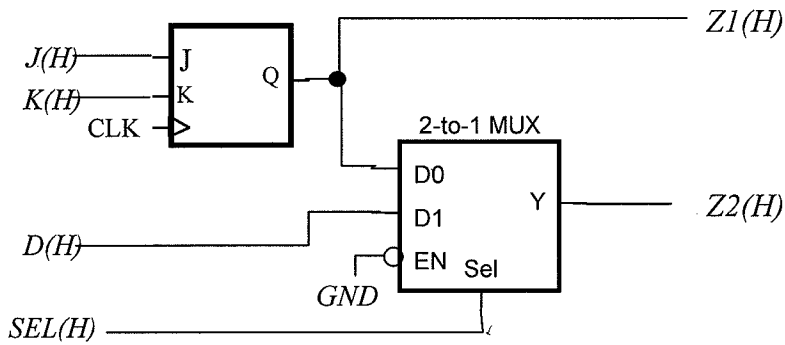
(a)

A	B	X	X ⁺	Y ⁺
L	L	L	H	H
L	L	H	H	H
L	H	L	H	L
L	H	H	H	L
H	L	L	L	H
H	L	H	L	H
H	H	L	L	H
H	H	H	H	L

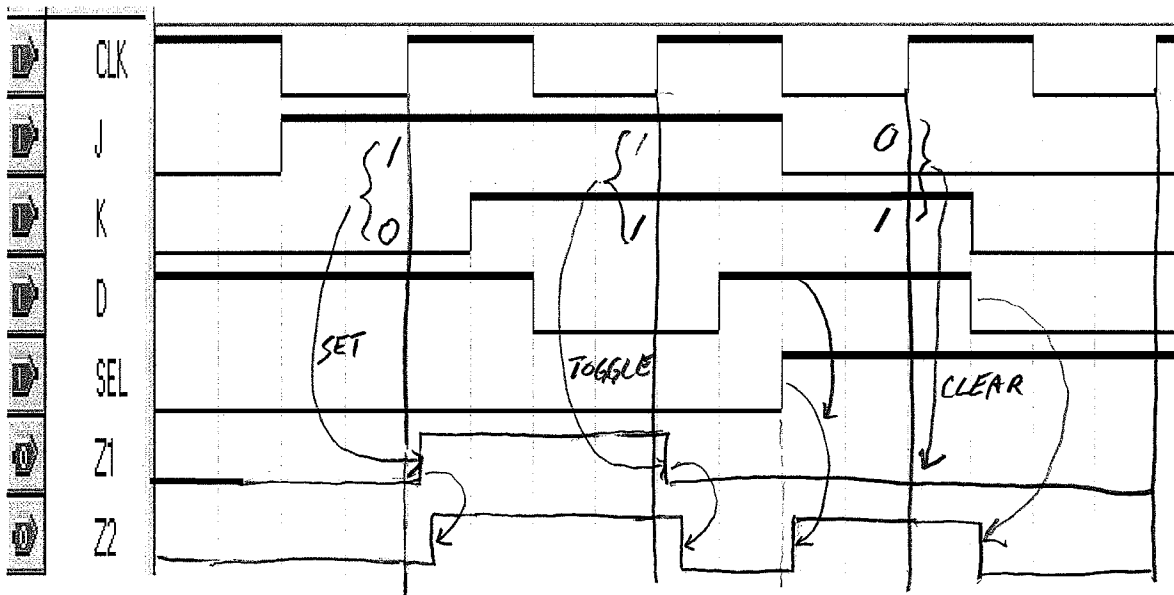
Exam 1

 Last Name, First Name

[8%] 10. Synchronous component (flip-flop) vs. combinatorial component (MUX)



Given the above circuit, complete the following voltage timing diagrams:



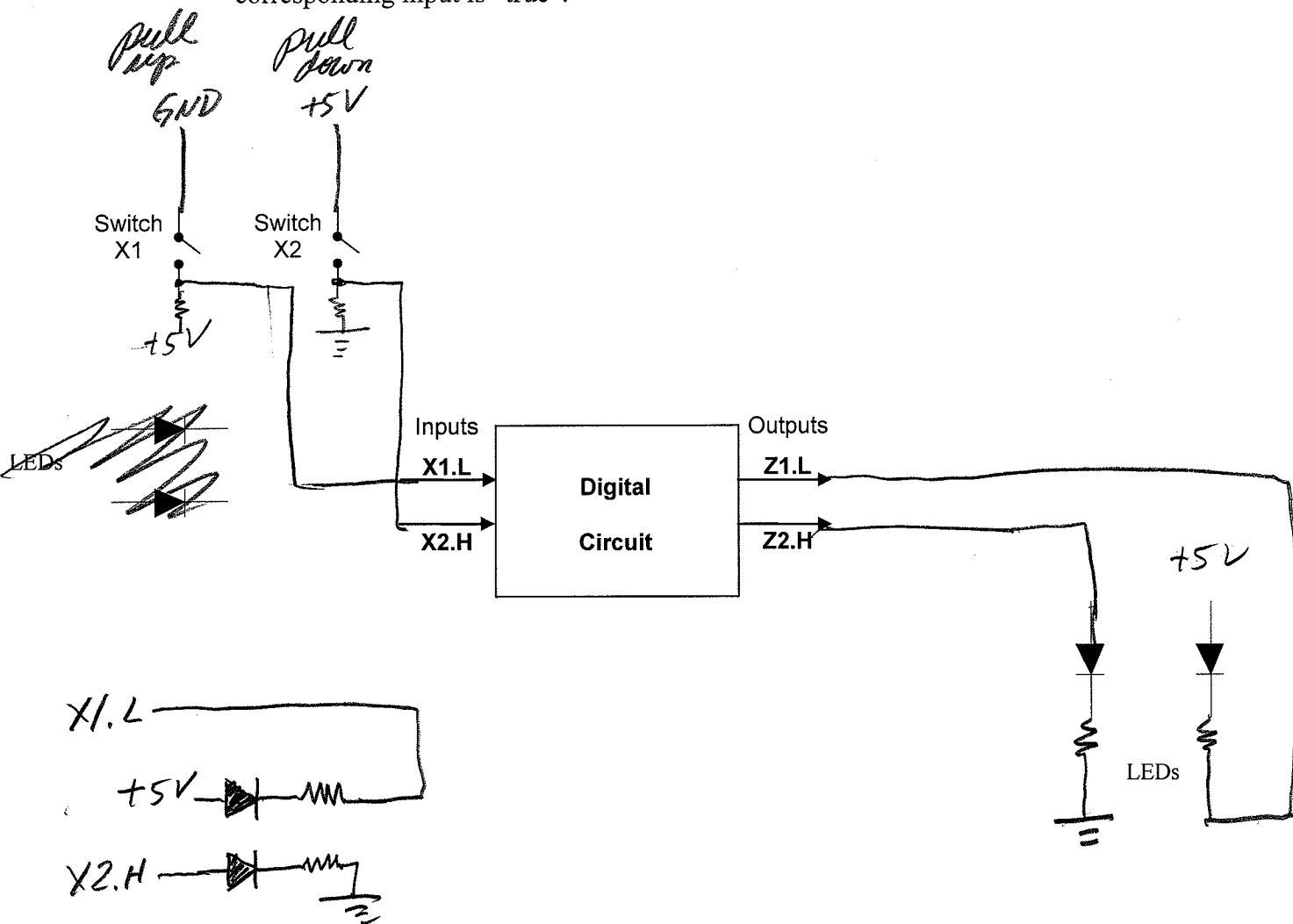
Show propagational delays and go as far as you can.

Exam 1

 Last Name, First Name

[8%] 11. Building switches and LEDs

- [4%] (a) Shown below are two switches X1 and X2. Complete the design of the two switches to generate two input signals: active low X1.L and active high X2.H. In other words, make the connections among the switches, resistors, VCC, and GND to produce the two signals.
- [2%] (b) Coming out of the digital circuit are two output signals. Make the connections among the LED's, resistors, VCC, and GND to display the active low output Z1.L to an active low LED and the active high output Z2.H to an active high LED. An LED should be lit when the corresponding output is "true".
- [2%] (c) The TA wants to see LEDs on the input signals. Make the connections among the LED's, resistors, VCC, and GND to display the active low input X1.L to an active low LED and the active high input X2.H to an active high LED. An LED should be lit when the corresponding input is "true".



Laws and Theorems of Boolean Algebra

Operations with 0 and 1:

- | | |
|----------------|---------------------|
| 1. $X + 0 = X$ | 1D. $X \cdot 1 = X$ |
| 2. $X + 1 = 1$ | 2D. $X \cdot 0 = 0$ |

Idempotent laws:

- | | |
|----------------|---------------------|
| 3. $X + X = X$ | 3D. $X \cdot X = X$ |
|----------------|---------------------|

Involution laws:

4. $(X')' = X$

Laws of complementarity:

- | | |
|-----------------|----------------------|
| 5. $X + X' = 1$ | 5D. $X \cdot X' = 0$ |
|-----------------|----------------------|

Commutative laws:

- | | |
|--------------------|---------------|
| 6. $X + Y = Y + X$ | 6D. $XY = YX$ |
|--------------------|---------------|

Associative laws:

- | | |
|--|---------------------------|
| 7. $(X + Y) + Z = X + (Y + Z) = X + Y + Z$ | 7D. $(XY)Z = X(YZ) = XYZ$ |
|--|---------------------------|

Distributive laws:

- | | |
|-------------------------|-------------------------------|
| 8. $X(Y + Z) = XY + XZ$ | 8D. $X + YZ = (X + Y)(X + Z)$ |
|-------------------------|-------------------------------|

Simplification theorems:

- | | |
|----------------------|---------------------------|
| 9. $XY + XY' = X$ | 9D. $(X + Y)(X + Y') = X$ |
| 10. $X + XY = X$ | 10D. $X(X + Y) = X$ |
| 11. $(X + Y')Y = XY$ | 11D. $XY' + Y = X + Y$ |

DeMorgan's laws:

- | | |
|---|-----------------------------------|
| 12. $(X + Y + Z + \dots)' = X'Y'Z'$ | 12D. $(XYZ\dots)' = X' + Y' + Z'$ |
| 13. $[f(A, B, \dots, Z, 0, 1, +, \cdot)]' = f(A', B', \dots, Z', 1, 0, \cdot, +)$ | |

Duality:

- | | |
|---|---|
| 14. $(X + Y + Z + \dots)^D = XYZ\dots$ | 14D. $(XYZ\dots)^D = X + Y + Z + \dots$ |
| 15. $[f(A, B, \dots, Z, 0, 1, +, \cdot)]^D = f(A, B, \dots, Z, 1, 0, \cdot, +)$ | |

Theorems for multiplying out and factoring:

- | | |
|----------------------------------|-----------------------------------|
| 16. $(X + Y)(X' + Z) = XZ + X'Y$ | 16D. $XY + X'Z = (X + Z)(X' + Y)$ |
|----------------------------------|-----------------------------------|

Consensus theorems:

- | | |
|--------------------------------|---|
| 17. $XY + YZ + X'Z = XY + X'Z$ | 17D. $(X + Y)(Y + Z)(X' + Z) = (X + Y)(X' + Z)$ |
|--------------------------------|---|