University of Florida
Department of Electrical & Computer Engineering

EEL 3701 Fall 1996
30 October 1996

Dr. Eric M. Schwartz
Professor in ECE

Exam #2

16-May-99 5:15 PM

_____ , _____
Last Name , First Name

Instructions:

- *Show **all** work on the **front** of the test papers. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will not be graded without an indication on the front.*
- *You may **not** use any notes, homeworks, labs, other books, or calculators.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *This exam counts for at least 20%. of your total grade (13.3% if you fail to take one of the 3 exams).*
- *Put your name at the top of **each** test page and be sure your exam consists of 9 distinct pages.*
- ***Read** each question **carefully** and **follow the instructions**.*
- *Boolean expression answers must be in **lexical order**.*

Good luck!

PLEDGE:
On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____ _____
PRINT YOUR NAME SIGN YOUR NAME DATE

COMMENTS, FEEDBACK, or any special instructions for the professor:

Page	Available	Points
1	0	0
2	0	
3	10	
4	20	
5	18	
6	8	
7	13	
8	14	
9	16	
TOTAL	100	

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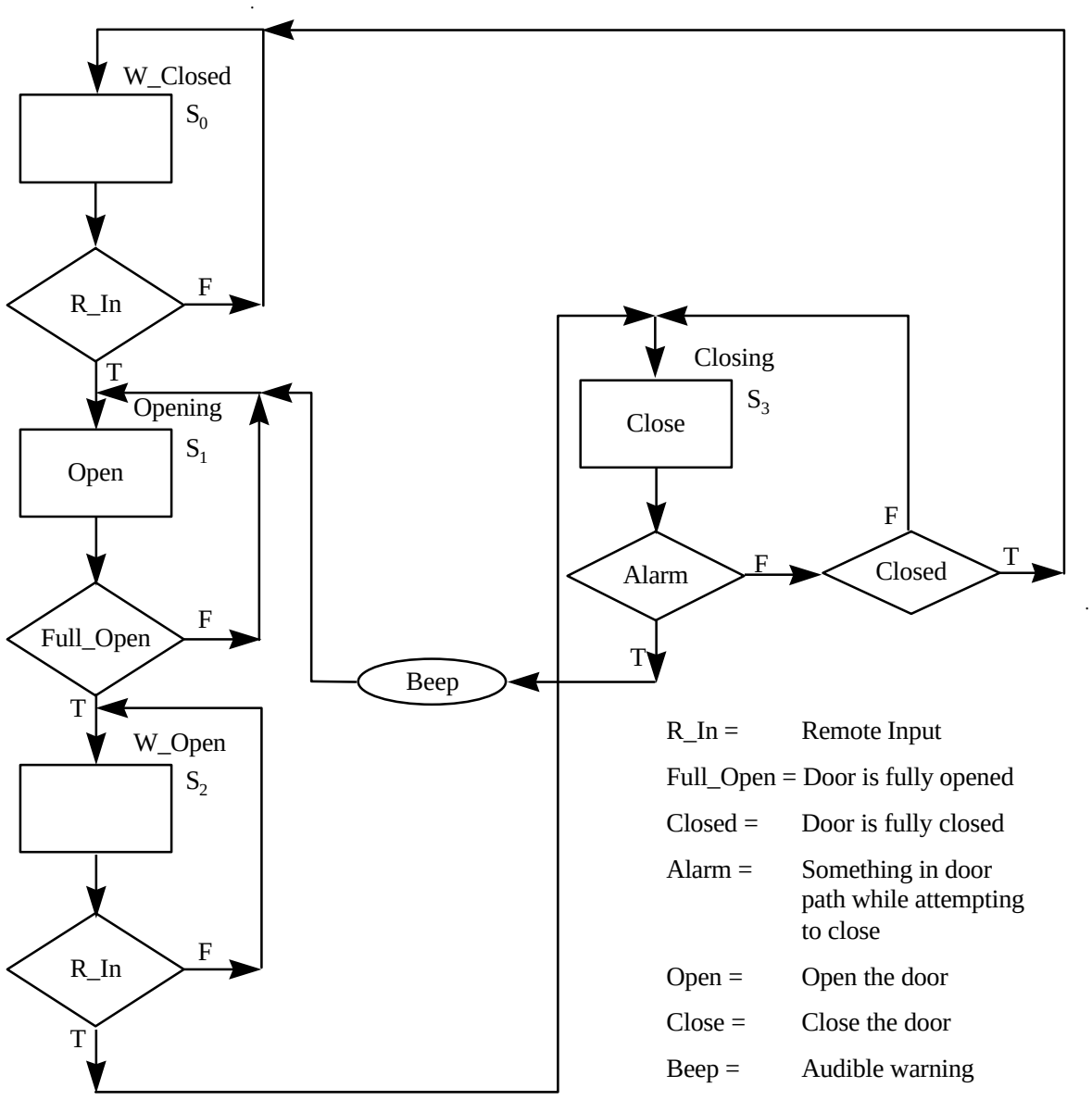
[65%] 1. Below is an ASM flowchart for an electric garage door. The input **R_In** (Remote input) causes a closed door to open and an opened door to close. When the door is opening, the output **Open** causes the motor to turn clockwise. When the door is closing, the output **Close** cause the motor to turn counterclockwise. There are three additional inputs to your controller: **Full_Open** (automatically set when the door is fully opened), **Closed** (automatically set when the door is fully closed), and **Alarm** (automatically set when something is in the door path while the door is closing). An **Alarm** causes a closing door to open instead, and a beep to sound.

4 min



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(4%) 2 min 1. a) What is the minimum number of D flip-flops needed to implement this design. Why? How many JK flip-flops would be needed (assuming D FF's are not available).

No explanation, no credit.

Number of D FFs =_____

Number of JK FFs =_____

(6%) 3 min b) What minimum size EPROM do you need to implement this design using **only** the EPROM, one D flip-flop, and as many JK flip-flops as you need. **(No other chips.)** Explain .

No explanation, no credit.

Size of EPROM
(# of Addresses x # of data bits, *e.g.*, 2k x 8) =_____

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(10%) 1. c) Draw a wiring diagram (without pin numbers) corresponding to parts a and b above. Make the outputs active low. (For **partial credit only**, do the design with only D flip-flops instead of a single D flip-flop and JK flip-flop(s).) Use only **rising** edge flip-flops.

3 min

(6%) 1. d) Fill in the below excitation table for D and JK flip-flops.

3 min

Q	Q^+	J	K	D

(4%) e) Give a state binary assignment that attempts to minimize the bit changes between states. Give state W_Closed (S_0) the minimum value (Q_i=0). Leave blank any columns not needed (see part a above.)

3 min

State Name	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
W_Closed (S_0)								
Opening (S_1)								
W_Open (S_2)								
Closing (S_3)								

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(18%) 1. f) Fill in the below **state transition and output** table. Use don't cares (X) as needed.

10 min

Current State Name	R_In	Full_Open	Alarm	Closed	Next State Name	Open	Close	Beep

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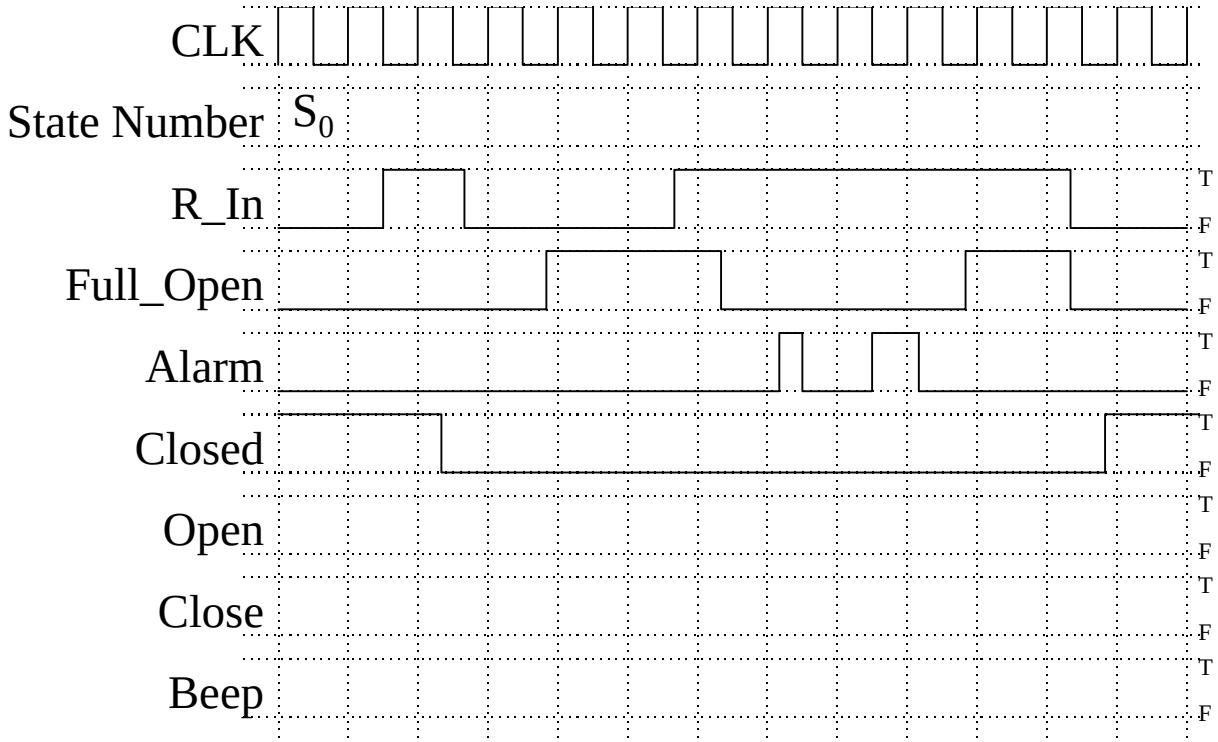
(8%) 1. g) Complete the below timing diagram and fill in the appropriate state names. (Use the short names, *e.g.,* S_0). The first state S_0 (W_Closed) is given, as are the input sequences.

8 min



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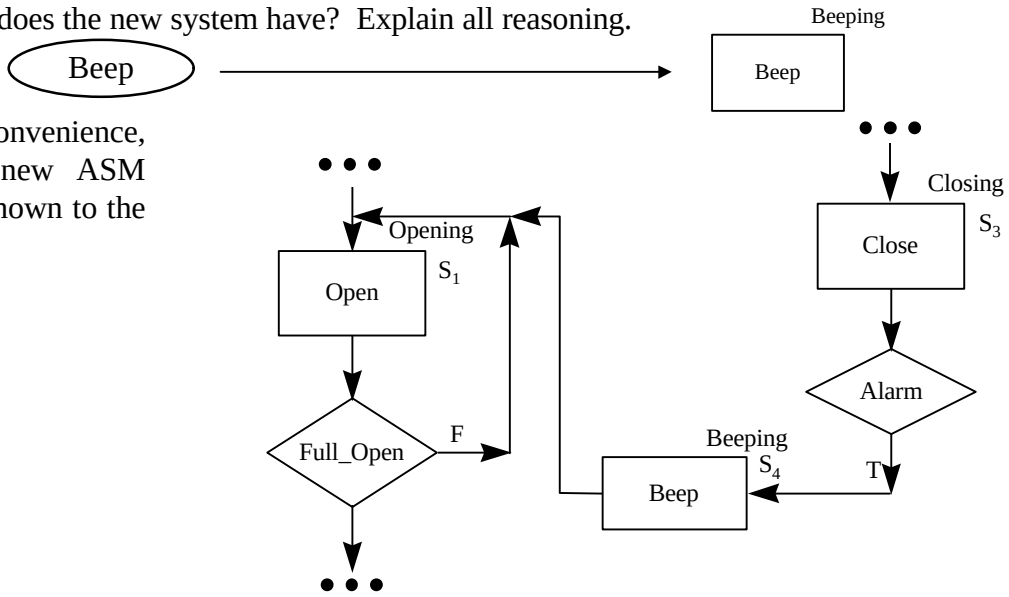
(9%) 1. h) A new ASM replaces the oval (with **Beep** inside) with a rectangle (see below). Explain the differences of operation for the circuit designed from the original ASM flowchart and one designed from this new ASM flowchart. What added or reduced costs does the new system have? Explain all reasoning.

3 min



For your convenience, part of the new ASM flowchart is shown to the right.

[4%] 2. How do PALs and PLAs differ.

3 min

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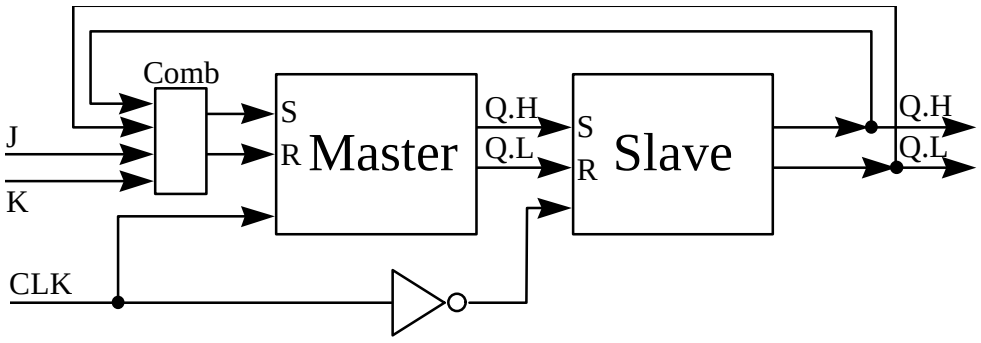
[4%] 3 min 3. Design a 3-bit parallel adder using as many FA and HA as you need. Use any other basic AND/OR gates you feel are necessary. The inputs are $X_2X_1X_0$ and $Y_2Y_1Y_0$ and the output is $Z_2Z_1Z_0$ and C_{OUT}. The inputs and outputs are all active-high.

[4%] 3 min 4. Design a 4-bit register using any of the following fundamental logic elements: ANDs, ORs, MUXs, DEMUXs, DECODERs, ENCODERs, Flip-Flops, Adders. This register should accomplish synchronous parallel loads and parallel outputs.

[6%] 3 min 5. We used SR latches to build our Master/Slave JK flip-flop in lab 5. Explain the "Master/Slave" operation of this block diagram.



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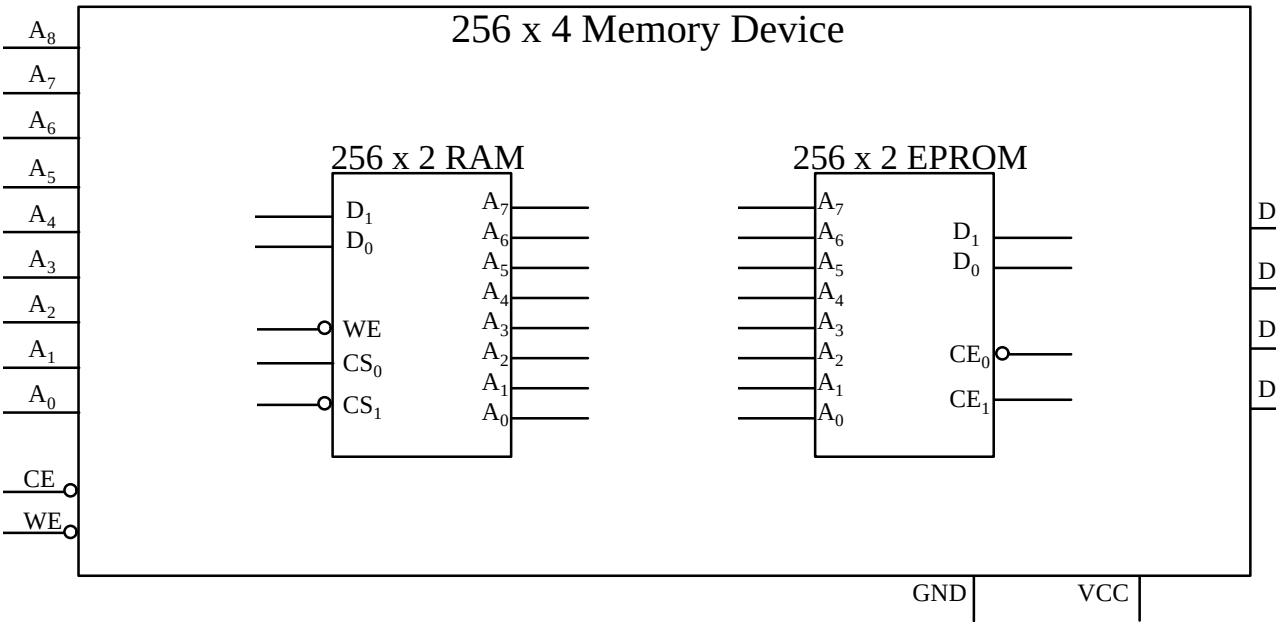
[16%] 6. Add the necessary wiring (or labels, as in LogicWorks™) and circuit elements to create the two memory devices described below.

8 min

(8%) a) A 256 x 4 memory device with RAM in the lower 2-bits (least significant bits) of data and EPROM in the upper 2-bits of data.



(8%) b) A 512 x 2 memory device with RAM in the lower 256 address space and EPROM in the upper 256 of memory address space.