University of Florida
Department of Electrical & Computer Engineering

EEL 3701—Fall 2007
Wednesday, 3 October 2007

Drs. Lam, Schwartz and Arroyo

Exam 1

_____

Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *This exam counts for 24% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page and be sure your exam consists of **12** distinct pages. Sign your name and add the date below.*
- *The point values for problems may be changed at prof's discretion*
- *Notation reminder: A(H) is the same as A.H..*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs/outputs of each gate with the appropriate logic equations.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good Evening! Welcome!

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (3 Oct 2007)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2	6	
3	10	
4	10	
5	9	
6	17	
7	12	
8	12	
9	8	
10	8	
11	8	
TOTAL	100	

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[6%] 1. Do the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(2%) a) Determine the unsigned binary, octal, hexadecimal, and BCD representations of the number 170_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(2%) b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -85_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) c) What is 170_{10} -85_{10} in 8-bit 2's complement? Remember that you must **show <u>all</u> work.**

$(170_{10}-85_{10})_2$: _____

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[10%] 2. Answer the following questions given the below **truth table** with inputs A, B and C and output *f*.

A	B	C	*f*
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(2%) a) Write the corresponding **minterm** (i.e., **canonical** sum of products CSOP) –***or***– **maxterm** (i.e., **canonical** product of sums CPOS) equation for *f* (one or the other, but not both).

Which did you write above? (circle one): Minterms (CSOP) Maxterm (CPOS)

(1%) b) Completely fill in the K-map (to the right) with 1's and 0's (no blanks).

C \ AB	00	01	11	10
0				
1				

(2%) c) With the K-map to the right, find the minimum sum of products (MSOP) solution. (Label each grouping with the appropriate expression and then write the total equation. Use proper lexical ordering; *i.e., /A before A, A before B, & D_3 before D_2.*)

f_{MSOP} = _____

(3%) d) Completely fill in the K-map (to the right) with 1's and 0's (no blanks) and find the minimum product of sums (MPOS) solution. **Note**: The order of the signals in the K-map has been changes! (**BC** is on top)

A \ BC	00	01	11	10
0				
1				

f_{MPOS} = _____

(1%) e) Are f_{MSOP} and f_{MPOS} equivalent expressions? Why?

Circle One: Yes (equivalent) No (not equivalent)

(1%) f) Which solutions is less costly (in gates) and why? **Circle One**: MSOP MPOS NEITHER

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[10%] 3. Using any technique you desire, simplify the following equation. Give the result as a minimum sum of products (MSOP). **Show all work!**

Z = /A (B + C) + /A/C + /A /B (/D + /C D)

Z_{MSOP} = _____

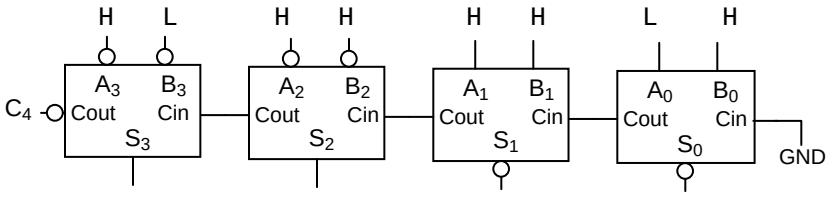
[9%] 4. **Logic vs. voltage** using adders.

A 4-bit adder will add two 4-bit numbers: $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$; and produce a 4-bit sum $S_3S_2S_1S_0$ and a carry-out C_4. For example:

If $A_3A_2A_1A_0 = 1001$
$B_3B_2B_1B_0 = 1100$
Then $S_3S_2S_1S_0 = 0101$, with $C_4 = 1$

The above example is to help you review how the adder works. It is **not** a part of the test.

The following 4-bit adder has signals A_3, B_3, A_2, B_2, S_1, and S_0 and C_4 assigned to active low. All other signals are assigned active high.



(a) We applied the above **VOLTAGE** values to add two binary numbers. What two binary numbers are we trying to add?

A_3 = ___ (0 or 1) A_2 = ___ (0 or 1) A_1 = ___ (0 or 1) A_0 = ___ (0 or 1)

B_3 = ___ (0 or 1) B_2 = ___ (0 or 1) B_1 = ___ (0 or 1) B_0 = ___ (0 or 1)

(b) What **VOLTAGE** values (i.e., high H or low L) do you expect for $S_3S_2S_1S_0$ and C_4?

S_3 = ___ (H or L) S_2 = ___ (H or L) S_1 = ___ (H or L) S_0 = ___ (H or L)

C_4 = ___ (H or L)

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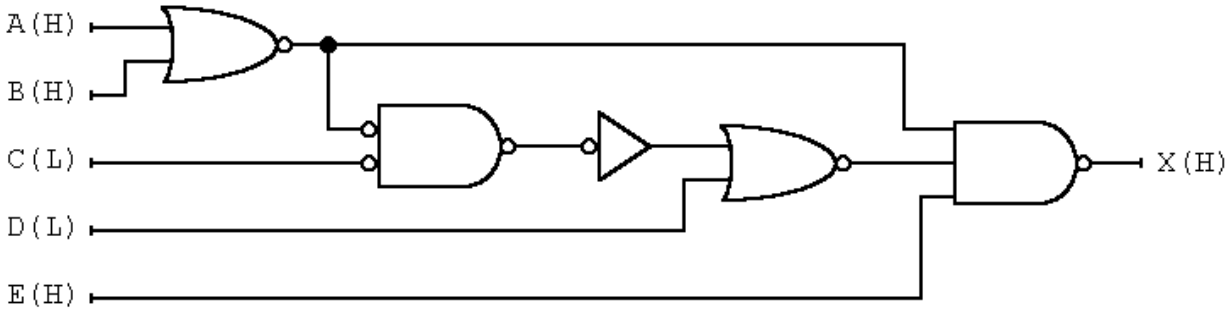
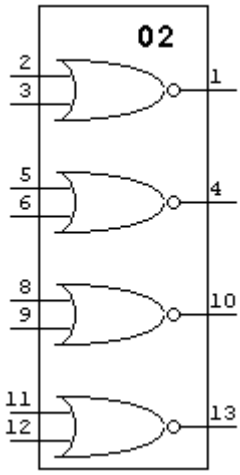
[7%] 5. Determine the equation **directly** implemented with this mixed-logic circuit. Do **not** minimize the equation. It is **not** necessary to put the equation in lexical order. For partial credit, label the intermediate signals from each gate.



X = _____

[10%] 6. Directly implement the below equation with a mixed-logic circuit diagram. Use only gates available on 74'02 chips. (Use the appropriate mixed-logic symbols). **Label** all gates and **pin numbers** as you should be doing in lab. Pick whatever activation levels you want for the inputs, but make the output W active-low.

$$W = (G * /A * T) + (/O * R * /S)$$



G( )__

A( )__

T( )__

O( )__

R( )__

S( )__

__W(L)

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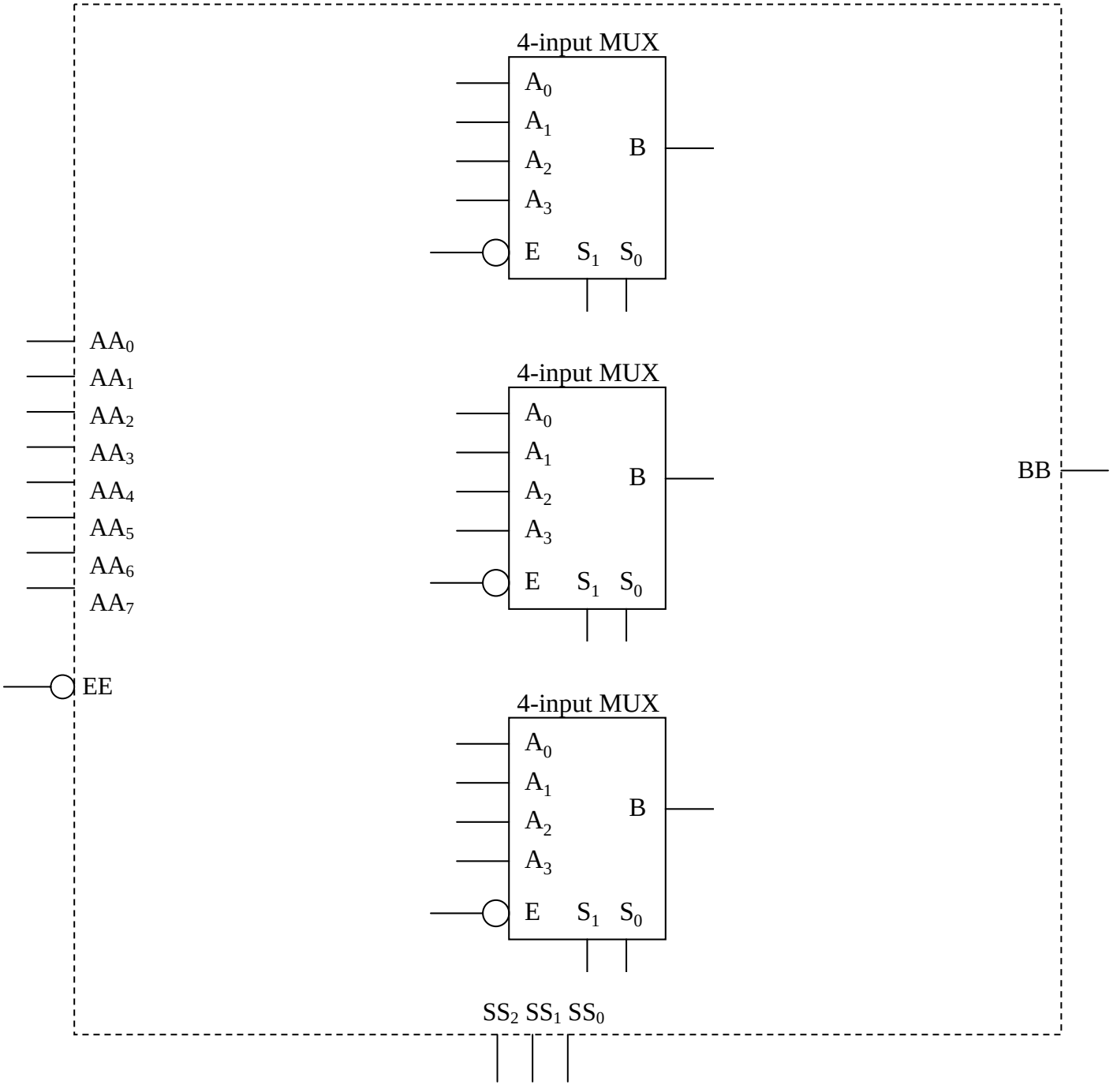
[12%] 7. Create an equivalent 8-input multiplexer using 4-input multiplexer**s** (see truth table), and using the **minimum number** of **components**. You can use additional gates if necessary. However, each gate counts as a component. A 4-input MUX also counts as one component.

E	**S_1**	**S_0**	**A_3**	**A_2**	**A_1**	**A_0**	**B**
0	*	*	X	X	X	X	Hi-Z
1	0	0	X	X	X	0	0
1	0	0	X	X	X	1	1
1	0	1	X	X	0	X	0
1	0	1	X	X	1	X	1
…	…	…	…	…	…	…	…



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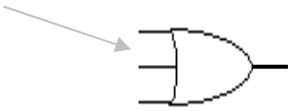
[12%] 8. Implementation of Logic with Decoders

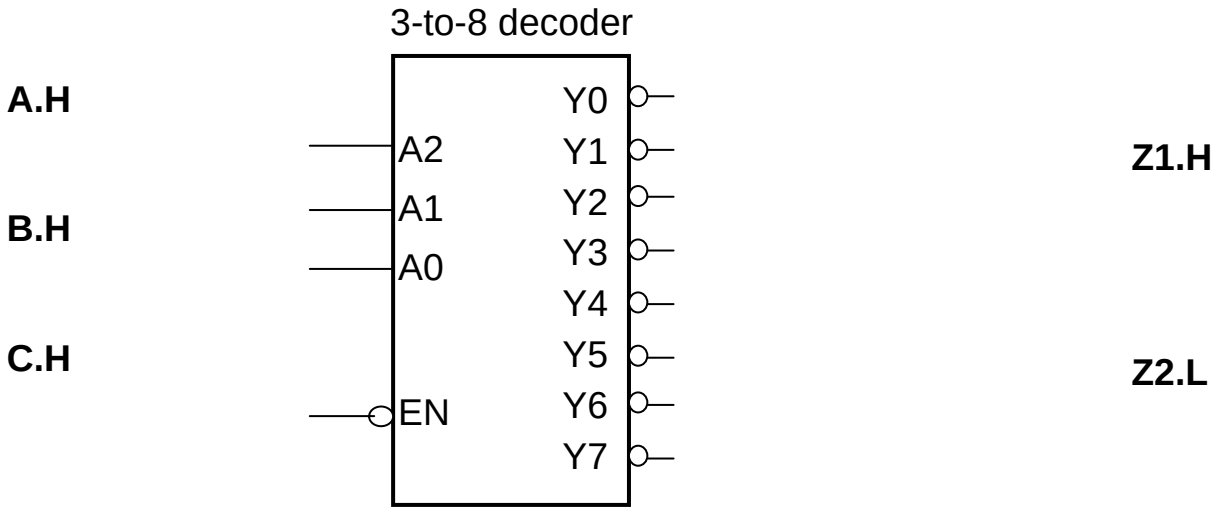
Given the following 2 logic equations and activation levels for the signals, implement them with the following decoder and any number of 3-input OR gates (**ONLY**).



- For maximum credit, use the minimum number of gates.
- Just draw the gates. You don't have to label them (e.g., like 7411)
- Note the * is the AND operator and /A is "NOT A".
- Signals A, B, C, and Z1 are active high, Z2 is active low.

Z1 = /A*/B*/C + A*/B*C + /A*B

Z2 = (/A+B+C) * (A+B)



For partial credit, show work here:

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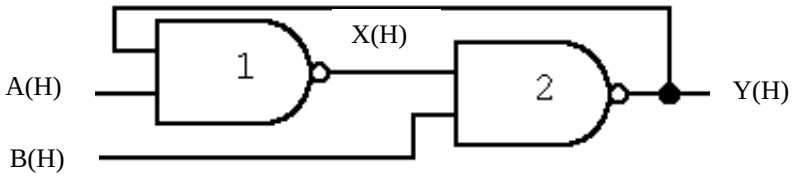
[8%] 9. Given the following simple circuit consisting of two NAND gates, derive the next state **voltage** table (use L and H) for the device. In other words, given each combination of voltage values for A, B, and X, what are the values for X and Y **after the circuit becomes stable**?



(a)

A	B	X	X^+	Y^+

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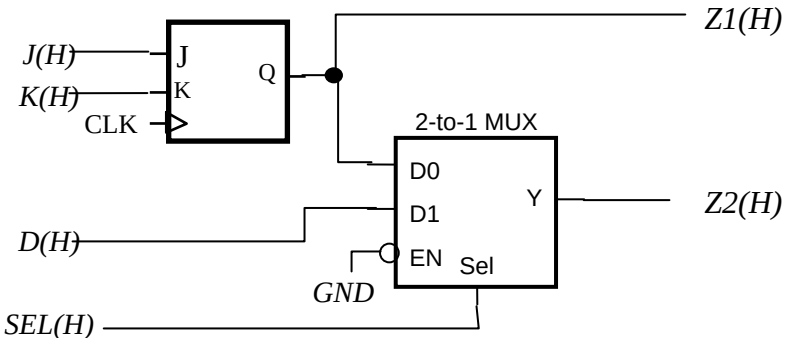
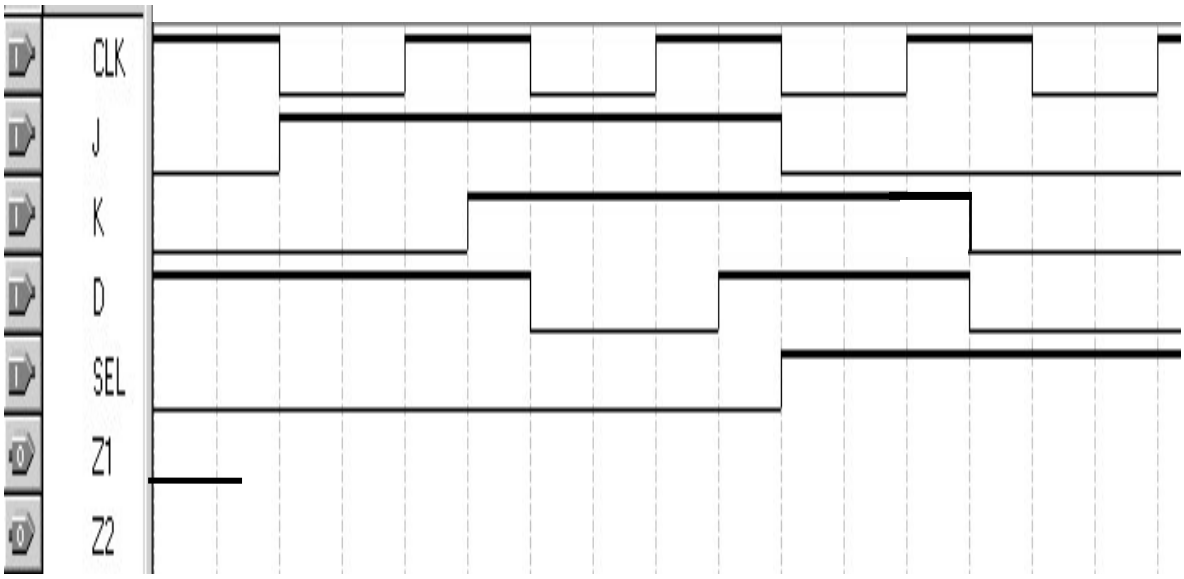
[8%] 10. Synchronous component (flip-flop) vs. combinatorial component (MUX)



Given the above circuit, complete the following **voltage** timing diagrams:



Show propagational delays and go as far as you can.

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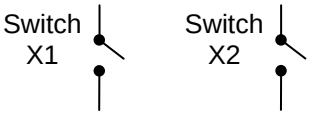
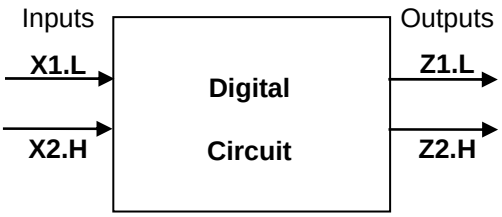
[8%] 11. Building switches and LEDs

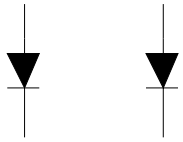
[4%] (a) Shown below are two switches X1 and X2. Complete the design of the two switches to generate two input signals: active low **X1.L** and active high **X2.H**. In other words, make the connections among the switches, resistors, VCC, and GND to produce the two signals.

[2%] (b) Coming out of the digital circuit are two output signals. Make the connections among the LED's, resistors, VCC, and GND to display the active low output Z1.L to an active low LED and the active high output Z2.H to an active high LED. An LED should be lit when the corresponding output is "true".

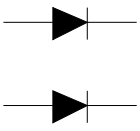
[2%] (c) The TA wants to see LEDs on the input signals. Make the connections among the LED's, resistors, VCC, and GND to display the active low input X1.L to an active low LED and the active high input X2.H to an active high LED. An LED should be lit when the corresponding input is "true".







LEDs



LEDs

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Laws and Theorems of Boolean Algebra

Operations with 0 and 1:

1. X + 0 = X
2. X + 1 = 1

1D. X • 1 = X
2D. X • 0 = 0

Idempotent laws:

3. X + X = X

3D. X • X = X

Involution laws:

4. (X')' = X

Laws of complementarity:

5. X + X' = 1

5D. X • X' = 0

Commutative laws:

6. X +Y = Y + X

6D. XY=YX

Associative laws:

7. (X +Y) + Z = X + (Y + Z) = X + Y + Z

7D. (XY)Z = X(YZ) = XYZ

Distributive laws:

8. X(Y + Z) =XY + XZ

8D. X + YZ = (X +Y)(X + Z)

Simplification theorems:

9. XY + XY' = X
10. X + XY = X
11. (X + Y')Y = XY

9D. (X + Y)(X + Y') = X
10D. X(X + Y) = X
11D. XY' + Y = X + Y

DeMorgan's laws:

12. (X + Y + Z + …)' = X'Y'Z'

12D. (XYZ…)' = X' + Y' + Z'

13. [f(A, B, …, Z, 0, 1, +, •)]' = f(A', B', …, Z', 1, 0, •, +)

Duality:

14. $(X + Y + Z + \ldots)^D = XYZ\ldots$

14D. $(XYZ\ldots)^D = X + Y + Z + \ldots$

15. $[f(A, B, \ldots, Z, 0, 1, +, \bullet)]^D = f(A, B, \ldots, Z, 1, 0, \bullet, +)$

Theorems for multiplying out and factoring:

16. (X + Y)(X' + Z) = XZ + X'Y

16D. XY + X'Z = (X +Z)(X' +Y)

Consensus theorems:

17. XY +YZ +X'Z = XY +X'Z

17D. (X + Y)(Y + Z)(X' + Z) = (X + Y)(X' +Z)