EEL 3701—Fall 2008
Monday, 6 October 2008

Drs. Lam, Schwartz and Arroyo

Exam 1

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Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *This exam counts for 24% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page and be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*
- *The point values for problems may be changed at prof's discretion*
- *Notation reminder: A(H) is the same as A.H..*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good Evening! Welcome!

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

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SIGN YOUR NAME

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DATE (6 Oct 2008)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2	6	
3	14	
4	12	
5	12	
6	16	
7	12	
8	18	
9	10	
TOTAL	100	

Exam 1

____
Last Name, First Name

[6%] 1. Do the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(2%) a) Determine the unsigned binary, octal, hexadecimal, and BCD representations of the number 99_{10}.

Binary: ____________________

Octal: ____________________

Hex: ____________________

BCD: ____________________

(2%) b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -19_{10}.

Signed Mag: ________________

1's Comp: ________________

2's Comp: ________________

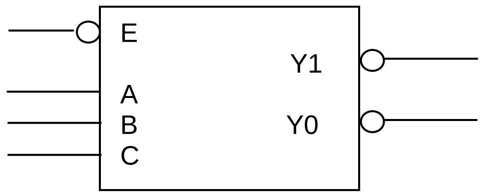
(2%) c) What is 99_{10} -100_{10} in 8-bit 2's complement? Remember that you must **show <u>all</u> work.**

$(99_{10}-100_{10})_2$: ______________

Exam 1

____
Last Name, First Name

[14%] 2. You are given the following new MSI device:



Inputs: E.L, A.H, B.H, C.H

Outputs: Y1.L, Y0.L

We would like to implement the following logic table:

E	A	B	C	Y1	Y0
0	X	X	X	0	0
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	0	0
1	1	1	0	0	1
1	1	1	1	0	0

(a) What are the logic equations for Y1 and Y0? Y1 should be in MSOP and Y0 MPOS.

Y1 (MSOP) = ____ (4%)

Y0 (MPOS) = ____ (4%)

(b) Draw the mixed-logic circuit diagram required to implement the logic equations for **Y0** (you don't have to implement Y1). Use minimum number of gates. (6%)

<u>Use only NAND gates (and their alternative views).</u>

Exam 1

____

Last Name, First Name

[12%] 3. Using any technique you desire, simplify the following equation. Give the result as a minimum product of sums (MPOS). **Show all work!**

$$\mathbf{Z = \overline{(\overline{A}+B+\overline{C})\bullet(A+\overline{C})} + \overline{A}\bullet B\bullet(\overline{C} + C\bullet\overline{D})}$$

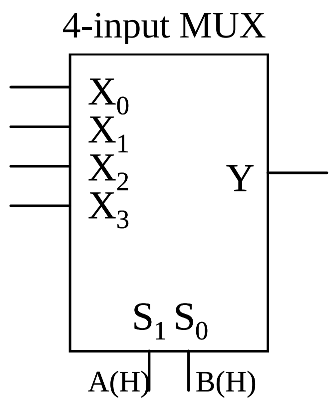
Z_{MPOS} = ____

Exam 1

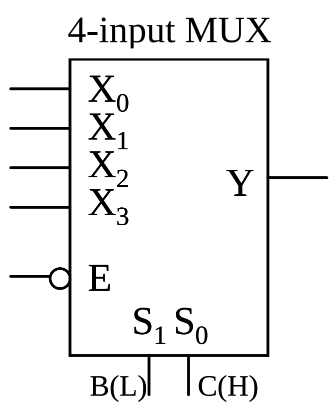
____
Last Name, First Name

[12%] 4. Use the given 4-input multiplexers to solve each of the below problems. Choose a single activation level (either active high or active low) for each of the inputs and outputs for each problem. Use the minimum number of additional components. Show all work and draw any required mixed logic circuit diagrams (i.e., equations must not be used as replacements for circuit diagrams).

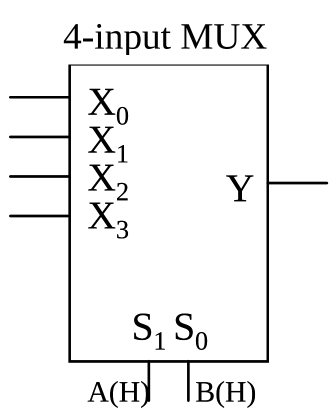
(4%) a) Z_0 = A*B + A*C*/D



(4%) b) Z_1 = A*B + A*C*/D (Notice the enable available on this MUX.)



(4%) c) Use the given 4-input multiplexer to implement Z_2, which is defined by the voltage table.



A	B	C	D	Z_2
L	L	L	L	L
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	L
L	H	H	L	H
L	H	H	H	L
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	H

EEL 3701—Fall 2008
Monday, 6 October 2008

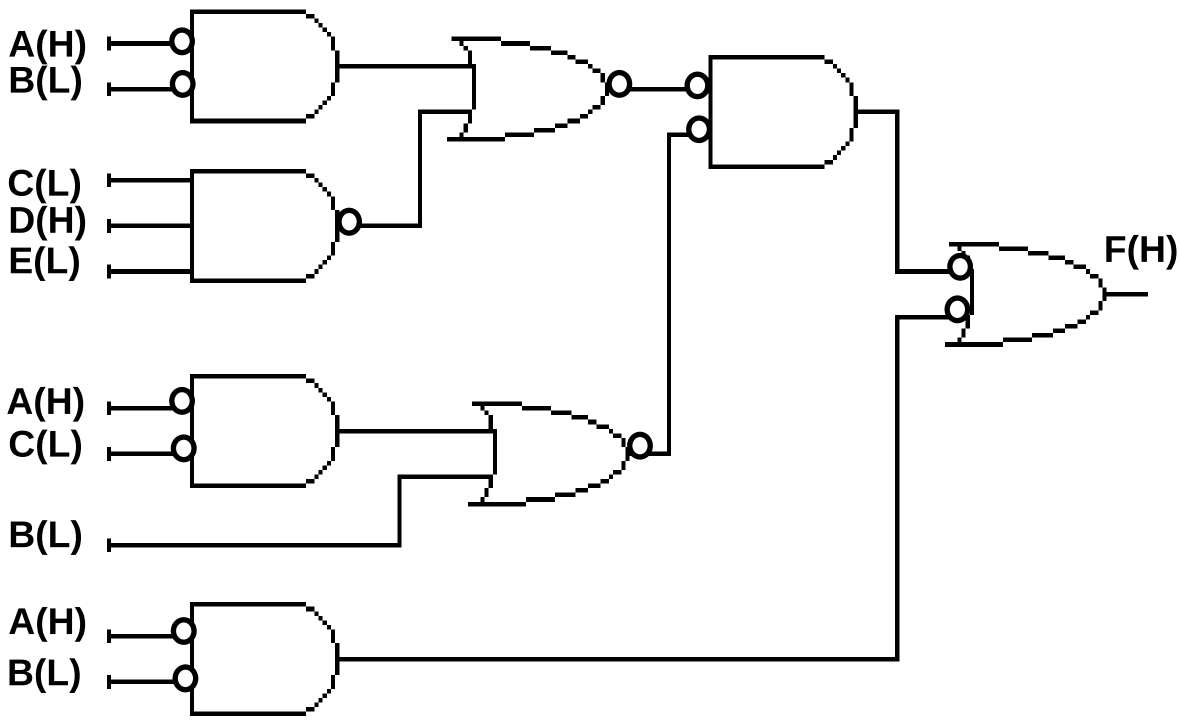
Drs. Lam, Schwartz and Arroyo

Exam 1

____

Last Name, First Name

[8%] 5. Determine the equation **directly** implemented with this mixed-logic circuit. Do **not** minimize the equation. It is **not** necessary to put the equation in lexical order. For partial credit, label the intermediate equations at the input to each gate.



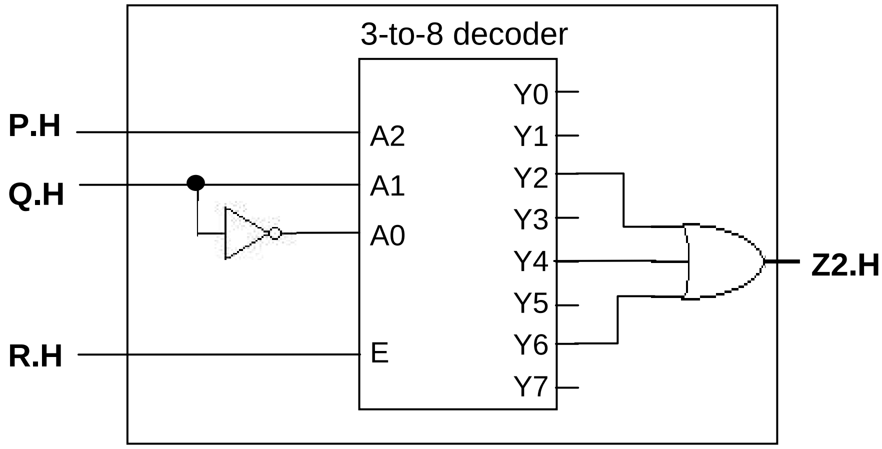
F = ____

EEL 3701—Fall 2008
Monday, 6 October 2008

Exam 1

____
Last Name, First Name

[8%] 6 Analyze the following circuit and produce a ***logic*** expression for **Z2.**



- For this problem, the expression for **Z2** should be in **minimum SOP (MSOP)** form.
- Z2 should be a function of P, Q, and R.
- For credit, show all work.

Z2 =

EEL 3701—Fall 2008
Monday, 6 October 2008

Drs. Lam, Schwartz and Arroyo

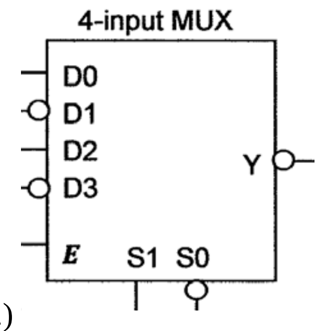
Exam 1

____

Last Name, First Name

[12%] 7. MUX, logic vs. voltage.

Show below is a block diagram of a "custom-built" 4-input MUX, with a mixture of active high and active low inputs and output.



(a) Give the logic equation for Y. (2 pts.)

(b) Give the ***voltage*** table for the MUX. For maximum credit: (8 pts.)

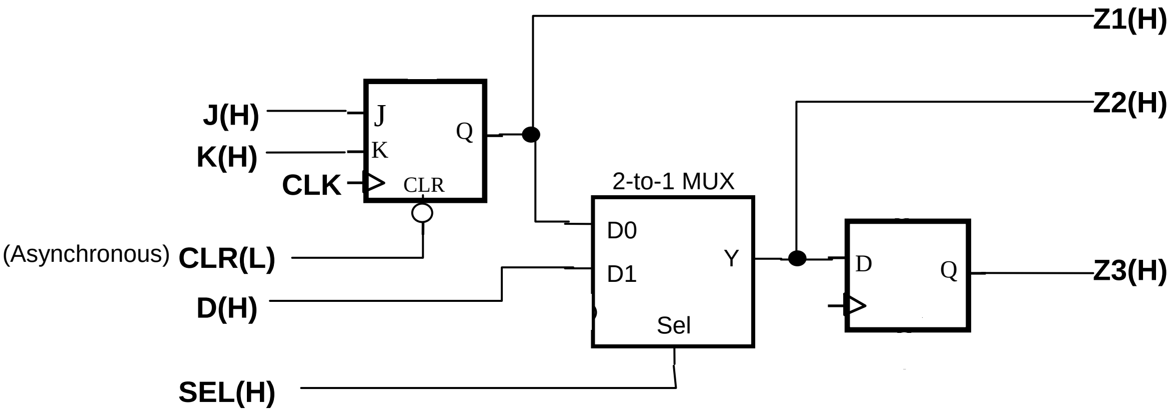
- Order the voltage table in the "standard" order (E,S1,S0,D0,D1,D2,D3).
- Use "wild cards" or "don't cares" to condense the table.

(c) Visualize the logic equation of a 64-to-1 MUX. Give me the first 2 product terms of that equation and the last 2 product terms of that equation. (2 pts.)

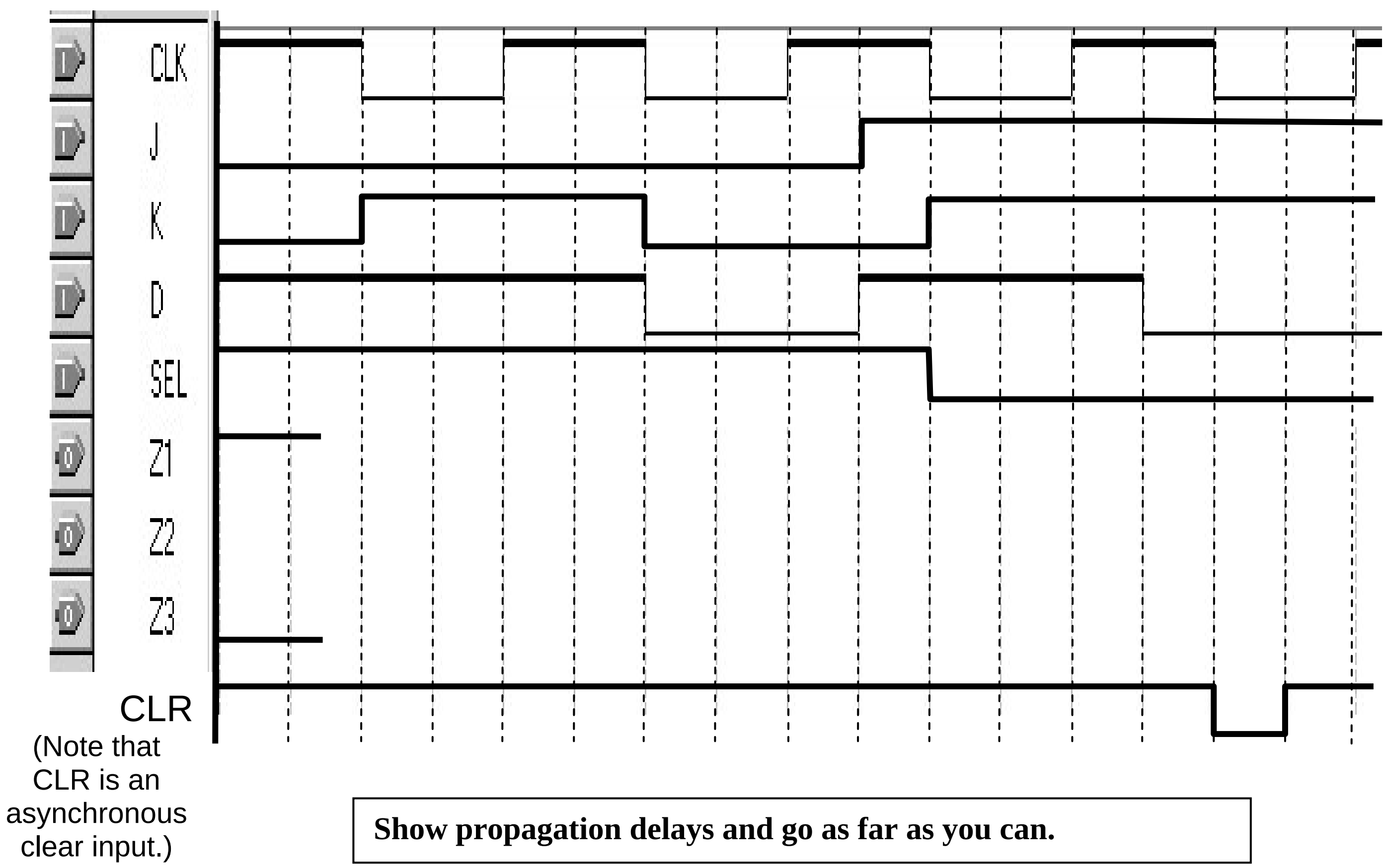
First two product terms:

Last two product terms:

[18%] 8. Circuit analysis and flip-flops.

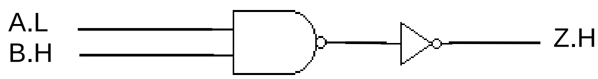


Given the above circuit, complete the following ***voltage*** timing diagrams.



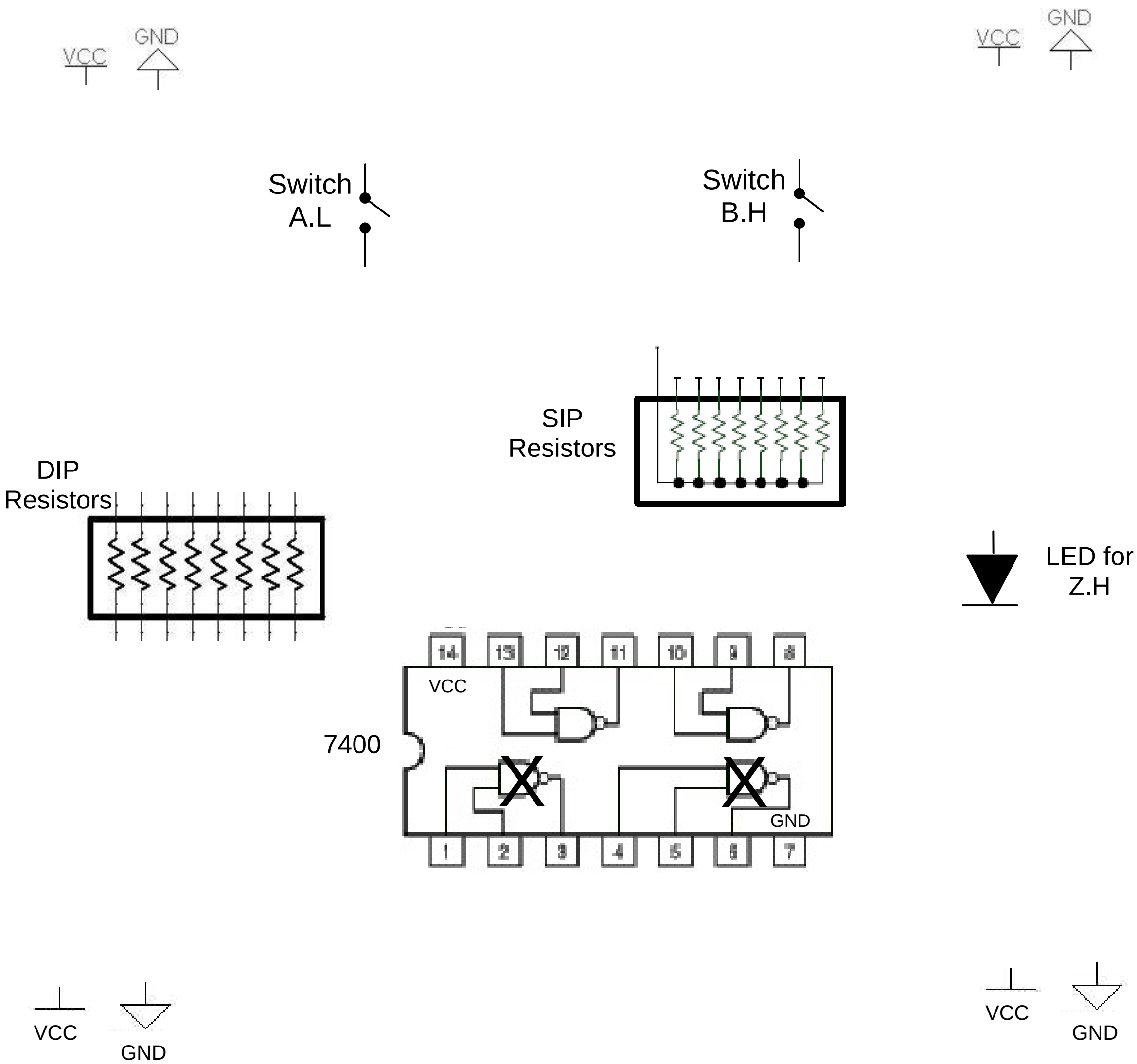
Show propagation delays and go as far as you can.

[10%] 9. Building switch and LED circuits.



Given the above circuit, implement the circuit on the "board" below using the given components. In other words, pretend that you are actually "wiring" your board in the lab and draw in the "wires"

- Make <u>all</u> the necessary connections, including all VCC and GND connections.
- For ease of grading, use only the top 2 NAND gates.
- Be sure to draw each switch in the position (i.e., open or close) for which the switch produce a "True" value.



Exam 1

____

Last Name, First Name

Laws and Theorems of Boolean Algebra

Operations with 0 and 1:

1. $X + 0 = X$ — 1D. $X \bullet 1 = X$
2. $X + 1 = 1$ — 2D. $X \bullet 0 = 0$

Idempotent laws:

3. $X + X = X$ — 3D. $X \bullet X = X$

Involution laws:

4. $(X')' = X$

Laws of complementarity:

5. $X + X' = 1$ — 5D. $X \bullet X' = 0$

Commutative laws:

6. $X + Y = Y + X$ — 6D. $XY = YX$

Associative laws:

7. $(X + Y) + Z = X + (Y + Z) = X + Y + Z$ — 7D. $(XY)Z = X(YZ) = XYZ$

Distributive laws:

8. $X(Y + Z) = XY + XZ$ — 8D. $X + YZ = (X + Y)(X + Z)$

Simplification theorems:

9. $XY + XY' = X$ — 9D. $(X + Y)(X + Y') = X$
10. $X + XY = X$ — 10D. $X(X + Y) = X$
11. $(X + Y')Y = XY$ — 11D. $XY' + Y = X + Y$

DeMorgan's laws:

12. $(X + Y + Z + \ldots)' = X'Y'Z'$ — 12D. $(XYZ\ldots)' = X' + Y' + Z'$
13. $[f(A, B, \ldots, Z, 0, 1, +, \bullet)]' = f(A', B', \ldots, Z', 1, 0, \bullet, +)$

Duality:

14. $(X + Y + Z + \ldots)^D = XYZ\ldots$ — 14D. $(XYZ\ldots)^D = X + Y + Z + \ldots$
15. $[f(A, B, \ldots, Z, 0, 1, +, \bullet)]^D = f(A, B, \ldots, Z, 1, 0, \bullet, +)$

Theorems for multiplying out and factoring:

16. $(X + Y)(X' + Z) = XZ + X'Y$ — 16D. $XY + X'Z = (X + Z)(X' + Y)$

Consensus theorems:

17. $XY + YZ + X'Z = XY + X'Z$ — 17D. $(X + Y)(Y + Z)(X' + Z) = (X + Y)(X' + Z)$