University of Florida
Department of Electrical & Computer Engineering

EEL 3701—Fall 2006
Wednesday, 4 October 2006

Drs. Lam, Schwartz and Arroyo

Exam 1

_____

Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *This exam counts for 24% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page and be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*
- *The point values for problems may be changed at prof's discretion*
- *Notation reminder: A(H) is the same as A.H..*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs/outputs of each gate with the appropriate logic equations.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good Evening! Welcome!

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (4 Oct 2006)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2	6	
3	10	
4	10	
5	10	
6	17	
7	12	
8	15	
10	10	
11	10	
TOTAL	100	

Exam 1

_____
Last Name, First Name

[6%] 1. Do the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(2%) a) Determine the unsigned binary, octal, hexadecimal, and BCD representations of the number 49_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(2%) b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -73_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) c) What is 49_{10} -73_{10} in 8-bit 2's complement? Remember that you must **show <u>all</u> work.**

$(49_{10}-73_{10})_2$: _____

Exam 1

Last Name, First Name

[10%] 2. Answer the following questions given the below **truth table** with inputs W, X and Y and output Z.

W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(2%) a) Write the corresponding **minterm** (i.e., **canonical** sum of products CSOP) –***or***– **maxterm** (i.e., **canonical** product of sums CPOS) equation for Z (one or the other, but not both).

Which did you write above? (circle one): Minterms (CSOP) Maxterm (CPOS)

(1%) b) Completely fill in the K-map (to the right) with 1's and 0's (no blanks).

(2%) c) With the K-map to the right, find the minimum sum of products (MSOP) solution. (Label each grouping with the appropriate expression and then write the total equation. Use proper lexical ordering; *i.e., /A before A, A before B, & D_3 before D_2*.)

XY / W	00	01	11	10
0				
1				

Z_{MSOP} = _____

(3%) d) Completely fill in the K-map (to the right) with 1's and 0's (no blanks) and find the minimum product of sums (MPOS) solution. **Note**: The order of the signals in the K-map has been changes! (WX is on top)

WX / Y	00	01	11	10
0				
1				

Z_{MPOS} = _____

(1%) e) Are Z_{MSOP} and Z_{MPOS} equivalent expressions? Why?

Circle One: Yes (equivalent) No (not equivalent)

(1%) f) Which solutions is less costly (in gates) and why? **Circle One**: MSOP MPOS

Exam 1

Last Name, First Name

[10%] 3. Using any technique you desire, simplify the following equation. Give the result as a minimum sum of products (MSOP).

$$Y = \left(\overline{A} + B + C + D\right) \bullet \left(A + B + \overline{C} + \overline{D}\right) \bullet \left(A + D\right) \bullet \left(\overline{B} + \overline{D}\right) \bullet \left(B + \overline{C} + D\right)$$

Y_{MSOP} = _____

Exam 1

Last Name, First Name

[10%] 4. Using a 4-input multiplexer (i.e., 4-to-1 multiplexer) and any other gates, draw a mixed-logic circuit diagram to realize the following function. (Do **not** attempt to simplify.) Minimize the **number of gates** required. You may choose any activation-levels that will simplify your design.

The 4-to-1 multiplexer has all active-high inputs and an active-high output.

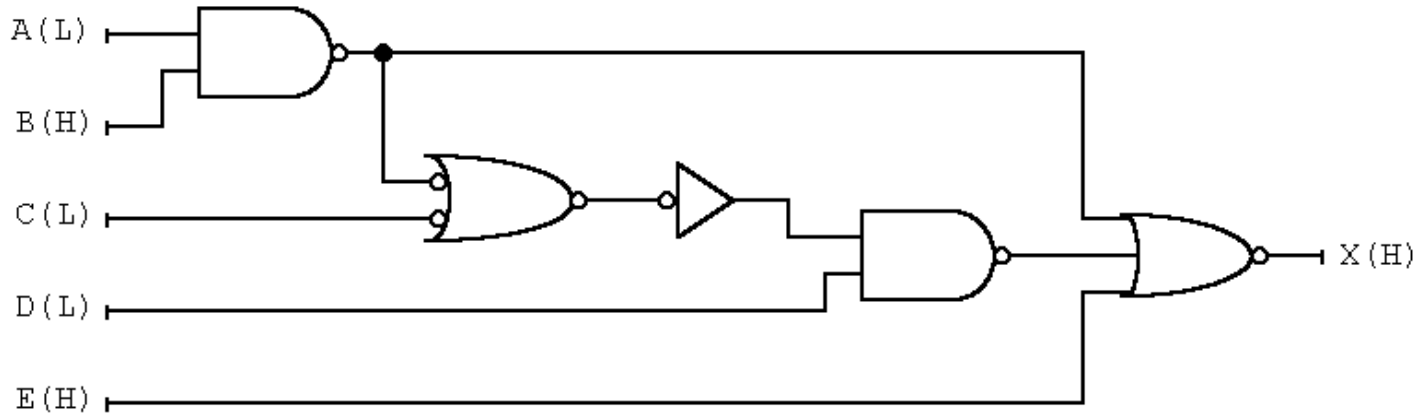
$$Y = \overline{A}\,\overline{B}C + \overline{A}B\overline{C}D + \overline{B}\,\overline{C}$$

Note: you must connect A to S1 of the 4-input mux and B to S0.

Exam 1

Last Name, First Name

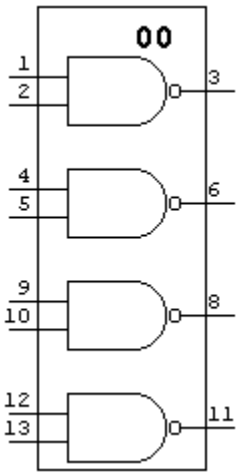
[7%] 5. Determine the equation **directly** implemented with this mixed-logic circuit. Do **not** minimize the equation. It is **not** necessary to put the equation in lexical order. For partial credit, label the intermediate signals from each gate.



X = _____

[10%] 6. Directly implement the below equation with a mixed-logic circuit diagram. Use only gates available on 74'00 chips. (Use the appropriate mixed-logic symbols). **Label** all gates and **pin numbers** as you should be doing in lab. Pick whatever activation levels you want for the inputs, but make the output Y active-high.

$$Y = (A * K * /B + E) * /(/R * T)$$



A( )__

K( )__

B( )__

E( )__

R( )__

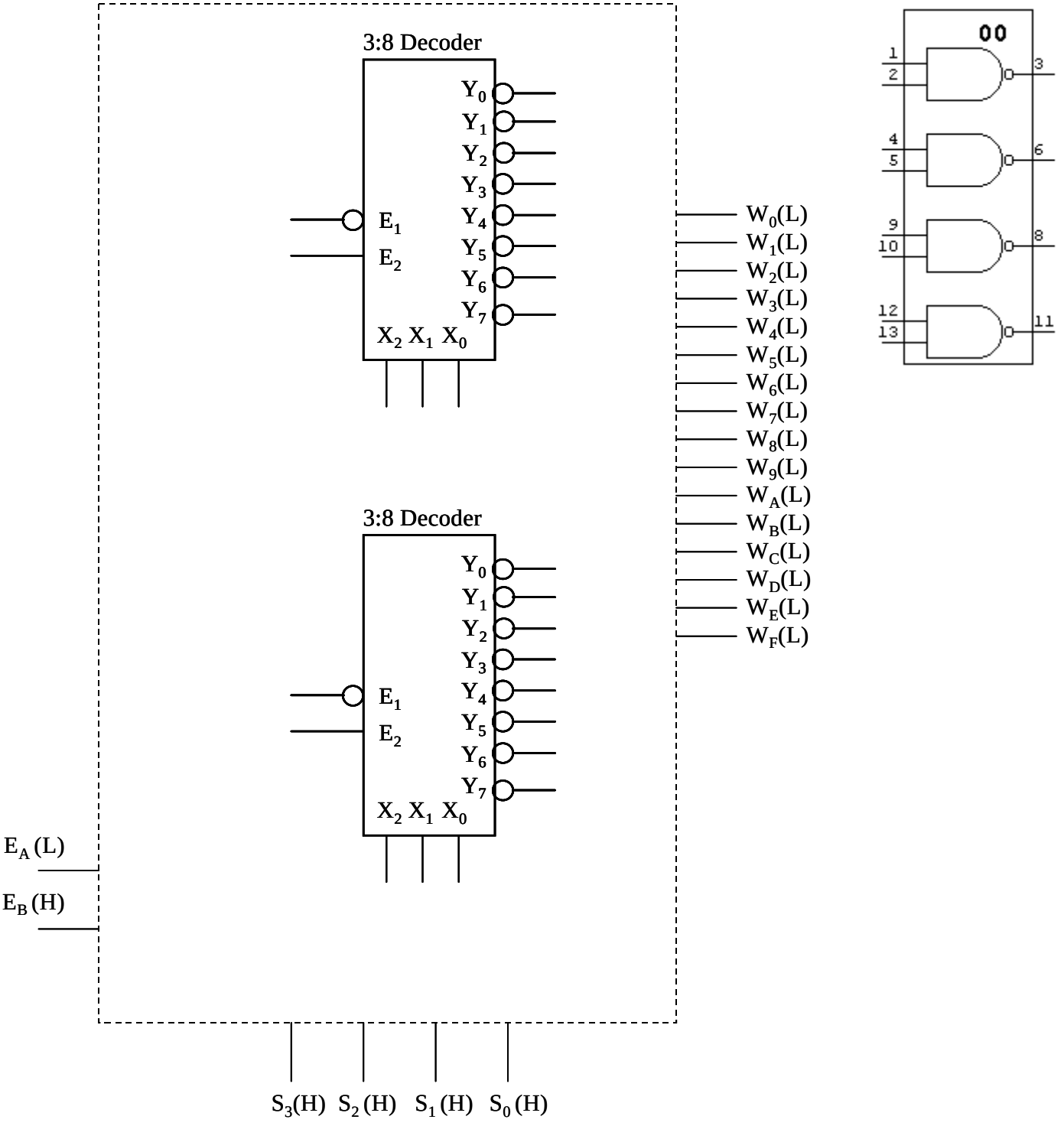
T( )__

__Y(H)

Exam 1

Last Name, First Name

[12%] 7. Given the two 3-to-8 decoders shown (each containing an active-low **and** an active-high enable), create a 4-to-16 decoder, also with an active-high **and** an active-low enable. Use **only** the gates available on **74'00** chips. (A 74'00 is shown.) Add the **minimum** number of additional 74'00 gates required to solve this problem. Note that both E1 and E2 have to be true before the 3:8 Decoder is "on".



Exam 1

Last Name, First Name

[15%] 8. Answer the following questions about the circuit shown on the next page (p. 9).

(5%) a) What is the logic equation of Z in terms of A, B and C? **Simplify** to an MSOP or an MPOS. **Show all work.** Note that Z is active low Z(L). Also, the inputs are active-high A and B and active-low C.

Z = _____

(2%) b) What is the logic equation of D(L) in terms of the inputs A and B (where A is active-high and B is active-low)?

_____

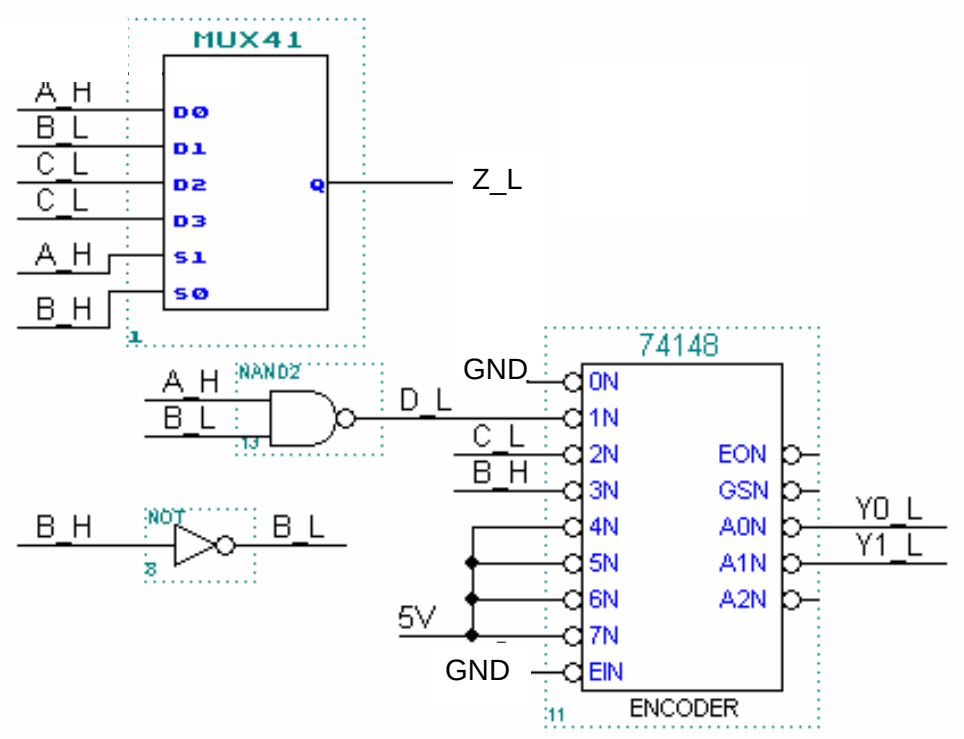
(8%) c) Complete the following **voltage** table. For the priority encoder, higher numbered inputs have higher priority.

A(H)	B(H)	C(L)	D(L)	Z(L)	Y_0(L)	Y_1(L)
L	L	L				
L	L	H				
L	H	L				
L	H	H				
H	L	L				
H	L	H				
H	H	L				
H	H	H				

Exam 1

Last Name, First Name

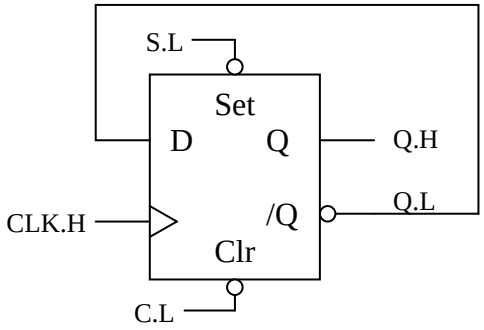
Use this figure for Problem 9 on the previous page (p. 8).



Exam 1

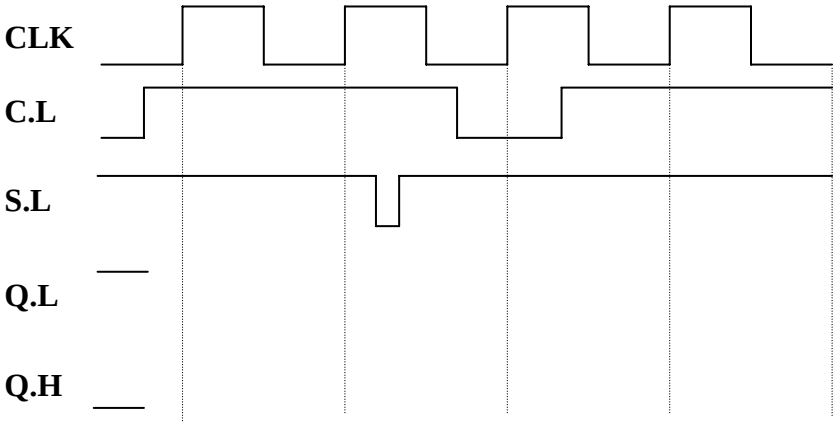
Last Name, First Name

[10%] 9. Given the following circuit, complete the **Voltage** Timing Diagram for Q.L & Q.H below.



Special Notes:
1. Rising edge triggered D Flip-Flop
2. Asynchronous Set & Clear
3. Q.H is initially false

Voltage Timing Diagram. (Fill in Q.L & Q.H.)



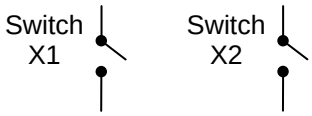
Q.H is initially false.

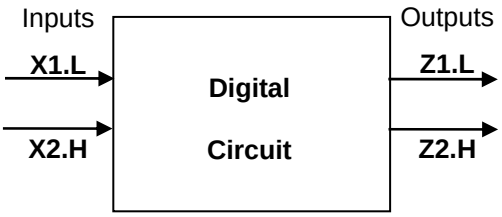
Clearly show all timing delays.

[10%] 10. Building switches and LEDs

[5%] (a) Shown below are two switches X1 and X2. Complete the design of the two switches to generate two input signals: active low **X1.L** and active high **X2.H**. In other words, make the connections among the switches, resistors, VCC, and GND to produce the two signals.

[5%] (b) Coming out of the digital circuit are two output signals. Make the connections among the LED's, resistors, VCC, and GND to display the active low output Z1.L to an active low LED and the active high output Z2.H to an active high LED. An LED should be lit when the corresponding output is "true".





Last Name, First Name

Laws and Theorems of Boolean Algebra

Operations with 0 and 1:

1. X + 0 = X
2. X + 1 = 1

1D. X • 1 = X
2D. X • 0 = 0

Idempotent laws:

3. X + X = X

3D. X • X = X

Involution laws:

4. (X')' = X

Laws of complementarity:

5. X + X' = 1

5D. X • X' = 0

Commutative laws:

6. X +Y = Y + X

6D. XY=YX

Associative laws:

7. (X +Y) + Z = X + (Y + Z) = X + Y + Z

7D. (XY)Z = X(YZ) = XYZ

Distributive laws:

8. X(Y + Z) =XY + XZ

8D. X + YZ = (X +Y)(X + Z)

Simplification theorems:

9. XY + XY' = X
10. X + XY = X
11. (X + Y')Y = XY

9D. (X + Y)(X + Y') = X
10D. X(X + Y) = X
11D. XY' + Y = X + Y

DeMorgan's laws:

12. (X + Y + Z + …)' = X'Y'Z'

12D. (XYZ…)' = X' + Y' + Z'

13. [f(A, B, …, Z, 0, 1, +, •)]' = f(A', B', …, Z', 1, 0, •, +)

Duality:

14. $(X + Y + Z + \ldots)^D = XYZ\ldots$

14D. $(XYZ\ldots)^D = X + Y + Z + \ldots$

15. $[f(A, B, \ldots, Z, 0, 1, +, \bullet)]^D = f(A, B, \ldots, Z, 1, 0, \bullet, +)$

Theorems for multiplying out and factoring:

16. (X + Y)(X' + Z) = XZ + X'Y

16D. XY + X'Z = (X +Z)(X' +Y)

Consensus theorems:

17. XY +YZ +X'Z = XY +X'Z

17D. (X + Y)(Y + Z)(X' + Z) = (X + Y)(X' +Z)