EEL3701 – Dr. Gugel
Fall 2017
Exam #1

Last Name, First Name _____

UF ID#_____

Open book and open notes, ***90-minute*** *examination.* ***No electronic devices are permitted.***

Page 1)	8 points	_____	Page 2)	24 points	_____
Page 3)	18 points	_____	Page 4)	18 points	_____
Page 5)	17 points	_____	Page 6)	16 points	_____
	TOTAL	_____ of 101			

Re-grade requests must be handed in the day exams are returned in class. *Write the problem number you wish reviewed.* ***A maximum of three review problems is allowed.*** *Do not write anywhere else on the exam other than below or you will receive a zero on the exam.*

1. Problem No. _____

2. Problem No. _____

3. Problem No. _____

1. Given a **16 bit Signed Hex** number, **FAB4**, what is it equivalent to in decimal? Note: You may express your answer as a sum of powers of 16. i.e. $5 \times 16^5 + 2 \times 16^1 + \ldots$ (2 pt.)

_____

_____

2. A student would like to use their **SIP (Single Inline Package) R-Pack** from lab as a group of **pull down** resistors for inputs A, B, C, D, E and F. Draw the device below and show/label all pins & connections. (2 pt.)

3. A student would like to add (6) **8 bit Unsigned** numbers. How many bits are required in the final answer such that no carry is generated and the final sum is correct? Hint: Solve for a smaller word length. (2 pt.)

4. When subtracting (3) **10 bit Signed** numbers (A – B – C), how many bits are required in the final answer such that no overflow will occur? Hint: Solve for a smaller word length. (2 pt.)

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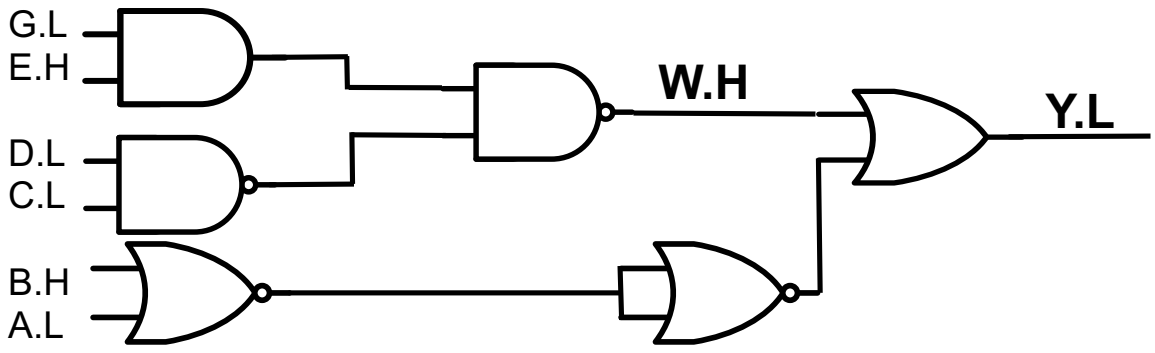
5 – 7. Perform the following addition, subtraction and multiplication as required below. (7 pt.)

1 1 1 1 1 1	1 1 0 1 1 0 1 0 1	1 0 1 1 1 . 1 0 1
1 0 1 1 0 1	- 0 1 1 1 0 1 0 1 1 1	x 1 0 0 1 . 0 1
+ 0 1 0 1 1 1		

8. Directly synthesize a circuit for the following equation using only ***3 Input AND gates*** and ***Inverters***. (9 pt.)

$$Y = \overline{\overline{A} + (\overline{B+C}) * \overline{E} + D}$$; A.H, B.L, C.H, D.L, E.H, Y.L **Do Not Simplify the Equation!**

9. Derive the logic equations for the following signals listed after the circuit below. ***Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!***

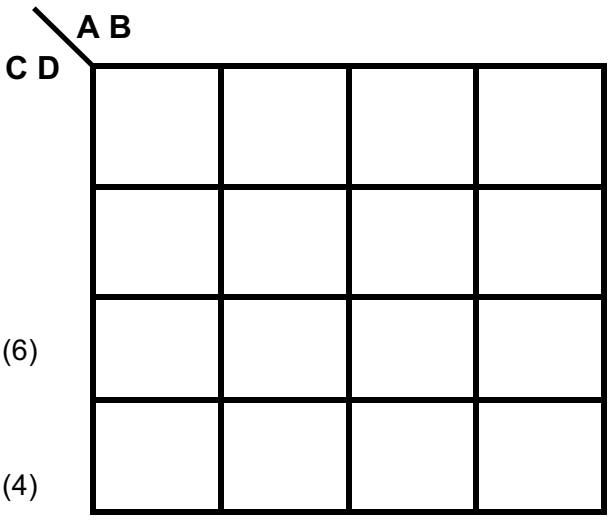


W.H = _____ (5 pt.)

Y.L = _____ (3 pt.)

10. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map.

$$\bar{A}BC + AB\bar{C}\bar{D} + A\bar{B}\bar{C} + B\bar{C}D + \bar{A}\bar{C}\bar{D}$$



Y (MSOP) = _____ (6)

Y (MPOS) = _____ (4)

11. Simplify the logic equation from #10 above using Boolean Identities. Show all your steps for full credit. You don't have to specify which Boolean Identity you are using but do have to show all intermediate steps. (8 pt.)

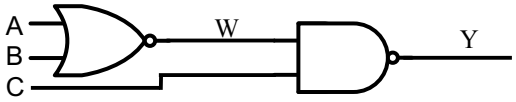
Page Score =

12. Simplify the equation below with **De Morgan's Rule** and **Boolean Identities** to find the **MSOP**. (10 pt.)

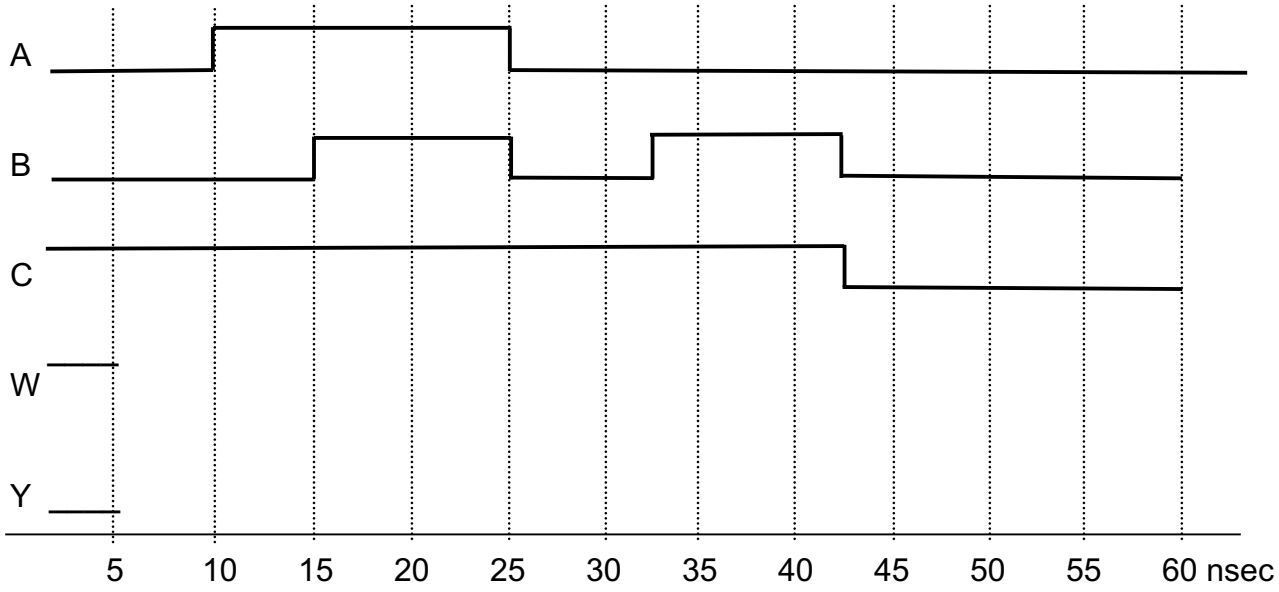
$$Y = \overline{(\overline{A}+\overline{C})(A+B)(\overline{B}+D+E)(B+\overline{C})(B+D+E)(\overline{A}+\overline{B}+D+E)}$$

Y = _____ **MSOP**

14. Given the circuit below complete the voltage timing diagram for signals X and Y. Assume all devices have a **10 nsec** propagation delay. (8 pt.) **Assume A = B = Y = L, C = W = H initially.**



Gate Propagation Delay is 10nsec!



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Design a **Signed Comparator** that compares a **2 bit Signed number A1:0** with a **3 bit Signed number B2:0**. The outputs therefore should be A = B, A > B and A < B. Assume all inputs and outputs are high true.

15. Fill in the Logic Truth Table below for the device. Use don't cares 'Xs" in the inputs to reduce the number of rows and write the A = B cases first on top followed by the A>B cases and then finally the A<B cases for the bottom rows. Note: ***Failure to follow the directions will result in receiving less points.*** (12 pt.)

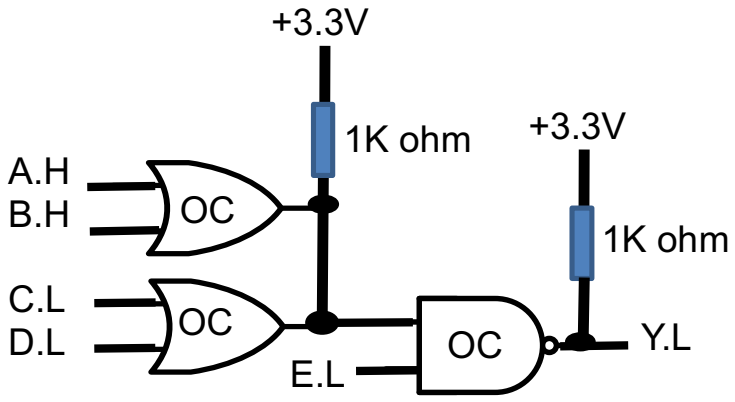
A1	A0	B2	B1	B0	A = B	A > B	A < B

16. Write the **Minimum Sum of Products (MSOP)** for the **A = B** output below. (2 pt.)

17. Write the **Minimum Sum of Products (MSOP)** for the **A > B** output below. (3 pt.)

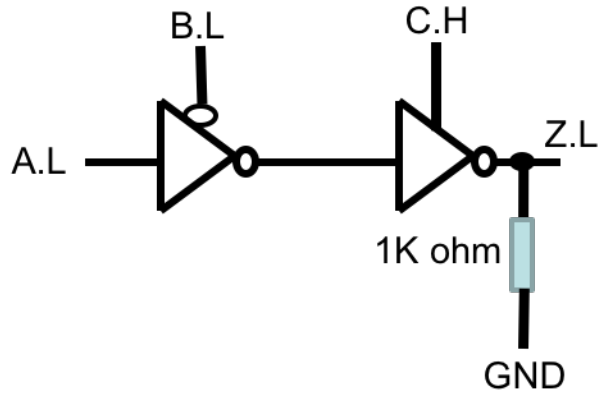
Page Score =

18. For the circuit below, derive the **MSOP logic equation** for **Y.L**. ***Note: Simplify as a Sum of Products!*** (4 pt.)



Y.L = _____ **MSOP**

19. For the circuit below, derive the **MSOP logic expression** for **Z.L** **Simplify as a Min. Sum of Products!** (4 pt.)



Z.L = _____ **MSOP**

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