EEL3701 – Dr. Gugel **_Last Name, First Name_** _____
Fall 2018
Exam #1 *Open book and open notes,* ***90-minute*** *examination.* ***No electronic devices are permitted.***

Page 1)	13 points	_____	Page 2)	25 points	_____
Page 3)	19 points	_____	Page 4)	15 points	_____
Page 5)	16 points	_____	Page 6)	12 points	_____
	TOTAL	_____ of 100			

Re-grade requests must be handed in the day exams are returned in class. *Write the problem number you wish reviewed.* ***A maximum of three review problems is allowed.*** *Do not write anywhere else on the exam other than below or you will receive a zero on the exam.*

1. Problem No. _____

2. Problem No. _____

3. Problem No. _____

1. Perform the following binary additions and subtractions by hand. For full credit, ***show all your work below.*** Assume the numbers are all ***unsigned binary***. (3,2,3 pt.)

```
  111111        10101010        1101.001
  101010      - 01111011      x 100.110
+ 111111
```

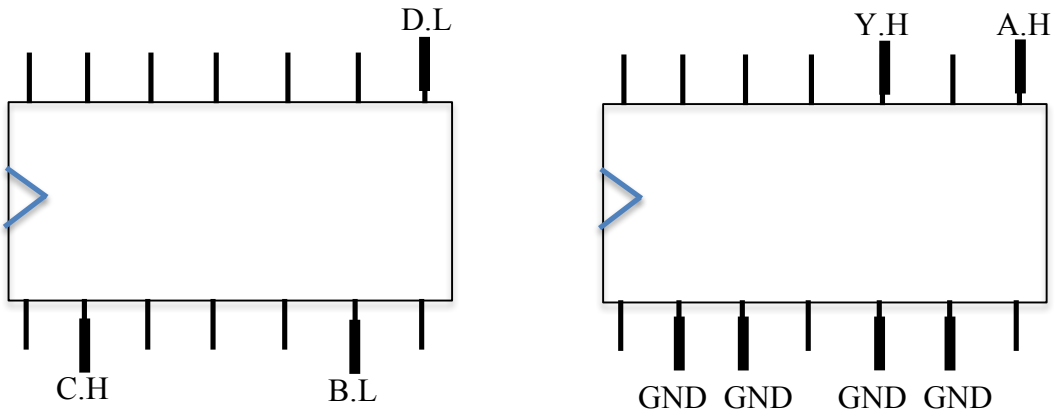
2. Write **-27** as a **16 bit Signed Hex** number. (2 pt.)

3. When multiplying (2) **8 bit Signed** numbers (A * B), how many bits are required in the final answer such that no overflow will ever occur? Hint: Solve for a smaller word length. (3 pt.)

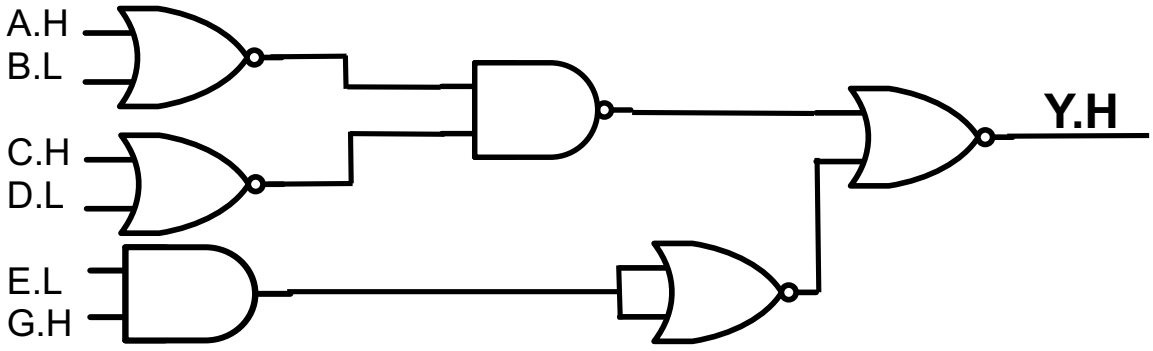
4. Directly synthesize a circuit for the following Logic Equation using only ***2 Input NOR gates***. (9 pt.)

$Y = \overline{\overline{A} + ((\overline{B+C}) * D)}$; A.L, B.L, C.H, D.L, Y.H **Do Not Simplify the Equation!**

5. Show the **ALL the CONNECTIONS** below to implement the above circuit in the two 74HC02 NOR ICs below. (7 pts.)



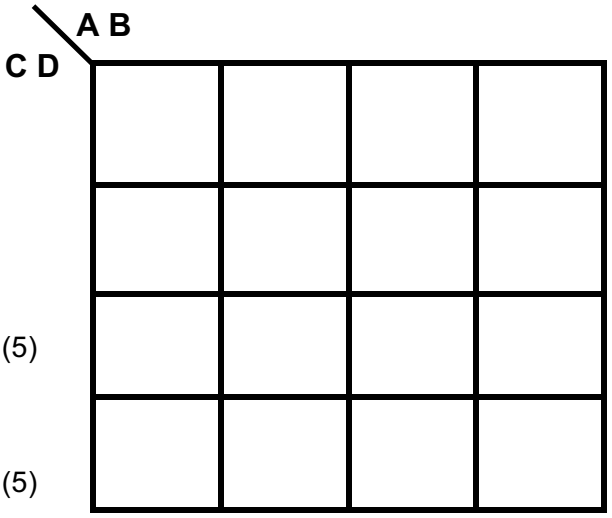
9. Derive the logic equations for the following signals listed after the circuit below. ***Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!***



Y.H = _____ (9 pt.)

10. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map.

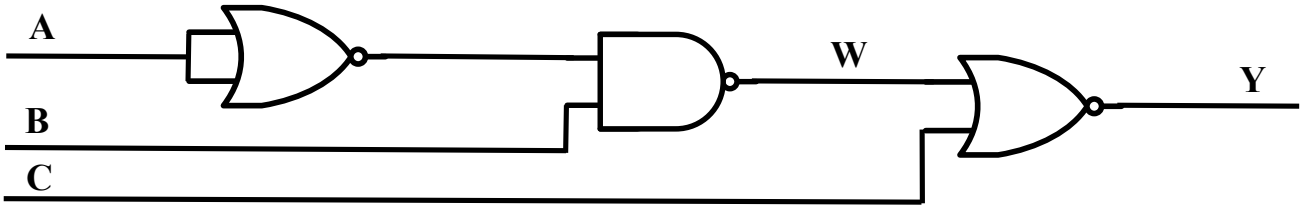
$$(B+C+D)(\overline{A}+B+\overline{C}+D)(A+\overline{C}+\overline{D})(\overline{B}+\overline{D})(A+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{D})$$

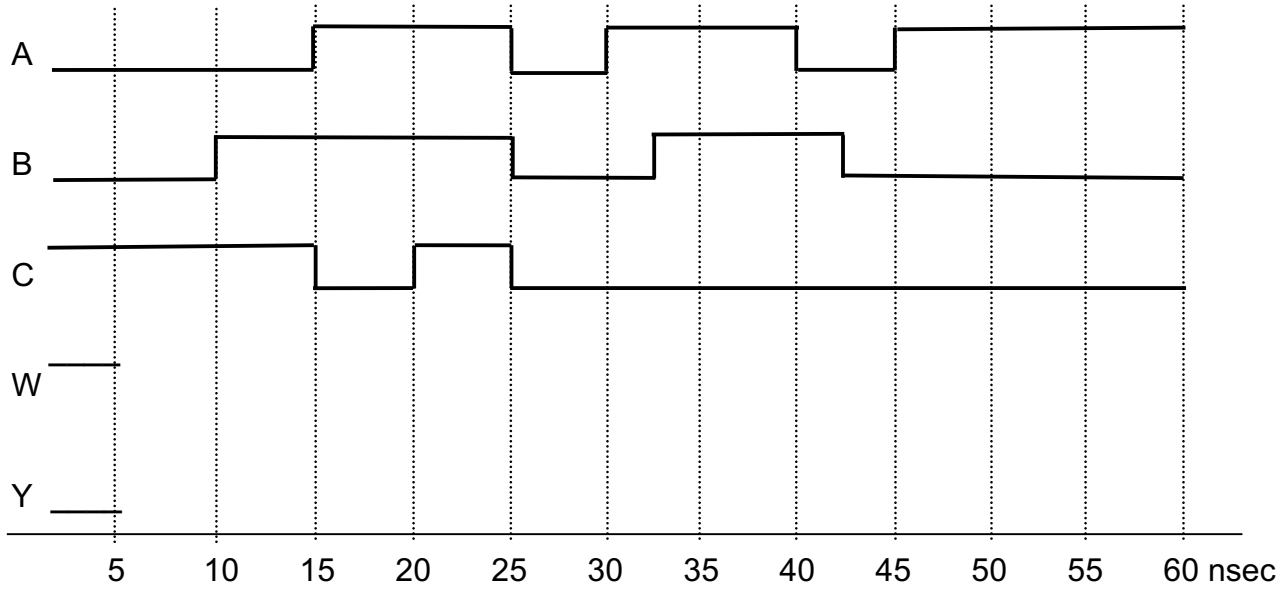


Y (MSOP) = _____ (5)

Y (MPOS) = _____ (5)

11. Given the circuit below complete the ***voltage timing diagram*** for signals X and Y. Assume all devices have a **10 nsec** propagation delay. (9 pt.) **Assume A = B = Y = L, C = W = H initially.**





=>| t_p 10 ns |<=

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12. Simplify the equation below with **De Morgan's Rule** and **Boolean Identities** to find the **MSOP**. (10 pt.)

$$P = \overline{(\overline{W}*X)(\overline{W}*\overline{Y}*\overline{Z})(V*W*\overline{Y}*\overline{Z})(V*X)(\overline{V}*\overline{W})(W*\overline{Y}*\overline{Z})}$$

Y = _____ **MSOP**

13. Lucky #%$@##! 13! Perform the following ***Unsigned Binary division*** below by hand. ***Show at least 6 fractional binary bits in your answer.*** (5 pt.)

11.01 ⟌ 10111.101

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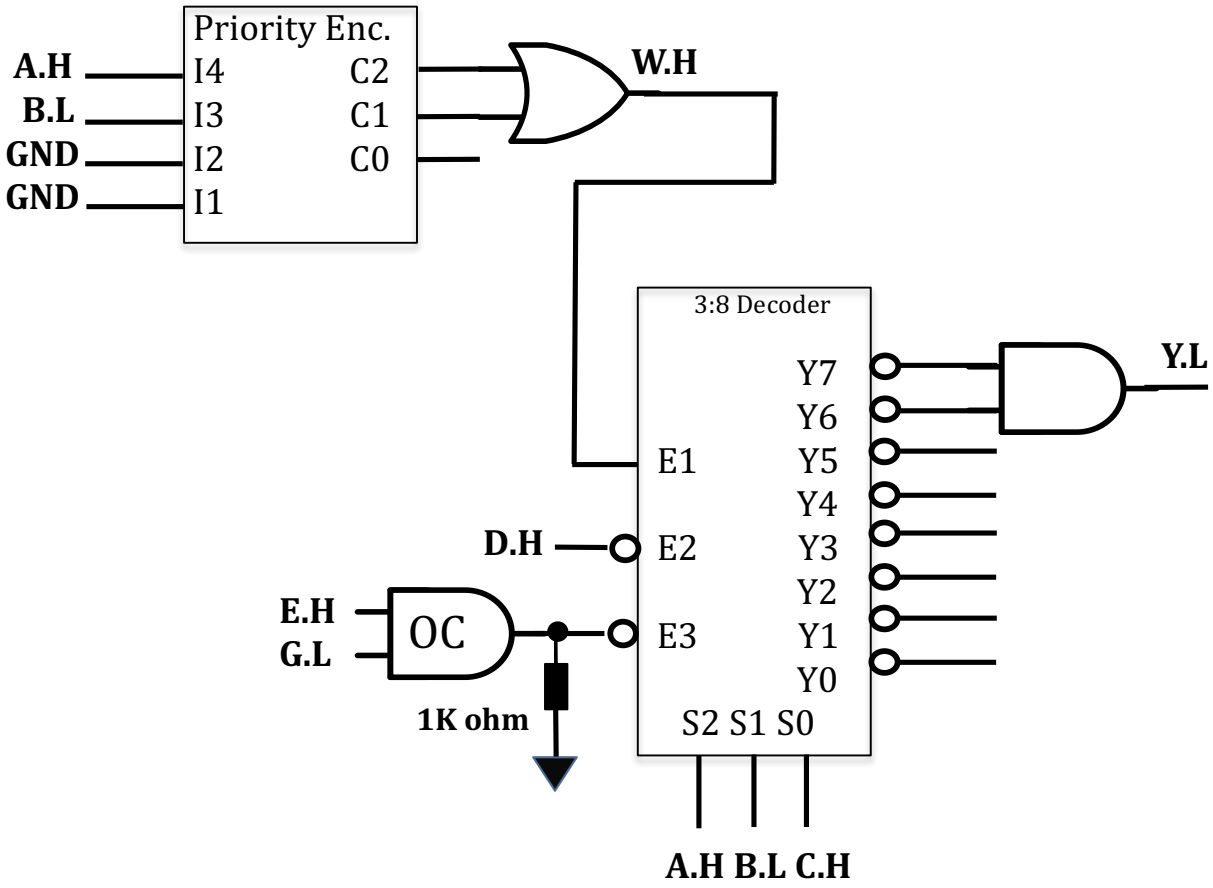
14. For the circuit below find the **MSOP for W.H and Y.L**. (10 pt.)



W.H = _____ **MSOP** (3 pt.)

Y.L = _____ **MSOP** (7 pt.)

15. Implement the logic equation **Z = A*/B*/C** (Z.L, A.L, B.H, C.L) in hardware using **Open Collector Inverters** and **1K ohm** resistors. (6 pt.)

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16A. Design a **Signed Multiplier** that **multiplies a 3 bit signed (2's complement) number by -7**. The input is therefore a 3 bit signed number and output should be the input value multiplied by a constant (-7) Assume all inputs & outputs are high true. Create a Logic Truth Table below for the device below. (8 pt.)

16B. Determine the MSOP logic equation for the output Most Significant Bit (MSB). (4 pt.)