EEL3701 – Dr. Gugel **_Last Name, First Name_** _____
Spring 2017
Exam #1 UF ID#_____

Open book and open notes, ***90-minute*** *examination.* ***No electronic devices are permitted.***

Page 1)	9 points	_____	Page 2)	23 points	_____
Page 3)	18 points	_____	Page 4)	17 points	_____
Page 5)	18 points	_____	Page 6)	15 points	_____
	TOTAL	_____ of 100			

Re-grade requests must be handed in the day exams are returned in class. *Write the problem number you wish reviewed.* ***A maximum of three review problems is allowed.*** *Do not write anywhere else on the exam other than below or you will receive a zero on the exam.*

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_____

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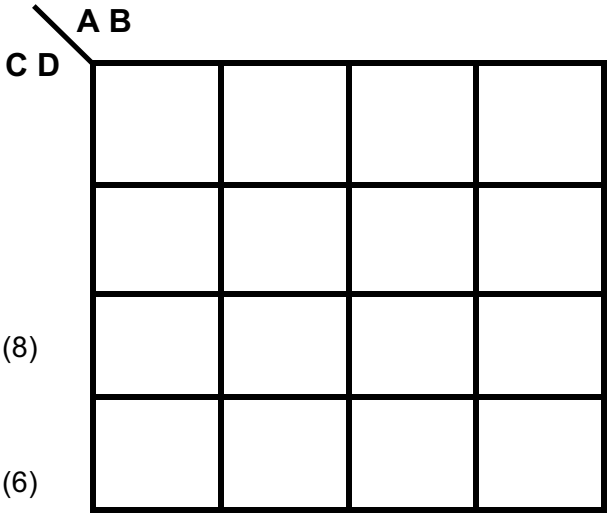
1. Directly synthesize a circuit for the following equation using only **2 Input NOR** gates only. (9 pt.)

$$Y = \overline{\overline{A} * (\overline{B*C}) + E + \overline{D}}$$; A.L, B.H, C.L, D.H, E.L, Y.H **Do Not Simplify the Equation!**

2. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map. (14 pt.)

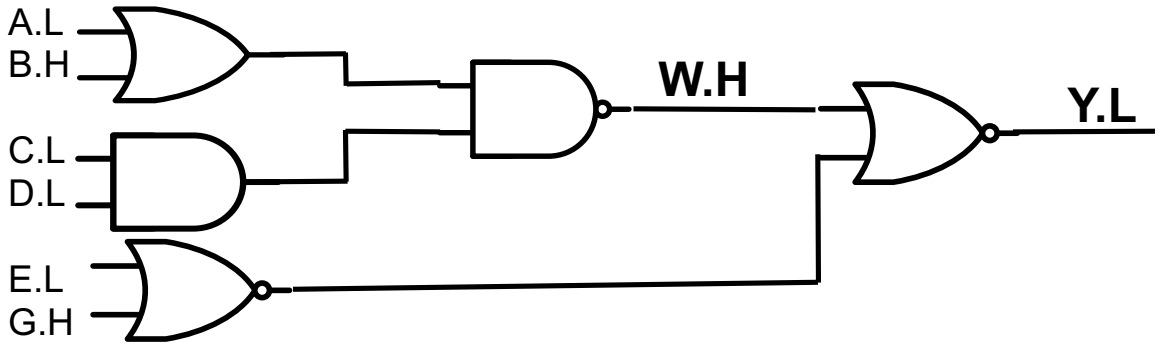
$$Y = (A+B+C+D)(/A+/B+C+D)(/A+C+D)(B+/C+D)(A+/B+/D)$$



Y (MSOP) = _____ (8)

Y (MPOS) = _____ (6)

3. Derive the logic equations for the following signals listed after the circuit below. ***Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!***



W.H = _____ (5 pt.)

Y.L = _____ (4 pt.)

Page Score =

4. Simplify the equation below with **De Morgan's Rule** and **Boolean Identities** to find the **MSOP**. (10 pt.)

$$\overline{Y = (X+Y+Z)(\overline{X}+\overline{Y}+\overline{W})(X+\overline{Z}+W)(X+\overline{Z})(\overline{X}+Z+\overline{W})(\overline{X}+Y+Z)}$$

Y = _____ **MSOP**

5. A student would like to design a **multiplier** that computes the product of a **2 bit unsigned number** times a **3 bit unsigned number**. i.e. P = M1:0 x N2:0 ;where all numbers are unsigned binary

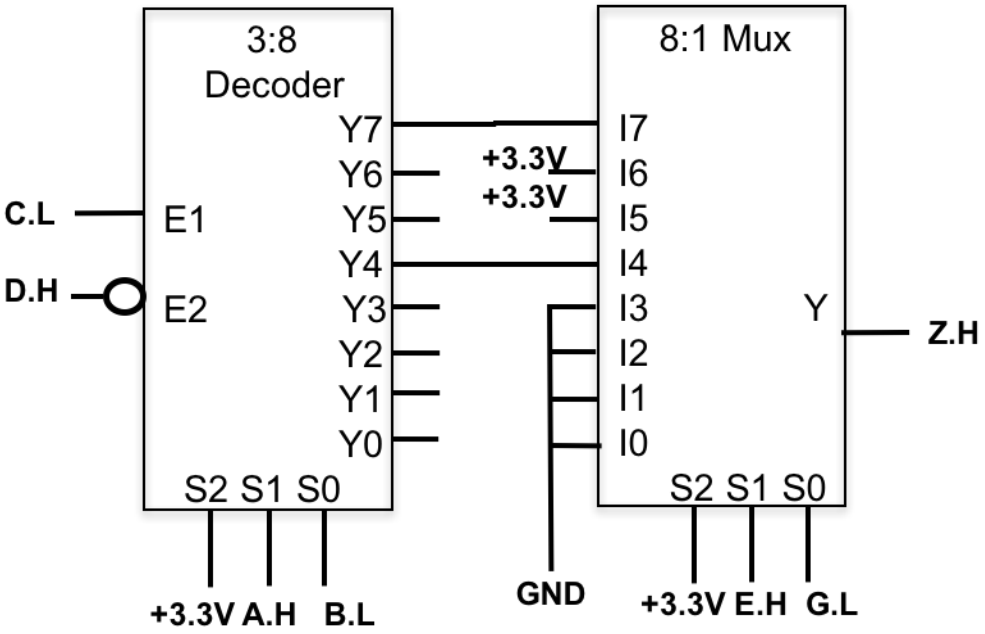
How many bits are required for P? _____ (2 pt.)

Write the **Canonical Sum of Products (CSOP)** for the **most significant bit of P** based on inputs **M1:0** and **N2:0** below. (8 pt.)

6 – 8. Perform the following addition, subtraction and multiplication. (9 pt.)

111001	10010001	10101.01
101101	- 01111110	x 101.01
+ 111111		

9. For the circuit below, derive the logic equation for Z.H. **Do not Simplify!** (8 pt.)



Z.H = _____

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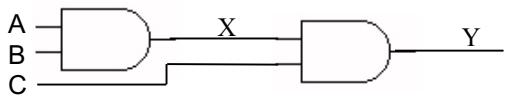
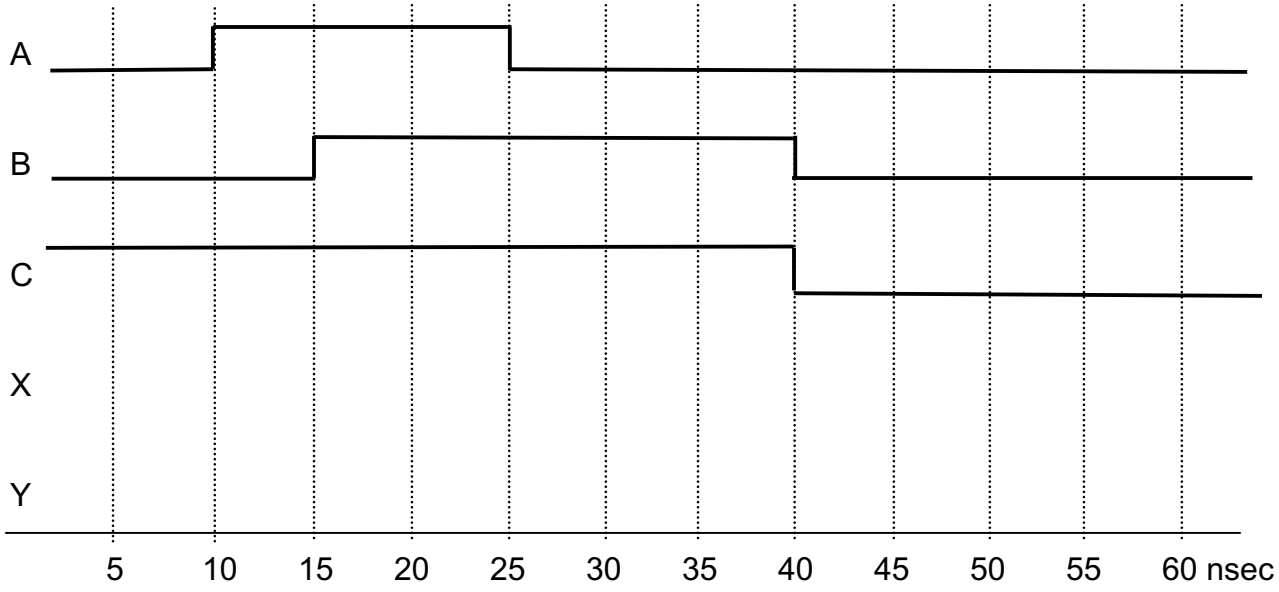
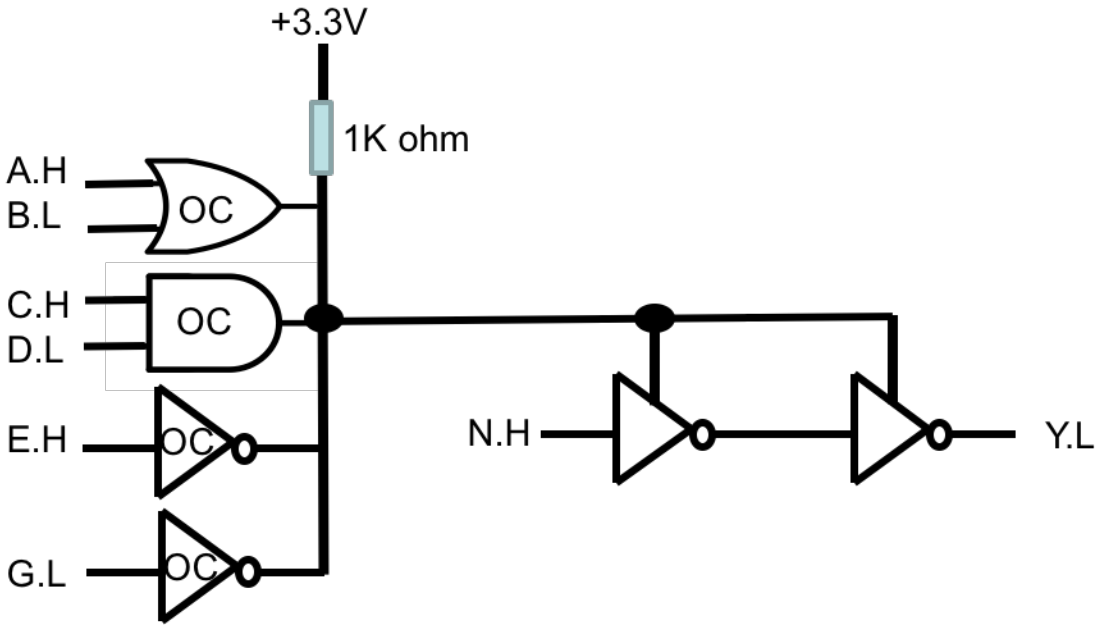
10. Given the circuit below complete the voltage timing diagram for signals X and Y. Assume all devices have a **10nsec** propagation delay. (8 pt.) **Assume A=L, B=L, C=H initially.**



Gate Propagation Delay is 10nsec!



11. For the circuit below derive the ***logic equation for Y*** and ***add the required missing Pull-up or Pull-down resistor*** to make Y a function of A,B,C,D, E, G and N. (10 pt.)



Y.L = _____

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12. Create a device that decrements a ***4 bit Signed Number*** by 1. **N3:0** is the **signed input** and **M3:0** is the **signed output** equivalent to **N3:0 – 1**. For example, if a "3" is input to the device, the output should be "2". One additional output, V, should also be generated that indicates when an overflow occurs. For example, if decrementing an input by 1 creates an overflow condition, output V = 1, otherwise V = 0.

Draw the truth table for the device below:

N3	N2	N1	N0	M3	M2	M1	M0	V

(10 pt.)

Derive the MSOP Logic Equation for **M0** and **V** (5 pt.):

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