EEL3701 – Dr. Gugel
Fall 2018
Exam #1

Last Name, First Name KEY

Open book and open notes, ***90-minute*** *examination.* ***No electronic devices are permitted.***

Page 1)	13 points	________	Page 2)	24 points	________
Page 3)	19 points	________	Page 4)	15 points	________
Page 5)	16 points	________	Page 6)	13 points	________
	TOTAL	________ of 100			

Re-grade requests must be handed in the day exams are returned in class. *Write the problem number you wish reviewed.* ***A maximum of three review problems is allowed.*** *Do not write anywhere else on the exam other than below or you will receive a zero on the exam.*

1. Problem No. ________________________________

2. Problem No. ________________________________

3. Problem No. ________________________________

1. Perform the following binary additions and subtractions by hand. Show all your work below. Assume the numbers are all ***unsigned binary***. (3,2,3 pt.)

```
    1 1
   10101
   111111           01010122 (borrows)
   101010           10101010            1101.001     13.125
 + 111111         - 01111011          x  100.110     4.75
 --------         ----------          ----------
 10101000           0101111             110.10010    62.34375
                                      + 011.01001
 10101000                               110100.10000
                                      ------------
                                        111110.01011
                                          62   .34375
```

2. Write **-27** as a **16 bit Signed Hex** number. (2 pt.)

27 = 16+11   100100
1B   011011 +1
             100101

FFE5

3. When multiplying (2) **8 bit Signed** numbers (A * B), how many bits are required in the final answer such that no overflow will ever occur? Hint: Solve for a smaller word length. (3 pt.)

N=4
1000 = -8 → 01000000
$(-8)^2 = 64$ ↑ sign bit
N=4, Need 8 bits

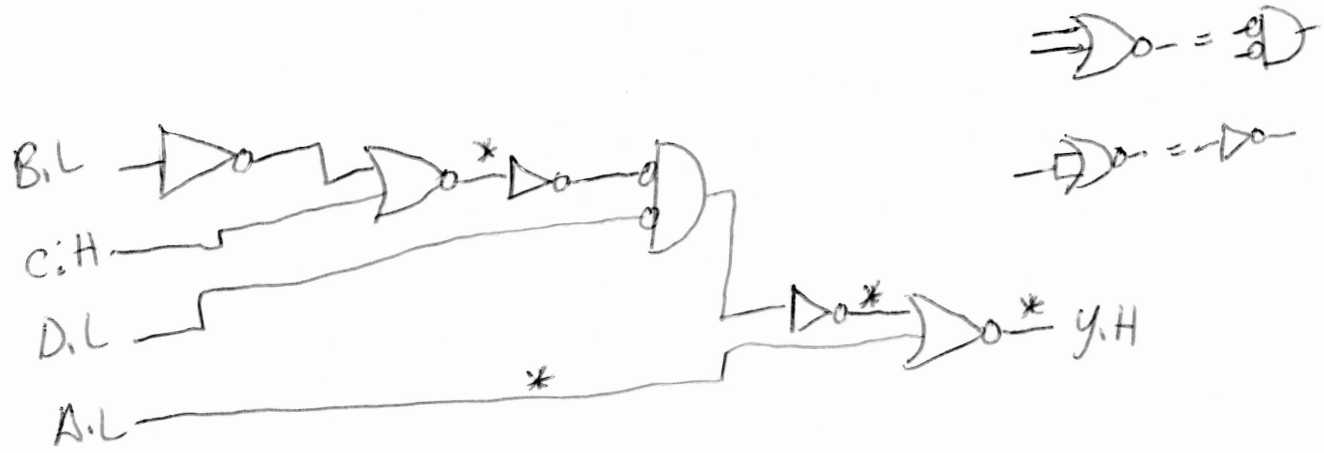
16 bits

Pg. Score =

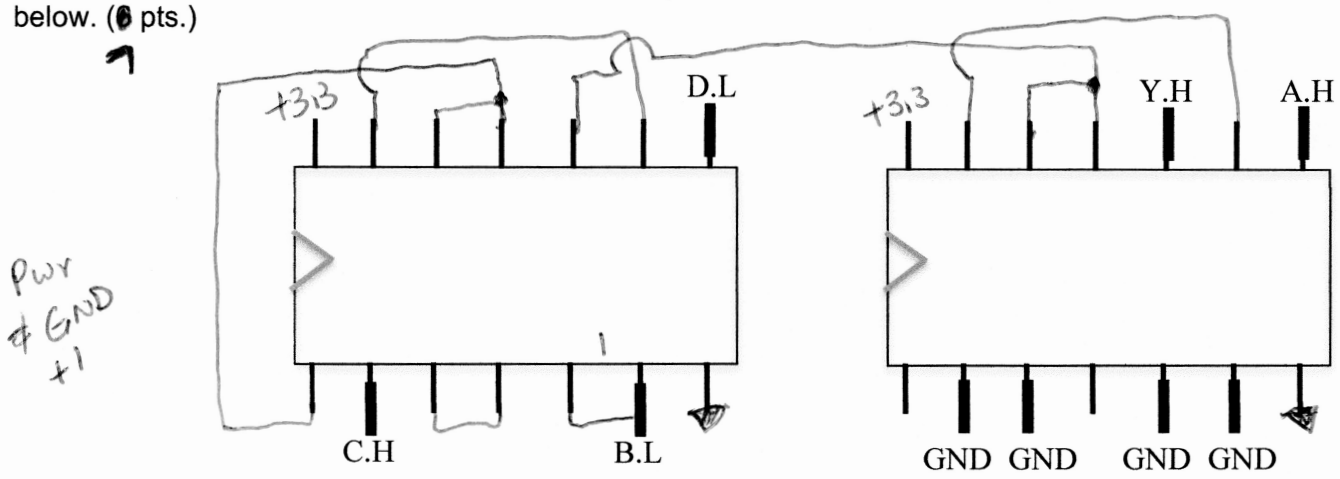
KEY

4. Directly synthesize a circuit for the following Logic Equation using only ***2 Input NOR gates***. (9 pt.)

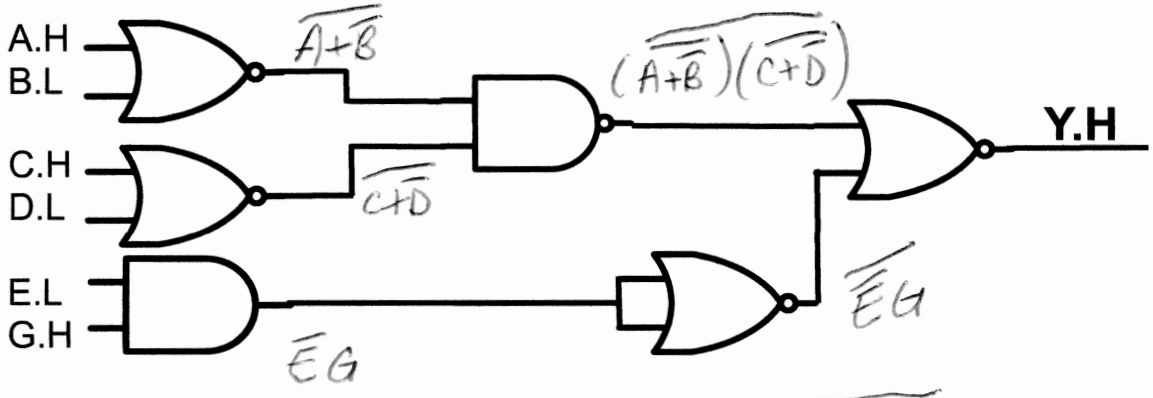
$Y = \overline{\overline{A} + ((\overline{B+C}) * D)}$; A.L, B.L, C.H, D.L, Y.H **Do Not Simplify the Equation!**



5. Show the **ALL the CONNECTIONS** below to implement the above circuit in the two 74HC02 NOR ICs below. (6 pts.)



9. Derive the logic equations for the following signals listed after the circuit below. ***Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!***



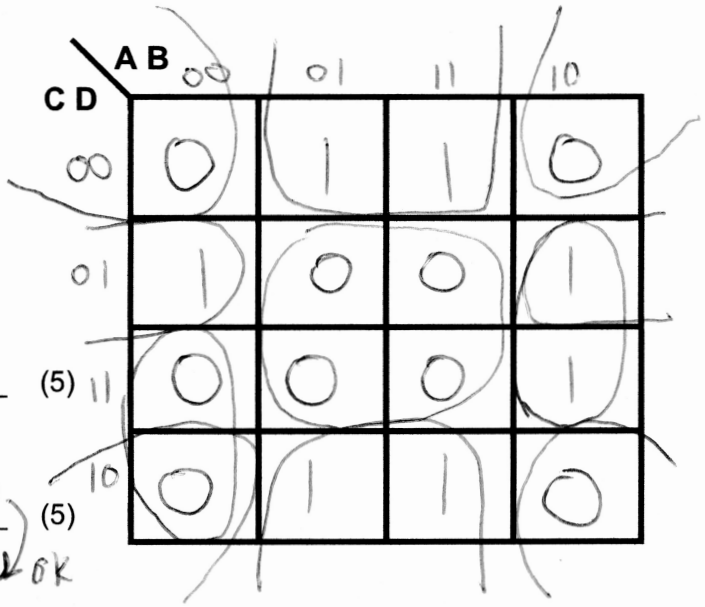
Y.H = $\overline{(\overline{A+B})(\overline{C+D})} + \overline{EG}$ (9 pt.)

Page Score =

KEY

10. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map.

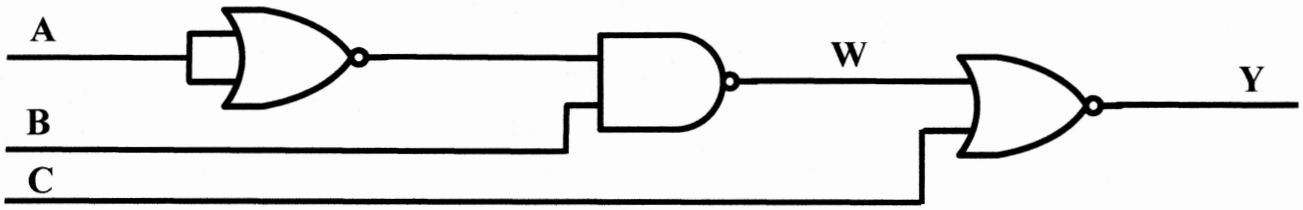
$$(B+C+D)(\overline{A}+B+\overline{C}+D)(A+\overline{C}+\overline{D})(\overline{B}+\overline{D})(A+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{D})$$

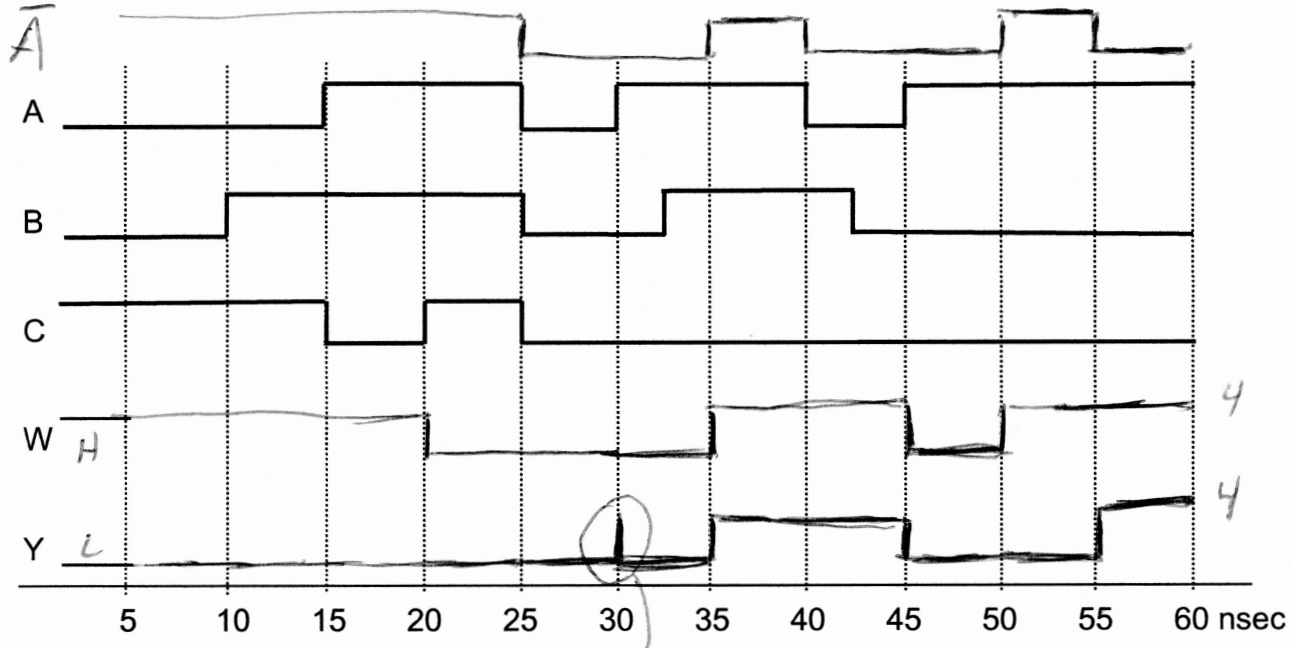


Y (MSOP) = $\bar{B}\bar{C}D + A\bar{B}D + B\bar{D}$ (5)

Y (MPOS) = $(B+D)(\bar{B}+\bar{D})(A+B+\bar{C})(A+\bar{C}+\bar{D})$ (5) OK

11. Given the circuit below complete the ***voltage timing diagram*** for signals X and Y. Assume all devices have a **10 nsec** propagation delay. (9 pt.) **Assume A = B = Y = L, C = W = H initially.**





=>| t_p 10 ns |<=

Page Score =

12. Simplify the equation below with **De Morgan's Rule** and **Boolean Identities** to find the **MSOP**. (10 pt.) KEY

$$P = \overline{(\bar{W}*X)(\bar{W}*\bar{Y}*\bar{Z})(V*W*\bar{Y}*\bar{Z})(\bar{V}*X)(\bar{V}*\bar{W})(W*\bar{Y}*\bar{Z})}$$

$\overline{(\bar{w}+\bar{x})(w+y+z)(\bar{v}+\bar{w}+y+z)(\bar{v}+\bar{x})(v+w)(\bar{w}+y+z)}$

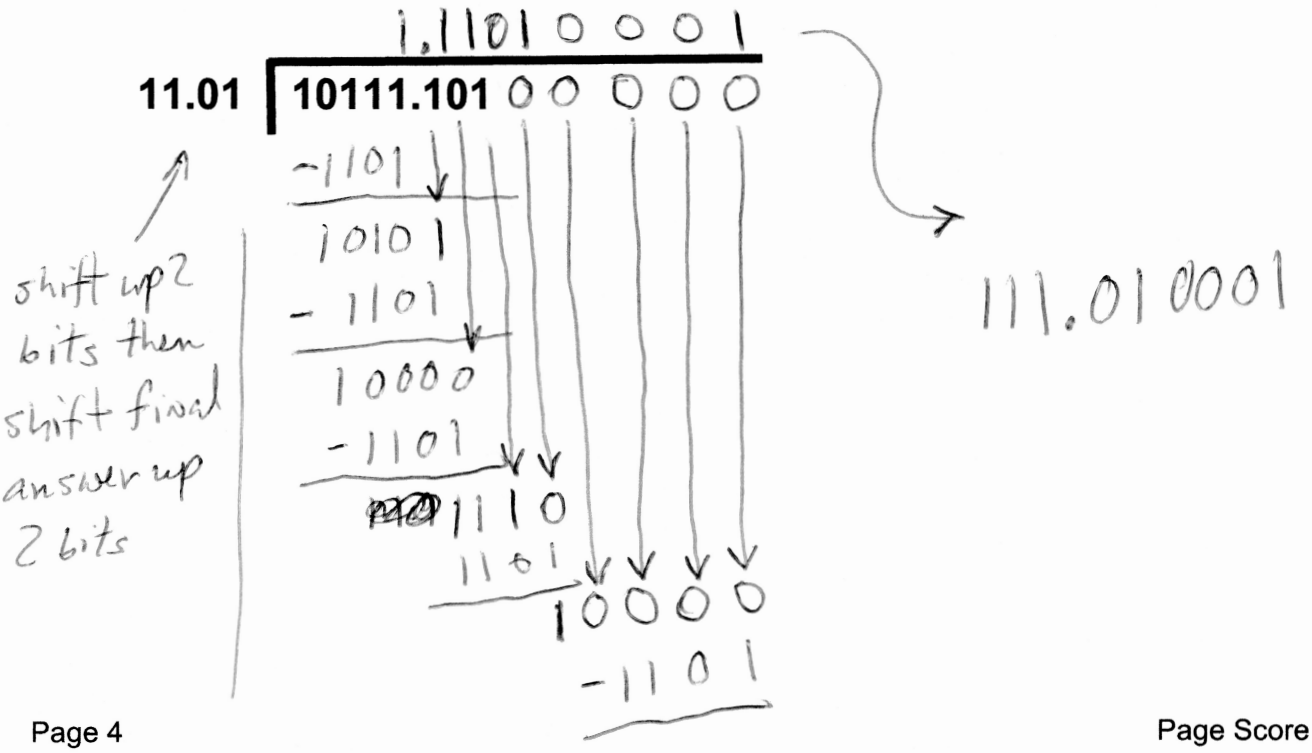
$(y+z)$

$\overline{(w+\bar{x})(y+z)(\bar{v}+\bar{x})(v+w)} = \bar{w}+\bar{x} + \bar{y}+\bar{z} + \bar{v}+\bar{x} + \bar{v}+w$

$\bar{w}x + \bar{y}\bar{z} + vx + \bar{v}\bar{w}$ → concensus to create $\bar{w}x$

Y = $\bar{y}\bar{z} + vx + \bar{v}\bar{w}$ **MSOP**

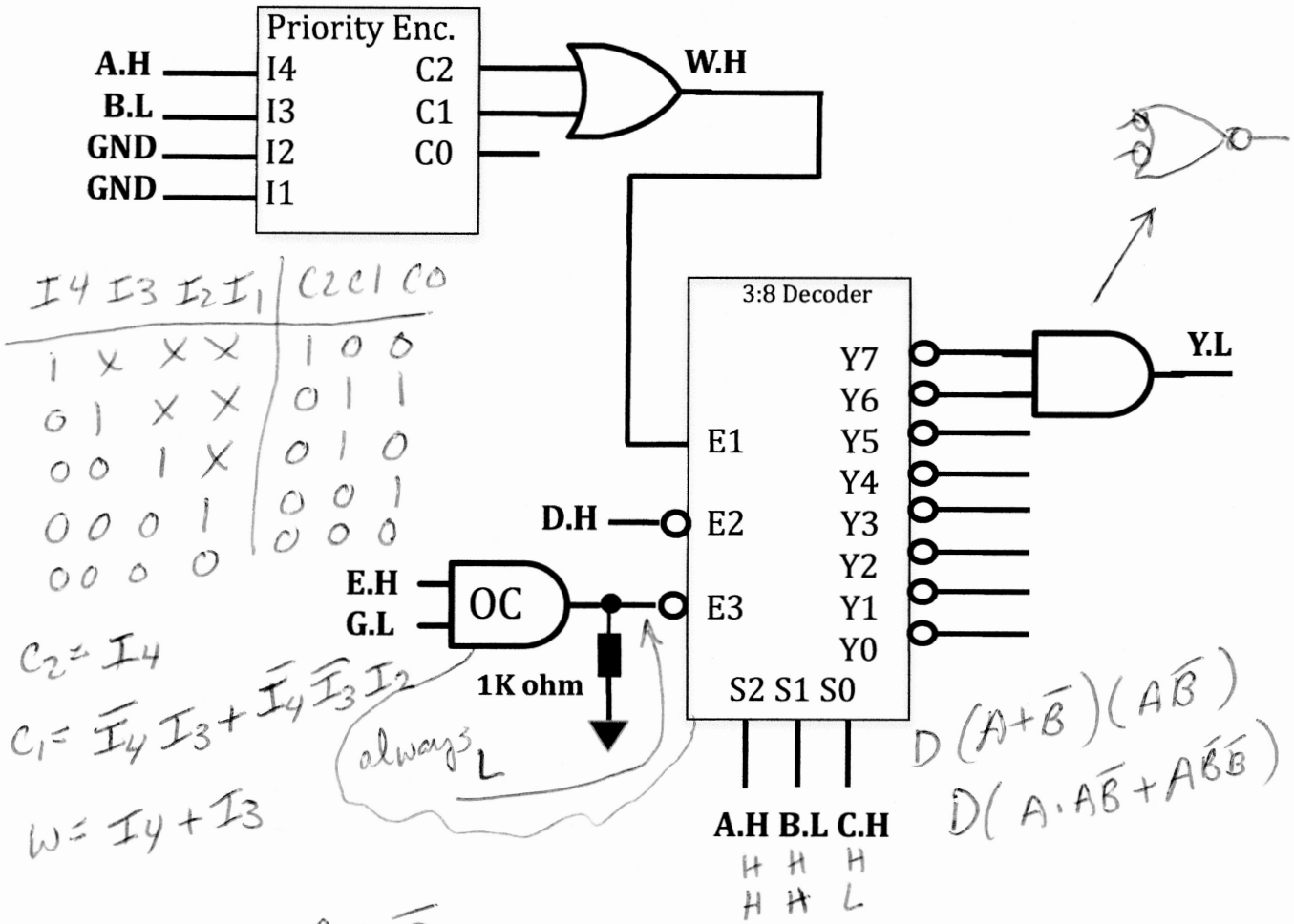
13. Lucky #%$@##! 13! Perform the following ***Unsigned Binary division*** below by hand. ***Show at least 6 fractional binary bits in your answer.*** (5 pt.)



Page Score =

KEY

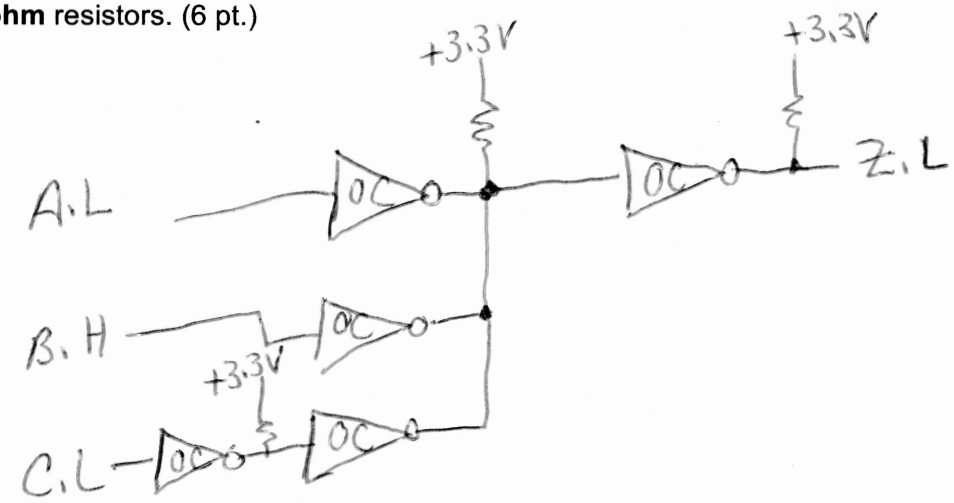
14. For the circuit below find the **MSOP for W.H and Y.L**. (10 pt.)



W.H = $A + \bar{B}$ **MSOP** (3 pt.)

Y.L = $(A+\bar{B})(D)(A\bar{B}C + A\bar{B}\bar{C}) = A\bar{B}D$ **MSOP** (7 pt.)

15. Implement the logic equation **Z = A*/B*/C** (Z.L, A.L, B.H, C.L) in hardware using **Open Collector Inverters** and **1K ohm** resistors. (6 pt.)



Page Score =

KEY

16A. Design a **Signed Multiplier** that **multiplies a 3 bit signed number by -7**. The input is therefore a 3 bit signed number and output should be the input value multiplied by a constant (-7) Assume all inputs & outputs are high true. Create a Logic Truth Table below for the device below. (9 pt.)

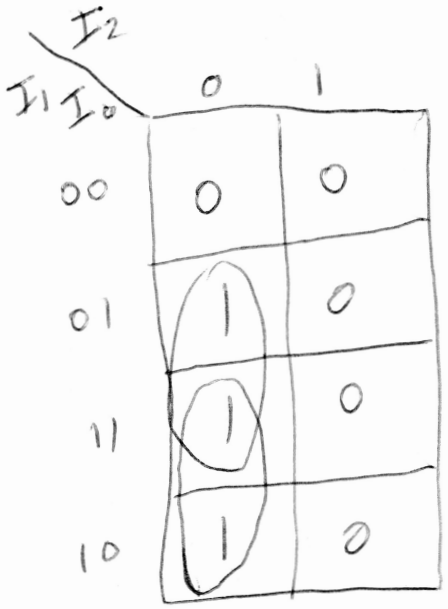
$(I_{3:0})(-7)$		I_2 I_1 I_0	y_5 y_4 y_3 y_2 y_1 y_0
0	0	0 0 0	0 0 0 0 0 0
-7	1	0 0 1	1 1 1 0 0 1
-14	2	0 1 0	1 1 0 0 1 0
-21	3	0 1 1	1 0 1 0 1 1
			0 1 1 1 0 0
28	-4	1 0 0	0 1 0 1 0 1
21	-3	1 0 1	0 0 1 1 1 0
14	-2	1 1 0	0 0 0 1 1 1
7	-1	1 1 1	

28 → 16+12 → 0 1 1100

-7	-14	-21
00 0111	00 1110	01 0101
11 1000 +1	11 0001 +1	10 1010 +1
11 1001	11 0010	10 1011

16B. Determine the MSOP logic equation for the output Most Significant Bit (MSB). (4 pt.)

y_5



$y_5 = \overline{I_2} I_0 + \overline{I_2} I_1$

Page Score =