EEL3701 – Dr. Gugel
Spring 2017
Exam #1

Last Name, First Name _____

UF ID# _____

Open book and open notes, ***90-minute*** *examination.* ***No electronic devices are permitted.***

Page 1)	9 points	Lucas	Page 2)	23 points	2 Daniel / 3 Aaron
Page 3)	18 points	4 Caleb / 5 Alan	Page 4)	17 points	6-8 Veronica / 9 Kyle
Page 5)	18 points	10) Wyatt / 11 Casey	Page 6)	15 points	12 Cody

TOTAL _____ of 100

Kevin – total points

Re-grade requests must be handed in the day exams are returned in class. *Write the problem number you wish reviewed.* ***A maximum of three review problems is allowed.*** *Do not write anywhere else on the exam other than below or you will receive a zero on the exam.*

_____

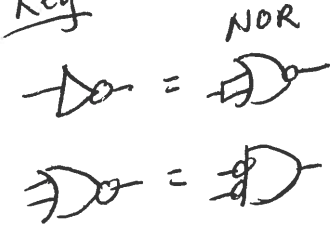
_____

_____

1. Directly synthesize a circuit for the following equation using only **2 Input NOR** gates only. (9 pt.)

$$Y = \overline{\overline{A} * (\overline{B*C}) + E + \overline{D}}$$; A.L, B.H, C.L, D.H, E.L, Y.H **Do Not Simplify the Equation!**

Key



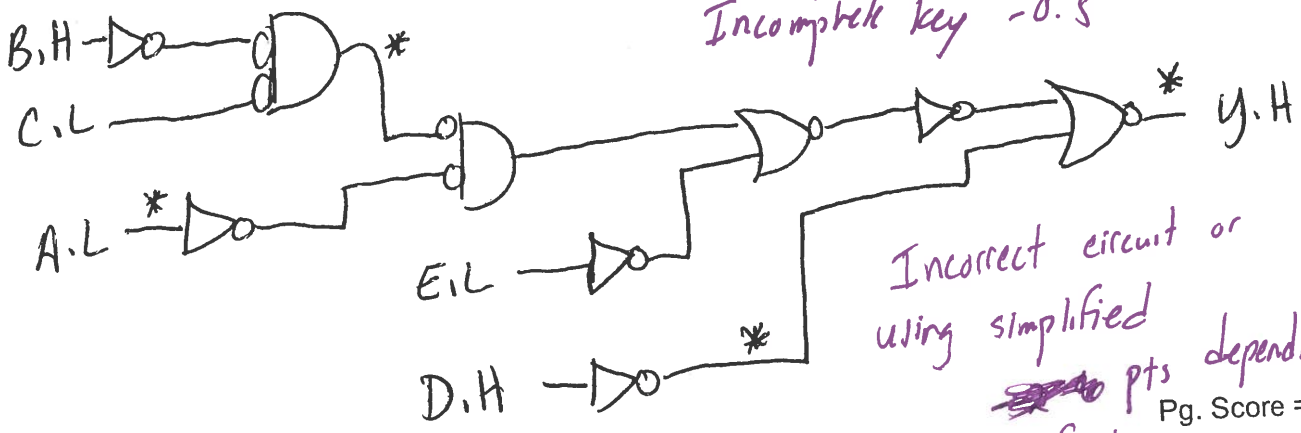
MOST OPTIMAL solution = Full credit

Each gate = 1 pt.

Any # of gates over 9 AND CORRECT -0.5 pt per gate

No key -2 pt

Incomplete key -0.5

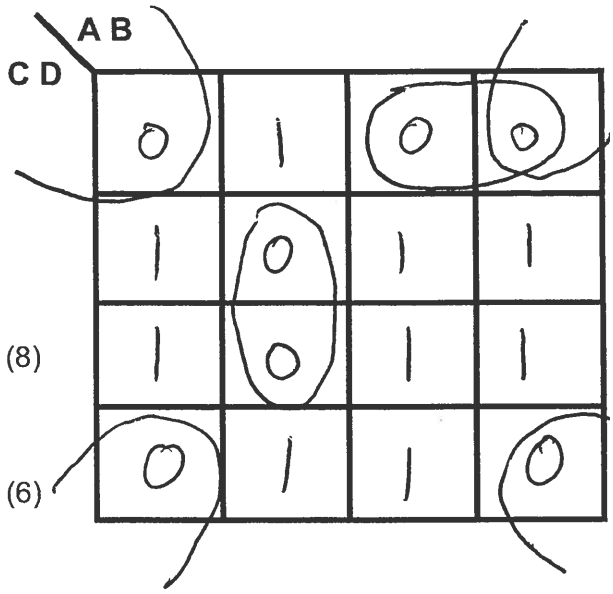


Incorrect circuit or using simplified pts depending -1-9 pts

Pg. Score =

2. Find the **minimum sum of products** and **minimum product of sums** for the logic equation below using a K-Map. (14 pt.)

$$Y = (A+B+C+D)(/A+/B+C+D)(/A+C+D)(B+/C+D)(A+/B+/D)$$



ABC or BCD

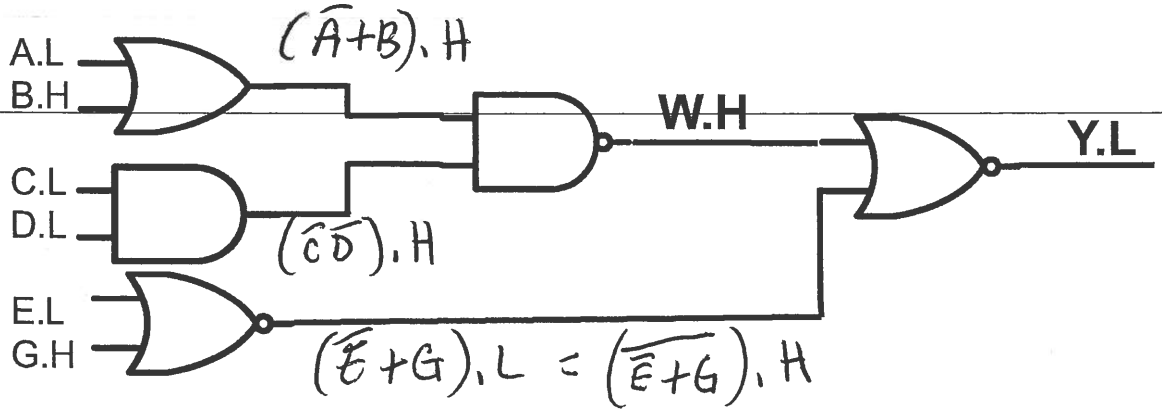
Y (MSOP) = $\bar{A}B\bar{D} + \bar{B}D + AD + \uparrow$ (8)

2 2 2 2

Y (MPOS) = $(B+D)(A+\bar{B}+\bar{D})(\bar{A}+C+D)$ (6)

2 2 2

3. Derive the logic equations for the following signals listed after the circuit below. ***Show all intermediate signals as HIGH true for partial credit purposes. DO NOT SIMPLIFY YOUR ANSWER!***



W.H = $\overline{(\bar{A}+B)(\bar{C}\bar{D})}$ (5 pt.)

1

2 2

Y.L = $\overline{(\bar{A}+B)(\bar{C}\bar{D})} + \overline{\bar{E}+G}$ (4 pt.)

1 3

Page Score =

4. Simplify the equation below with **De Morgan's Rule** and **Boolean Identities** to find the **MSOP**. (10 pt.)

$$Y = \overline{(X+Y+Z)(\bar{X}+\bar{Y}+\bar{W})(X+\bar{Z}+W)(X+\bar{Z})(\bar{X}+Z+\bar{W})(\bar{X}+Y+Z)}$$

$$\overline{x+y+z} + \overline{\bar{x}+\bar{y}+\bar{w}} + \overline{x+\bar{z}+w} + \overline{x+\bar{z}} + \overline{\bar{x}+z+\bar{w}} + \overline{\bar{x}+y+z}$$

$$\bar{x}\bar{y}\bar{z} + xyw + \bar{x}z\bar{w} + \bar{x}z + x\bar{z}w + x\bar{y}\bar{z}$$

$\bar{x}z$

$\bar{y}\bar{z}$ concensus 2

zw \ xy	00	01	11	10
00	1	0	0	1
01	1	0	1	1
11	1	1	1	0
10	1	1	0	0

$\bar{z}\bar{y}$ $\bar{x}z$ xyw

$Y = \underbrace{\bar{x}z}_{2} + \underbrace{\bar{y}\bar{z}}_{2} + \underbrace{xyw}_{2}$ **MSOP**

5. A student would like to design a **multiplier** that computes the product of a **2 bit unsigned number** times a **3 bit unsigned number**. i.e. P = M1:0 x N2:0 ;where all numbers are unsigned binary

How many bits are required for P? 5 (2 pt.) -2

Write the **Canonical Sum of Products (CSOP)** for the **most significant bit of P** based on inputs **M1:0** and **N2:0** below. (8 pt.) -2 * P4 = 1

* $3 \times 7 = 21$
* $3 \times 6 = 18$
  $3 \times 5 = 15$

$$P4 = \underset{4}{M_1 M_0 N_2 N_1 N_0} + \underset{4}{M_1 M_0 N_2 N_1 \bar{N}_0}$$

-4 if 1 term is correct

$P4 = M_1 M_0 N_2 N_1$ -1 simplified

-1/2 if not Pm or Pmss

Page Score =

6 – 8. Perform the following addition, subtraction and multiplication. (9 pt.)

$$\begin{array}{r} {\scriptstyle 1\ \ \ \ \ \ } \\ 10111 \\ 111001 \\ 101101 \\ +\ 111111 \\ \hline 10100101 \end{array}$$

3

$$\begin{array}{r} {\scriptstyle 2\ \ \ \ \ \ } \\ 01101112 \\ 100010001 \\ -\ 01111110 \\ \hline 00010011 \end{array}$$

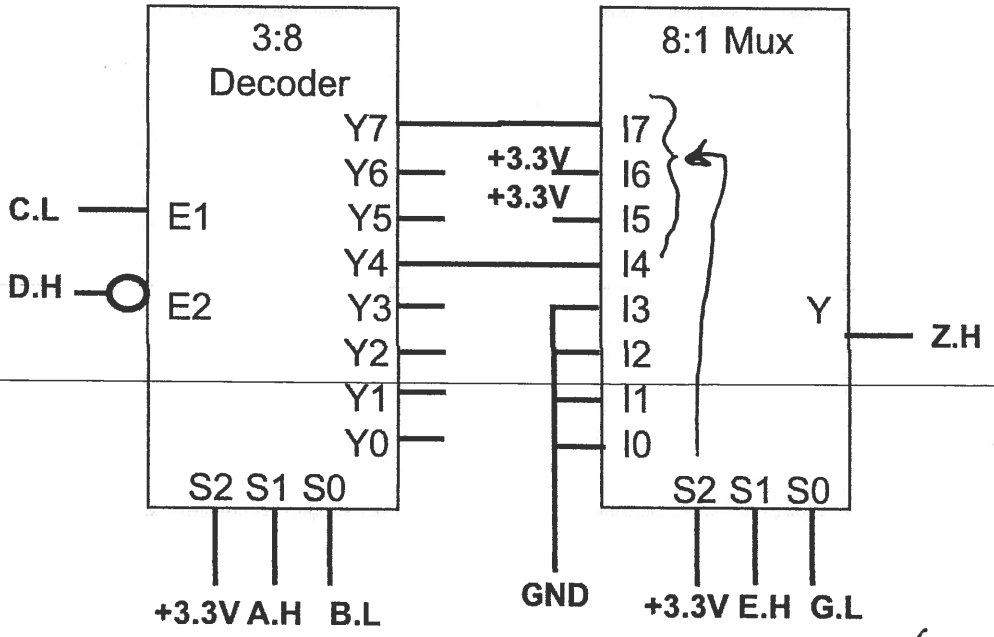
[-1 wrong carry on any] 3

$$\begin{array}{r} 10101.01 \\ \times\ 101.01 \\ \hline 10101.01 \\ 10101.00 \\ 101.0101 \\ \hline 1101111.1001 \end{array}$$

↑ -1

3

9. For the circuit below, derive the logic equation for Z.H. **Do not Simplify!** (8 pt.)



7 H H H

4 H L L

H H L 6

H L H 5

H H H 7

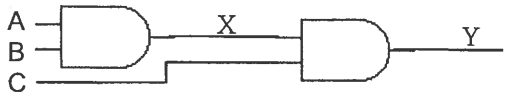
H L L 4

Z.H = $E\bar{G} + \bar{E}\bar{G} + \bar{C}\bar{D}A\bar{B}E\bar{G} + \bar{C}\bar{D}\bar{A}B\bar{E}G$

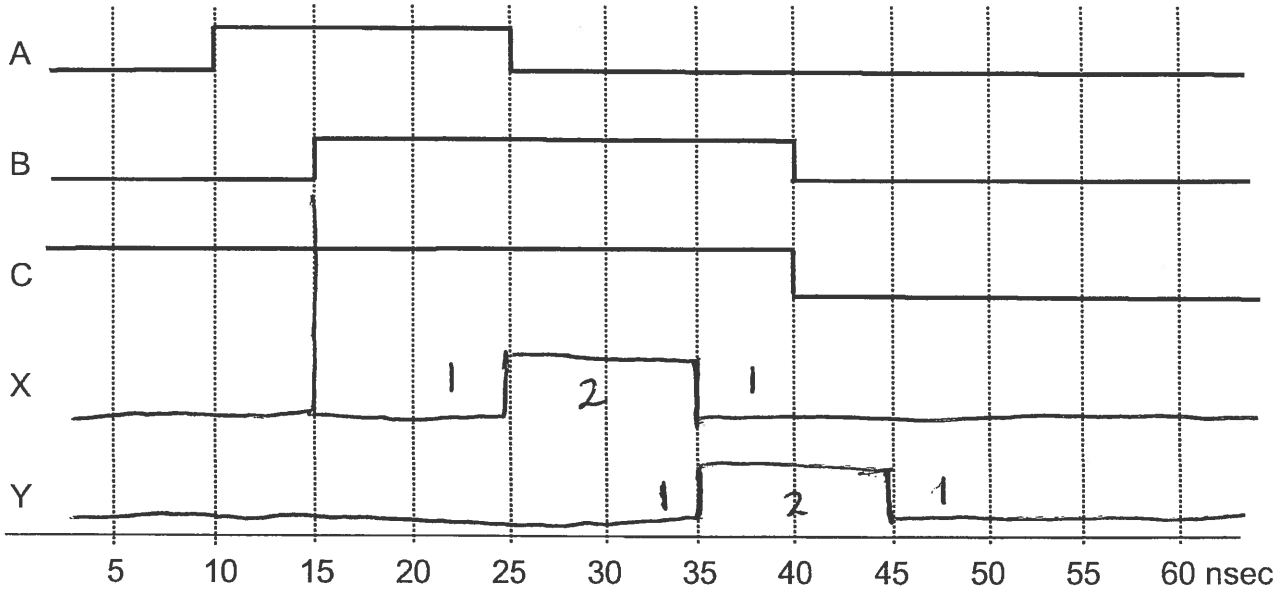
1 1 3 3

Page Score =

10. Given the circuit below complete the voltage timing diagram for signals X and Y. Assume all devices have a **10nsec** propagation delay. (8 pt.) **Assume A=L, B=L, C=H initially.**

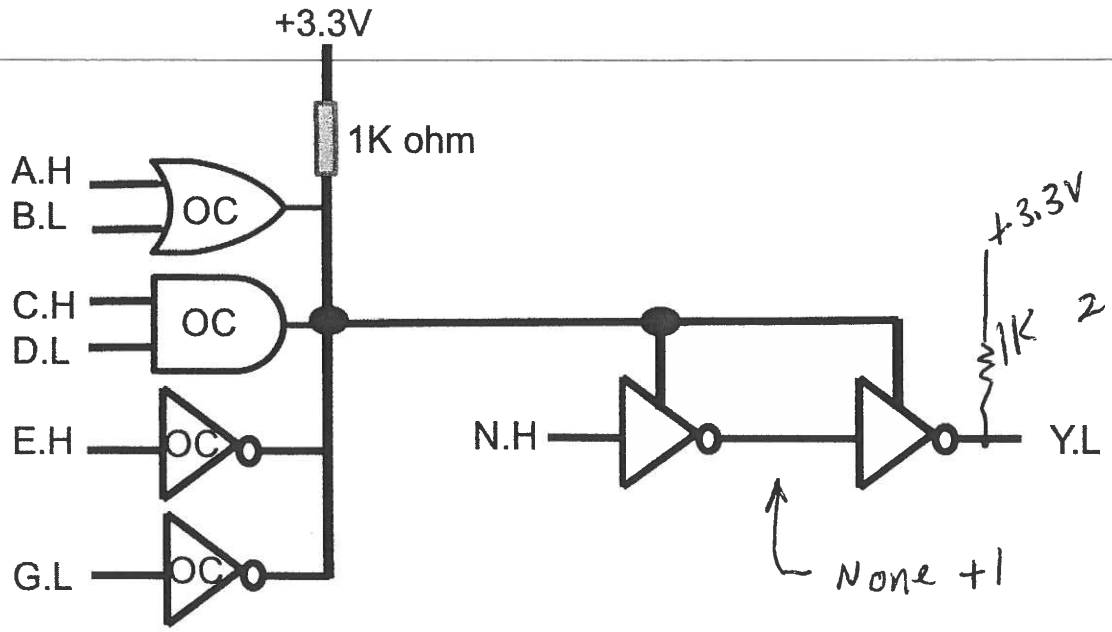


Gate Propagation Delay is 10nsec!



+1 if size of pulse is correct (out of 2)

11. For the circuit below derive the ***logic equation for Y*** and ***add the required missing Pull-up or Pull-down resistor*** to make Y a function of A,B,C,D, E, G and N. (10 pt.)



Y.L = $(A+\bar{B})(C\bar{D})(\bar{E})(G)(\bar{N})$

2 2 1 1 1

Page Score =

12. Create a device that decrements a ***4 bit Signed Number*** by 1. **N3:0** is the **signed input** and **M3:0** is the **signed output** equivalent to **N3:0 – 1**. For example, if a "3" is input to the device, the output should be "2". One additional output, V, should also be generated that indicates when an overflow occurs. For example, if decrementing an input by 1 creates an overflow condition, output V = 1, otherwise V = 0.

Draw the truth table for the device below:

N3	N2	N1	N0	M3	M2	M1	M0	V
0	0	0	0	1	1	1	1	0
1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	0	0	0
6	0	1	1	0	0	1	0	0
7	0	1	1	1	0	1	1	0
-8	1	0	0	0	X	X	X	X	1
-7	1	0	0	1	1	0	0	0	0
-6	1	0	1	0	1	0	0	1	0
-5	1	0	1	1	1	0	1	0	0
-4	1	1	0	0	1	0	1	1	0
-3	1	1	0	1	1	1	0	0	0
-2	1	1	1	0	1	1	0	1	0
-1	1	1	1	1	1	1	1	0

(10 pt.)

→ 2 for V column

2 M&N

2

2

Derive the MSOP Logic Equation for **M0** and **V** (5 pt.):

$M_0 = \overline{N_0}$

2

$V = N_3 \overline{N}_2 \overline{N}_1 \overline{N}_0$

3

Page Score = 15