EEL3701 – Dr. Gugel **Last Name**_____ **First** Key
Fall 2017 Exam II

Open book/open notes, 90-minutes. Calculators permitted. Do not write on the back side of any of the pages.

Page 1)	12 points Angela		Page 2)	22 points Casey	
Page 3)	21 points 5/6 Tomasz 7 Ben		Page 4)	17 points Matt	
Page 5)	18 points 10/Aamir 11-13/Gabe		Page 6)	10 points ~~Adam~~ Juan	
	Copy & Sean Cody/Kyle		TOTAL _____		out of 100

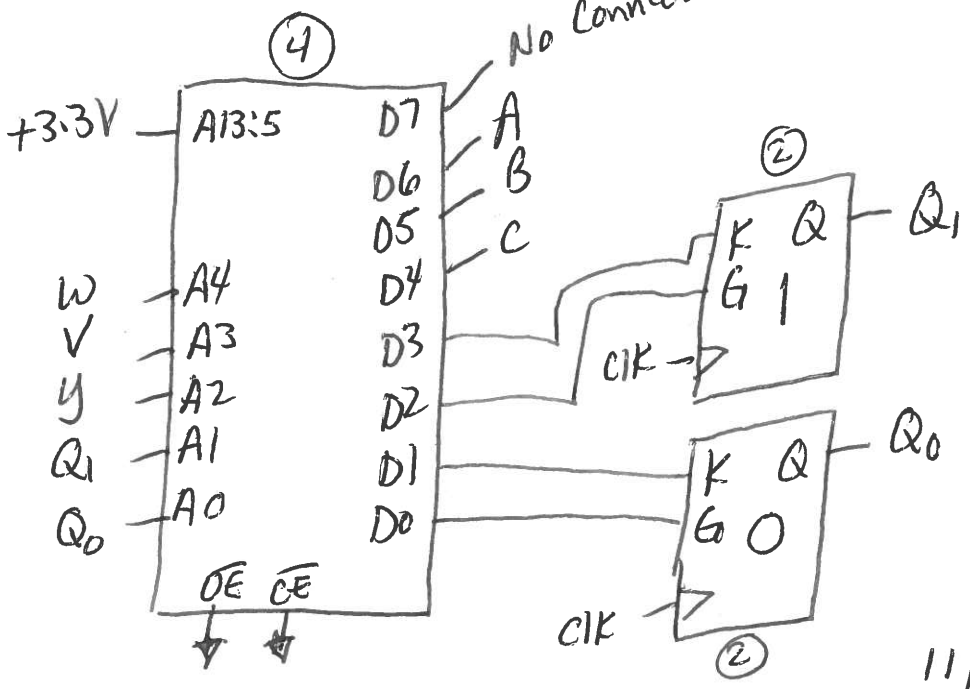
Grade Review Information: *1. Deadline of request for grade review is the day the exam is returned.* 2. Do not make any changes to problems in the test as this will be considered cheating. 3. Write only in this blocked area for a re-grade request. 4. Simply write the problem number that you would like re-graded. ***3 Maximum.***

1. _____
2. _____
3. _____

See the **ASM Flow Chart** in **Appendix A** to answer question 1-5.

1. Assuming that we will implement the ASM Flow Chart in ***Appendix A*** with a **16K x 8 ROM** and **KG** Flip-Flops (see Appendix A), draw a complete block diagram for the system below that contains the ROM, Flip-Flops and any other required hardware. **Label all signals** and assume that all **unused address lines will be tied to 3.3V**. Assume the following order of signals for most significant bit to least significant bit: W, V, Y, Q1, Q0, A, B, C, K1, G1, K0, G0 for connections to address and data lines. (8 pt.)

$16K \Rightarrow 2^4 \cdot 2^{10} = 2^{14}$
A13:0



11/1111/111x/xxxx

2. How many memory locations will need to be programmed in this design and what is the address range of these locations? Also, identify the designated part number of this device.

Number of locations programmed in memory $2^5 = 32$ (Decimal number, 1 pt.)

Range of memory to be programmed 3FE0 - 3FFF (Hex, 3 pt.)

Pg. Score =

3. Show the ***complete*** Next State Table below for the design described in problem #1. Assume the following order of signals for ***most significant*** bit to ***least significant*** bit in the Next State Table: W, V, Y, Q1, Q0, A, B, C, K1, G1, K0, G0. Use X's in the inputs and outputs when necessary to simplify the table. (14 pt.)

KG	Q^+	
00	1	set
01	Q	hold
10	$\bar{Q}$	toggle
11	0	clear

Q	Q^+	KG
0	0	X1
0	1	X0
1	0	1X
1	1	0X

Present W	V	Y	Q_1	Q_0	Next Q_1^+	Q_0^+	A	B	C	K1	G1	K0	G0	
1	X	1	0	0	0	1	0	1	0	X	1	X	0	(2)
1	X	0	0	0	1	0	0	1	1	X	0	X	1	(2)
0	1	X	0	0	1	0	0	0	1	X	0	X	1	(2)
0	0	X	0	0	0	0	1	1	0	X	1	X	1	(2)
X	X	X	0	1	0	0	1	1	1	X	1	1	X	(2)
X	X	X	1	0	0	0	0	0	1	1	X	X	1	(2)
X	X	X	1	1	X	X	X	X	X	X	X	X	X	(2)

4. Show the ROM memory contents (**Address** and **Data** in **Hex**) that needs to be programmed for the locations corresponding to **State 0**. Program **Don't Cares** (X) **in Data** as **Zeros/Low**. Note: **signal definitions** are **W.L, V.H, Y.H, A.L, B.L, C.H and the KG inputs are high true.** (8 pt.)

Room to Convert Next State Table to Voltages Below

Addr	W.L	V.H	Y.H	Q_1	Q_0	A.L	B.L	C.H	K1	G1	K0	G0
04, 0C	L	X	H	L	L	H	L	L	L	H	L	L
00, 08	L	X	L	L	L	H	L	H	L	L	L	H
18, 1C	H	H	X	L	L	H	H	H	L	L	L	H
10, 14	H	L	X	L	L	L	L	L	L	H	L	H

Addr (Hex)	Data (Hex)
04	44
0C	44
00	51
08	51
18	71
1C	71
10	05
14	05
(4)	(4)

5. For the ASM Flow Chart in Appendix A and the Next State Table in #3, assume that the design will now be implemented entirely in your CPLD. Show the simplified logic equations required for **B** and **K1**. (6 pt.)

(4) B = $w\bar{Q}_1 + \bar{V}\bar{Q}_1 + Q_0\bar{Q}_1$ MSOP

(2) K1 = 1 MSOP

W:L, V:H, Q_1:H Q_0:H

$B = w\bar{Q}_1\bar{Q}_0 + \bar{w}\bar{V}\bar{Q}_1\bar{Q}_0 + \bar{Q}_1Q_0$ (3)

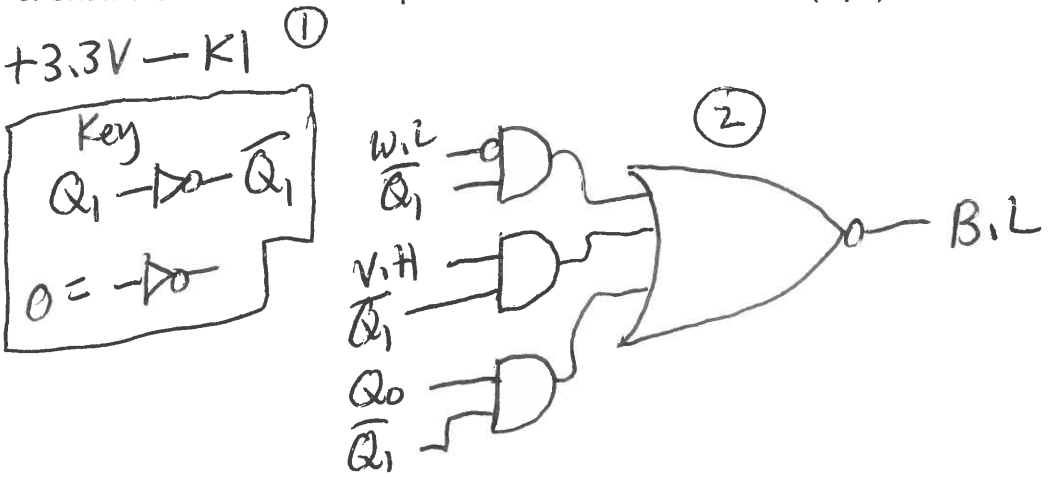
$= (w+\bar{w}\bar{V})\bar{Q}_1\bar{Q}_0 + \bar{Q}_1Q_0$

$= (w+\bar{V})\bar{Q}_1\bar{Q}_0 + \bar{Q}_1Q_0$

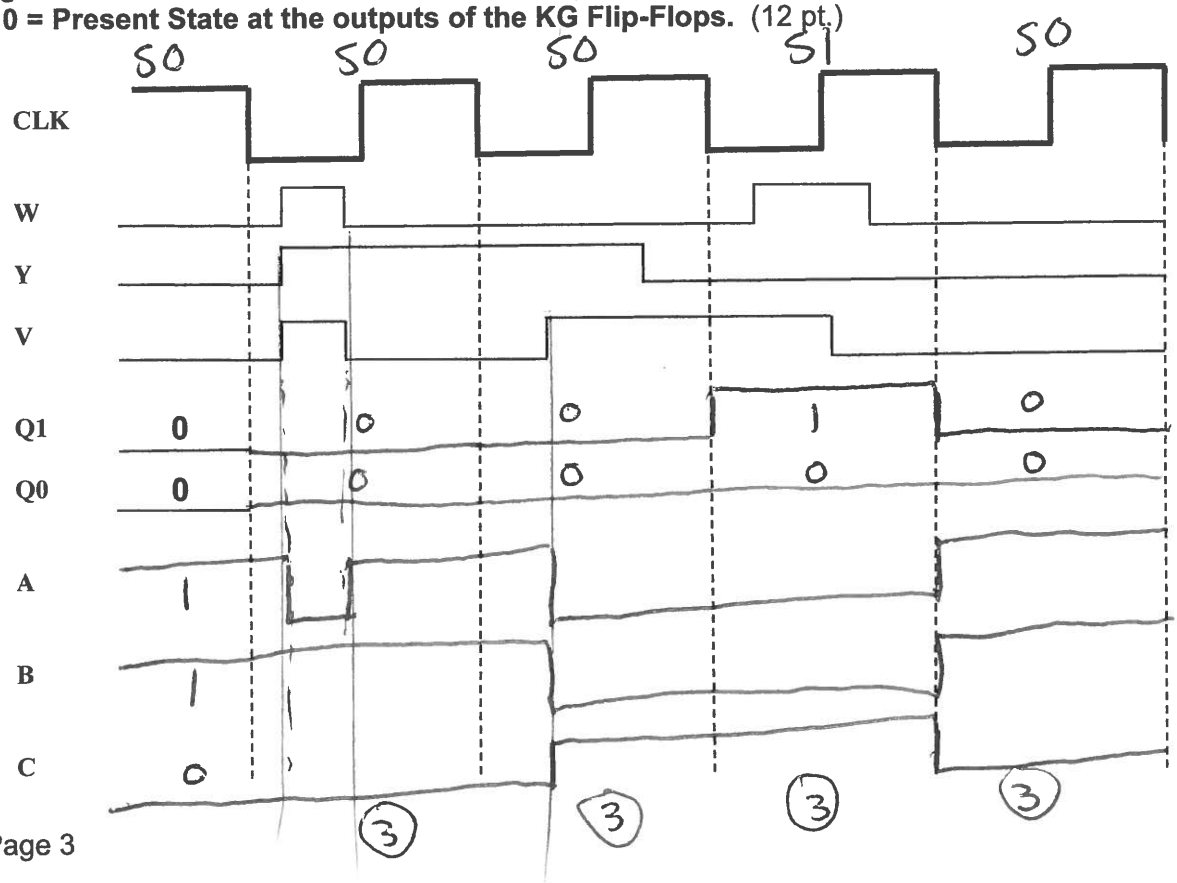
$= (w\bar{Q}_0 + \bar{V}\bar{Q}_0 + Q_0)\bar{Q}_1$

$= (w+\bar{V}+Q_0)\bar{Q}_1$ (1)

6. Show the above circuits required for **B.L** and **K1.H** below. (3 pt.)

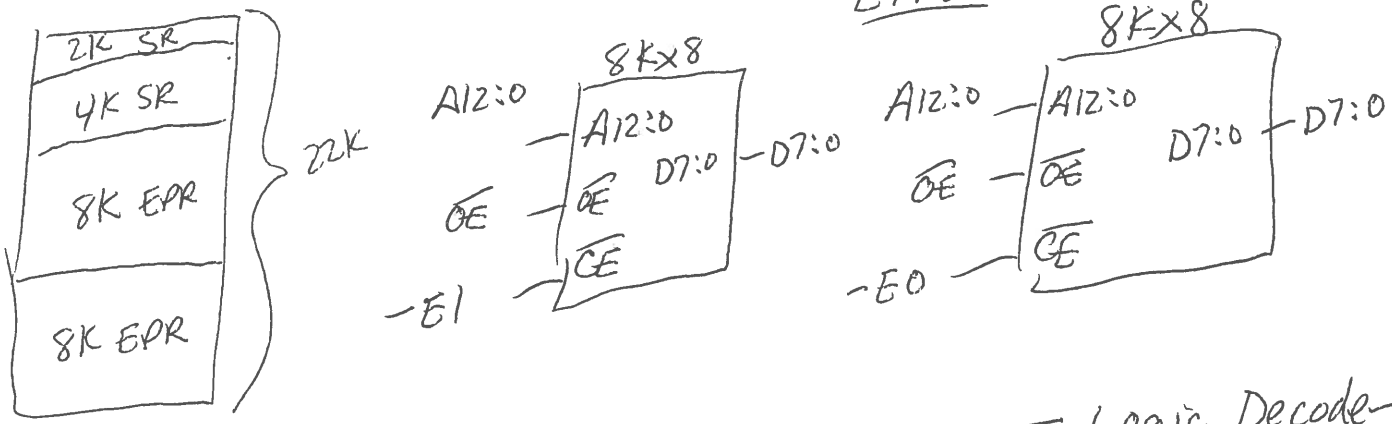


7. Assuming again that we are referencing the ASM Flow Chart in Appendix A. **Fill in** the **Logic Timing Diagram** below. Assume all devices zero propagation delay equal and the flip-flops are falling edge triggered. **Q1:0 = Present State at the outputs of the KG Flip-Flops.** (12 pt.)



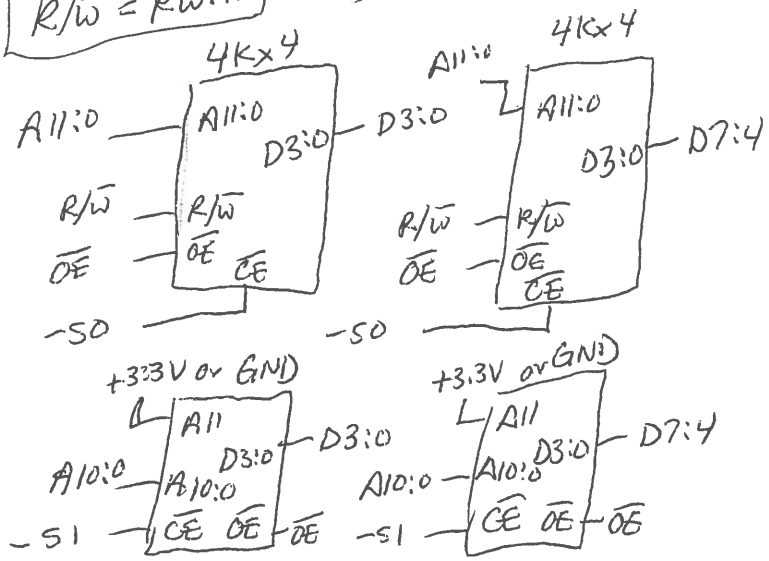
8. Design a **22K x 8 memory module** containing ***16K x 8 of EPROM*** and ***6K x 8 of SRAM***. Assume that the following devices are available: **8K x 8 EPROMs** and **4K x 4 SRAMs**. The memory module contains the usual address and data lines along with control signals **CE.L**, **RW.H** and **OE.L**. Note: The EPROM should go in the lowest 16K of the memory module. Show all device connections and ***logic decode*** equations. (12 pt.)

$22K = 16K + 4K + 2K$ $16K = 2^{14}, A13:0$ $32K = 2^{15}, A14:0$ $4K = 2^{12}, A11:0$ $8K = 2^{13}, A12:0$ $2K, A10:0$ 2^{11}



$\overline{OE} = OE.L$

$R/\overline{W} = RW.H$



Logic Decode

$-E0 = \overline{A14} \cdot \overline{A13} \cdot RW.H \cdot CE.L$

$-E1 = \overline{A14} \cdot A13 \cdot RW.H \cdot CE.L$

$-S0 = A14 \cdot \overline{A13} \cdot \overline{A12} \cdot CE.L$

$-S1 = A14 \cdot \overline{A13} \cdot A12 \cdot \overline{A11} \cdot CE.L$

9A. What are the address ranges (Hex) for the memory devices you have used in your design above? (4 pt.)

00X	XXXX	XXXX	XXXX
01X	XXXX	XXXX	XXXX
100	XXXX	XXXX	XXXX
101	XXXX	XXXX	XXXX

0 - 1FFF EPROM

2000 - 3FFF EPROM

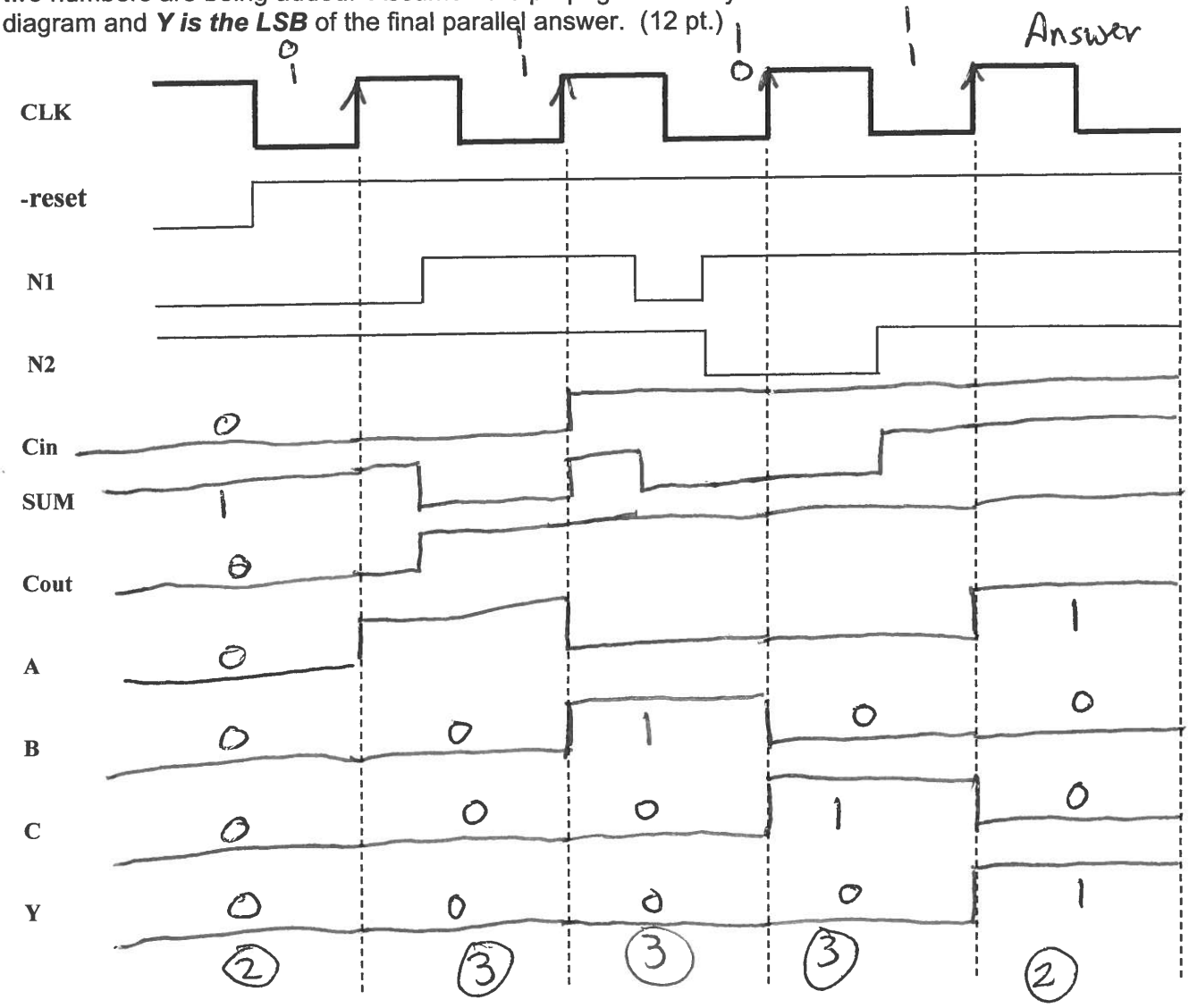
4000 - 4FFF SRAM

5000 - 57FF SRAM

highest Eprom

9B. What device is enabled when data is read from 3000 Hex? (1 pt.) _____

10. For this problem consult the circuit in Appendix B that contains the Serial Adder/Parallel Out. Assume two numbers are being serially inputted as in a Quartus simulation. Fill in all the remaining signals and identify the two numbers are being added. Assume zero propagation delays and time zero is the far left of the timing diagram and ***Y is the LSB*** of the final parallel answer. (12 pt.)



11. What two 4 bit **binary numbers** are being added above? (2 pt.) 1110 , 1011 (2)

1pt Each

N1 1110
N2 1011

$$\begin{array}{r} {\scriptstyle 1\,1\,1\,0} \\ +\,1011 \\ \hline (1)\,1001 \end{array}$$

12. What is the final computed result for ABCY **in binary** after 4 clocks? (1 pt.) 1001 (1)

13. If the two binary numbers being added are **SIGNED 4 bits**, what is the result in decimal and is it correct? (3 pt.)

-7, yes correct (2) (1)

result in decimal

Is it correct/valid?

1110 = -2

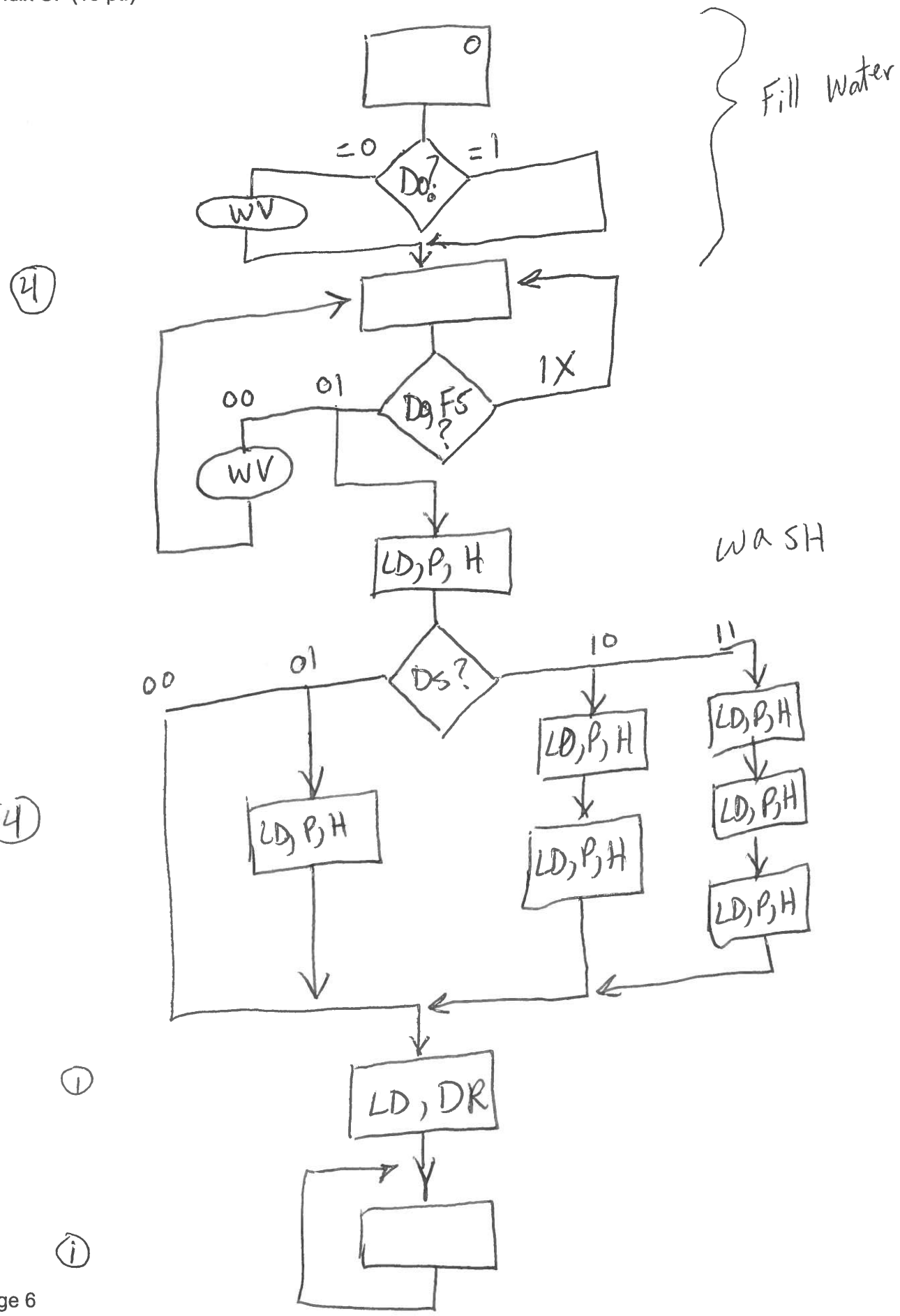
1011 = -5

Circle one. **Yes** or **No**

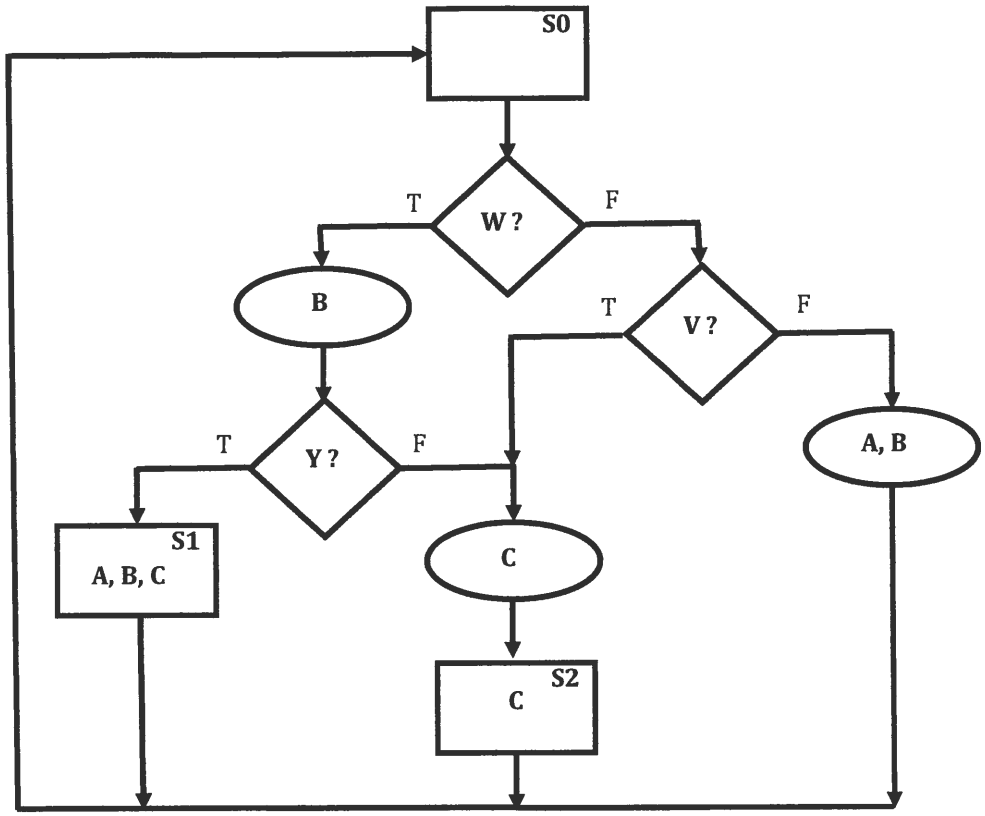
-2 + (-5) = -7

0111
1000
+1
1001

14. In the space provided below, show the ASM Flow Chart required for the Automatic Dish Washer design in Appendix C. (10 pt.)



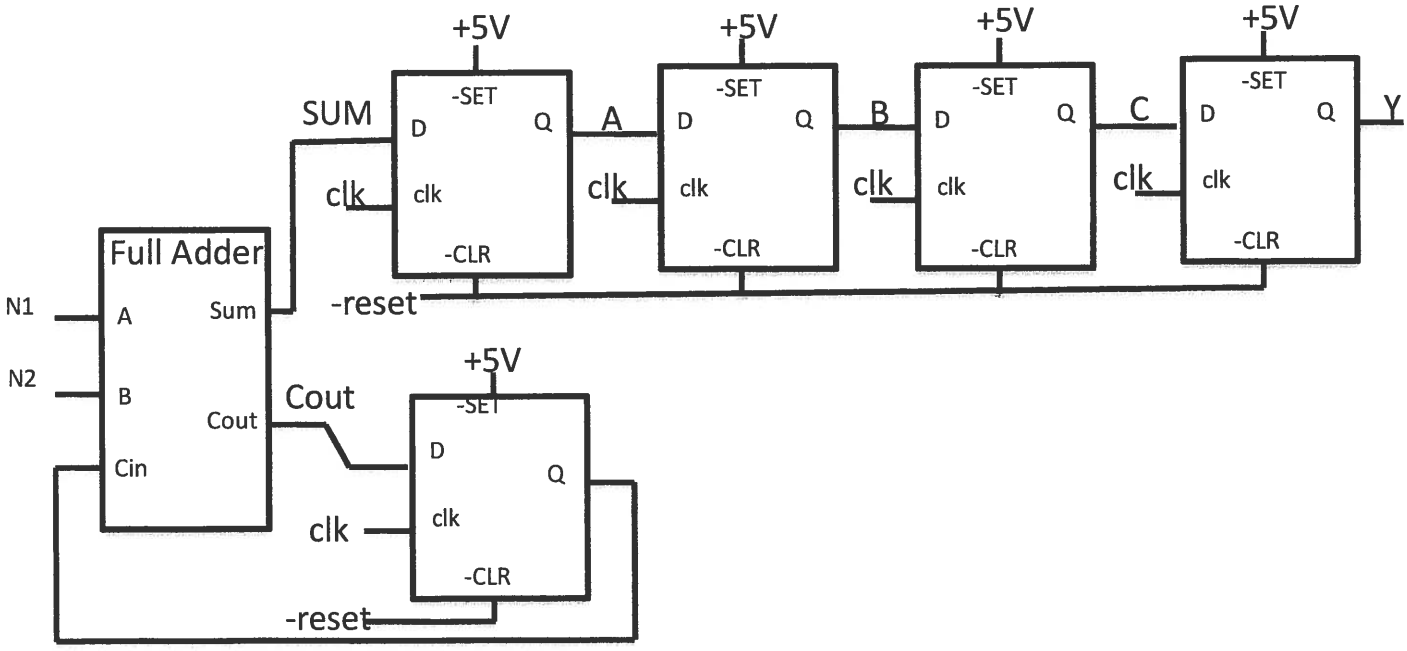
Appendix A. ASM Diagram (W.L, Y.H, V.H, A.L, B.L, C.H)



KG Flip-Flop
Next State Table

K G	Q+	
0 0	1	set
0 1	Q	hold
1 0	/Q	toggle
1 1	0	clear

Appendix B. Serial Adder with Parallel Output Conversion



Appendix C. System Description – ***Automatic Dish Washer***

Inputs:

Dirt Sensor (**DS1:0**) => two bits, 00 = ***clean***, 01 = ***slightly dirty***, 10 = ***dirty***, 11 = ***extremely dirty***

Water Full Sensor (**FS**) => one bit, If FS = 1, Water is at max limit. Else, FS = 0, Water is below the max limit and more can be added.

Door Open (**DO**) => one bit, If DO = 1 then door is open. Else, DO = 0, the door is closed.

Outputs:

Lock Door (**LD**) => one bit, If LD = 1, the main door remains locked. Else, LD = 0, door is unlocked.

Water Value (**WV**) => one bit, If WV = 1, water is turned on. Else, WV = 0, water is off.

Pump Water (**P**) => If true, pump water through the internal spray jets to wash the dishes.

Heat Water (**H**) => If true, turns on the hot water heating element for additional cleaning power.

Drain Water (**DR**) => If true, the water drain is open. Else, if false, the drain is closed.

Design Rules:

The system clock period is 5 minutes. The control process is broken into four main phases: ***fill with water***, ***wash dishes***, ***drain water*** and ***sit idle for drying***.

Fill Water Phase - Begin adding water for 5 minutes. During this time, the Dirty Sensor will calibrate and deliver a two bit indication of dish dirtiness level. i.e. 00, 01, 10, 11 as described above. The door should be unlocked for this phase, however, if the door is opened, immediately stop adding water.

When the door is closed, continue filing the water in the tank until full for as long as it takes the Water Full Sensor (FS) to become true. The door should be unlocked and again immediately shut off the water if the door is opened.

Wash Phase - Once the tank is full of water, begin the wash phase as follows. If the dishes are ***clean***, run the wash cycle for 5 minutes. If the dishes are ***slightly dirty*** run the wash cycle for 10 minutes. If the dishes are **dirty** run the wash cycle for 15 minutes. If the dishes are **extremely dirty** run the wash cycle for 20 minutes. During the wash phase lock the door, heat the water and pump it through the jets to clean the dishes.

Drain Phase - After finishing the wash phase, drain the water for 5 minutes and continue to keep the door locked.

Idle Phase – Unlock the door and sit idle forever in the last state. Assume that when it is time to wash the dishes, a start button (similar to reset) will be used to reset to the first state in the ASM flow chart.