EEL3701 – Dr. Gugel **Last Name**________________________ **First** Key

Fall 2018 Exam II

Open book/open notes. No electronic devices permitted. Do not write on the back side of any of the pages.

Page 1)	14 points #1 Ben	Page 2)	16 points #2 Mao #3 Marquez
Page 3)	22 points #4 Beichen #5 Steph #6 Daniel C.	Page 4)	18 points #7A Tom #7B Patrick
Page 5)	22 points #8 Alex P #9 Lesny #10	Page 6)	8 points #11 Danny B.
		TOTAL	________ out of 100

Grade Review Information: *1. Deadline of request for grade review is the day the exam is returned.* 2. Do not make any changes to problems in the test as this will be considered cheating. 3. Write only in this blocked area for a re-grade request. 4. Simply write the problem number that you would like re-graded. ***3 Maximum.***

1. Tomasz Scan, clip, staple Gradebook Greg
2. Daniel O., Kevin Totals
3. * Alex B gets the works on the FQ

1. For the following questions refer to **Appendix A.** In Appendix A. the flow chart is a logic flow chart with all low true input and output signals. **JK flip-flops** should be used in the state generation. Assume that the JK flip-flop ***DOES NOT*** have a reset or clear operation and therefore at power up, if an unused state is accidentally entered, the un-used state should be forced to go to State 0 in the next cycle. Show ***the next state table below where the state variables (present state and JK flip-flop inputs) are placed in the most significant bit positions. All remaining variables should then be written in alphabetical order.*** i.e. A (most significant bit), B, C (least significant bit), etc. (14 pt.)

JK	Q^+
00	Q
01	0
10	1
11	/Q

	Q_1 Q_0	v w y	Q_1^+ Q_0^+	J_1K_1	J_0K_0	A B C
2	0 0	X 0 0	0 0	0X	0X	0 0 0
2	0 0	X 0 1	0 1	0X	1X	0 1 0
2	0 0	X 1 X	1 1	1X	1X	0 0 1
2	0 1	X X X	1 0	1X	X1	1 0 0
2	1 0	X X X	0 0	X1	0X	0 0 1
2	1 1	0 X X	0 0	X1	X1	1 1 0
2	1 1	1 X X	0 0	X1	X1	0 0 0

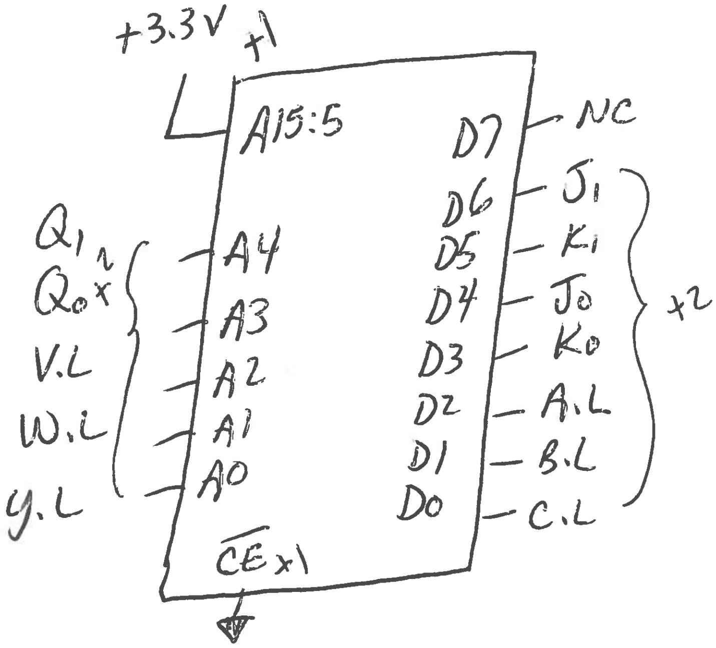
 Pg. Score =

Key

2. Assuming that we will implement the ASM Flow Chart in ***Appendix A*** in a **64K x 8 ROM** and **JK** Flip-Flops, draw a complete functional block diagram for the system below. **Label all signals** and assume that all **unused address lines will be tied high**. Note: All ***state variables (present state and JK flip-flop inputs) should be in the most significant bit positions. All remaining variables should then be written in alphabetical order.*** i.e. A (most significant bit), B, C (least significant bit). (6 pt.)

$64K = 2^6 \cdot 2^{10} = 2^{16}$

A15:0



1111/1111/111x/xxxx

F F E0 - FFFF

3. Show the 64K x 8 ROM memory contents (**Address** and **Data** in **Hex**) that needs to be programmed for the memory locations corresponding to **States 0**. Also, program **JK Don't Cares** (X) **in Data** as **Zeros/Low**. (10 pt.)

Room to Convert Next State Table to Voltages Below

Addr	Q_1	Q_0	V	W	y	J_1K_1	J_0K_0	A	B	C	Data
3,7	L	L	X	H	H	L X	L X	H	H	H	07
2,6	L	L	X	H	L	L X	H X	H	L	H	15
0,1,4,5	L	L	X	L	X	H X	H X	H	H	L	56

V	y
L	L
L	H
H	L
H	H

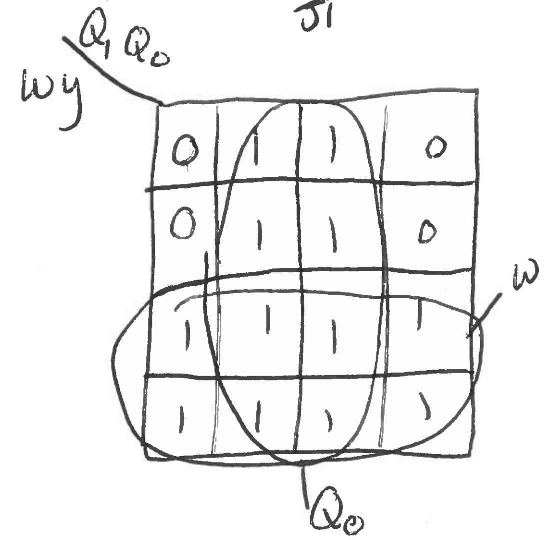
Addr (Hex)	Data (Hex)
FFE0	56 +1
FFE1	56 +1
FFE2	15 +1
FFE3	07 +1
FFE4	56 +1
FFE5	56 +1
FFE6	15 +1
FFE7	07 +1

+2 Addr

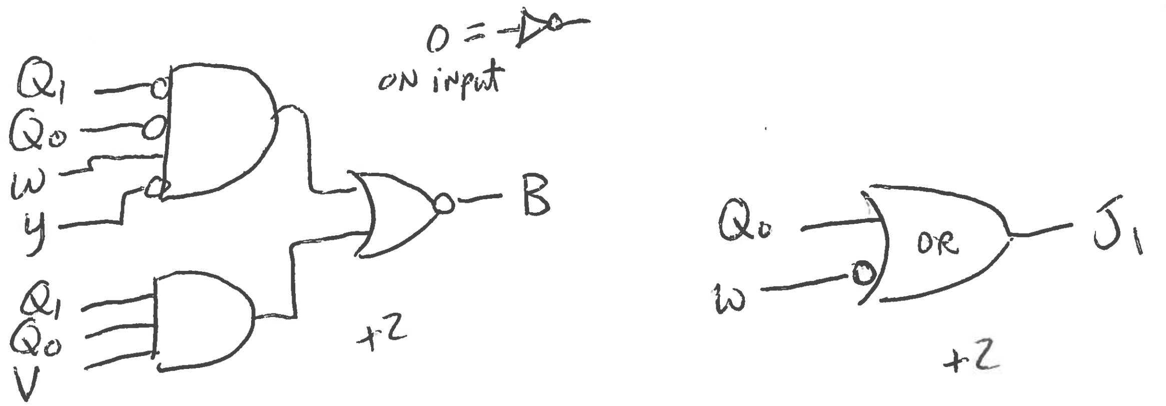
4. For the ASM Flow Chart in Appendix A and the Next State Table in #1, assume that ***the design will now be implemented entirely in your CPLD***. Show the simplified logic equations required for **B** and **J1**. (6 pt.)

B = $\overline{Q_1}\,\overline{Q_0}\,\overline{w}\,y + Q_1 Q_0 \overline{V}$ MSOP

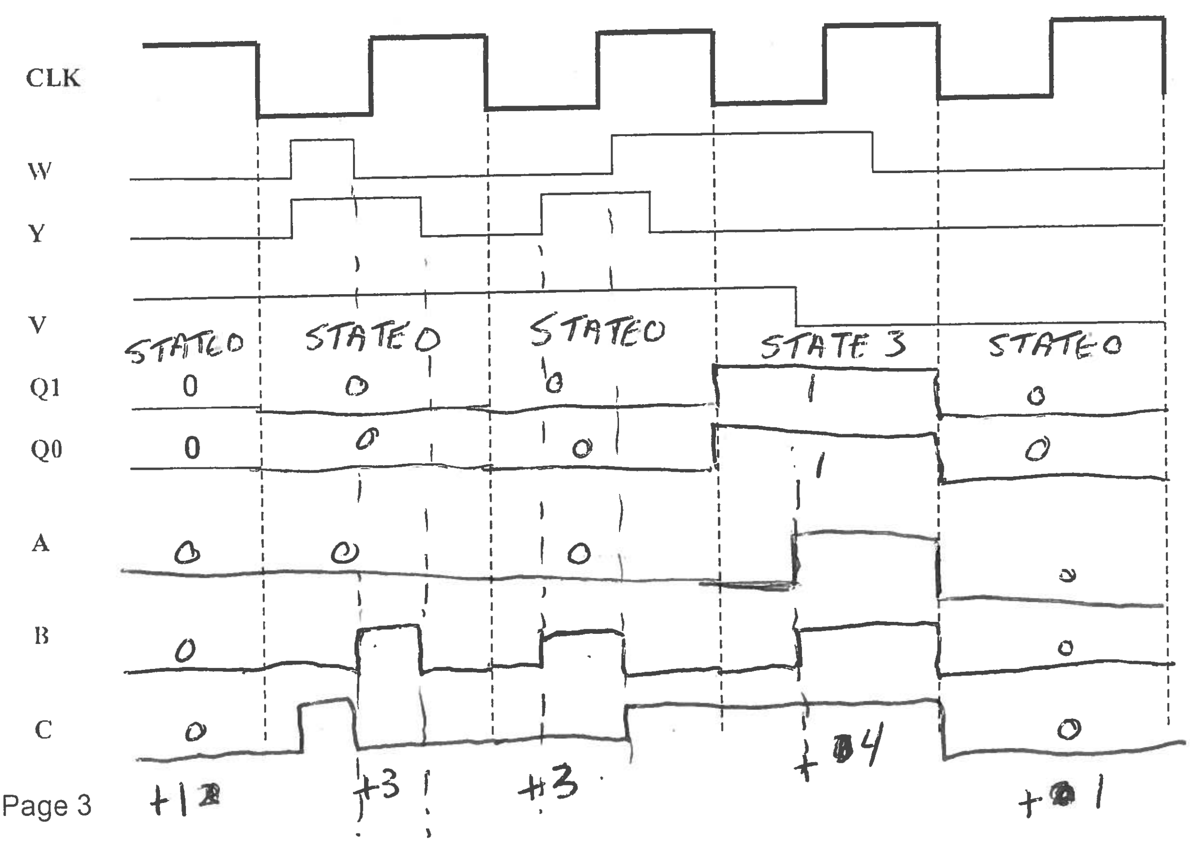
J1 = $Q_0 + w$ MSOP



5. Show the above circuits required for **B.L** and **J1.H** below. (4 pt.)

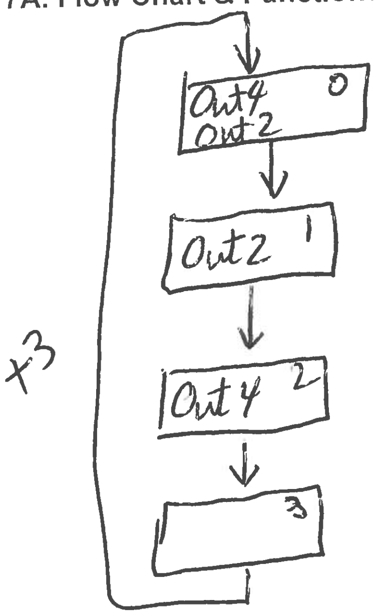


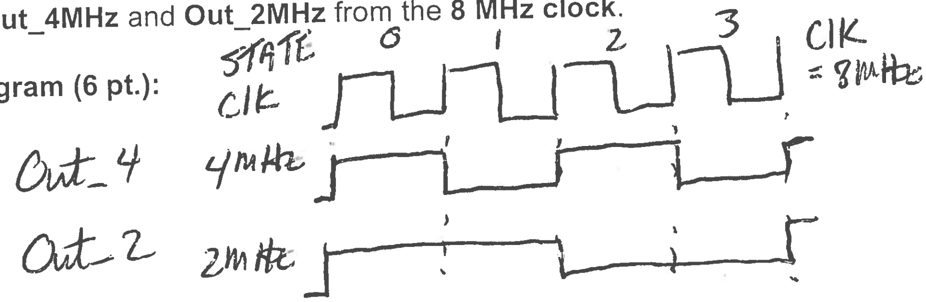
6. Assuming again that we are referencing the ASM Flow Chart in Appendix A. **Fill in** the **Logic Timing Diagram** below. Assume all devices zero propagation delay equal and the flip-flops are falling edge triggered. **Q1:0 = Present State at the outputs of the JK Flip-Flops.** (12 pt.)

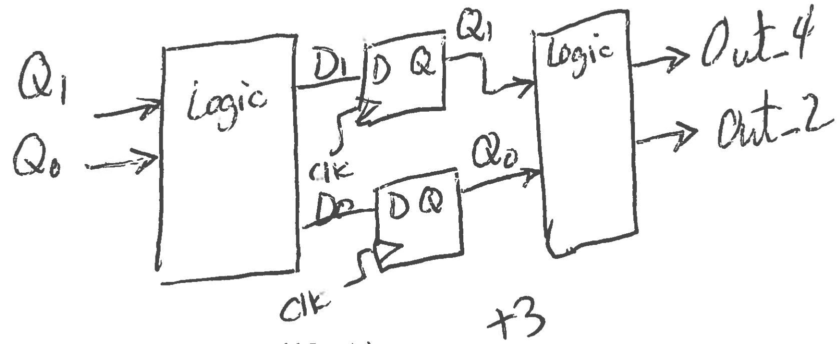


7. A student has found an 8 MHz clock chip but requires 4 MHz and 2 MHz in their design. Using your vast array of devices learned to date in this class, create a ***flow chart***, ***functional block diagram***, ***next state table*** and ***logic equations*** required to create **Out_4MHz** and **Out_2MHz** from the **8 MHz clock**.

7A. Flow Chart & Functional Block Diagram (6 pt.):







7B. Next State Table and Required MSOP Logic Equations (12 pt.):

	Q_1	Q_0	Q_1^+ (D_1)	Q_0^+ (D_0)	Out_4	Out_2
+2	0	0	0	1	1	1
+2	0	1	1	0	0	1
+2	1	0	1	1	1	0
+2	1	1	0	0	0	0

+1 $D_1 = Q_1 \oplus Q_0$

+1 $D_0 = \overline{Q_0}$

+1 Out_4MHz $= \overline{Q_0}$ [$= Q_0$]

Out_2MHz $= \overline{Q_1}$ [$= Q_1$]

+1 also acceptable

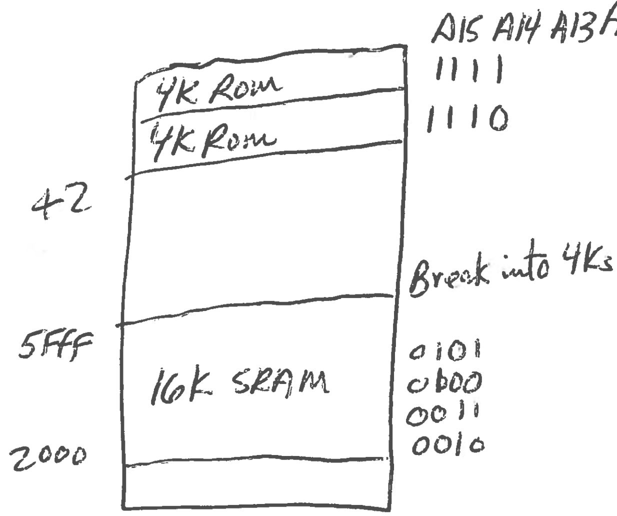
8. You are given a microprocessor with a **16 bit address bus** and **8 bit data bus**. The control bus consists of a **RW.H** signal and a low true data strobe (**DS.L**). Upon reset, the processor begins fetching the ***address of the first instruction*** from the ***highest two addresses in the system memory map***. You are given any number of **4K x 8 ROMs** and **16K x 4 SRAMs**. Place **8K of ROM** in the system and **16K of SRAM** starting at 2000 Hex in the system memory map. Show the required Rom & Ram memory devices below. Label all signals and use bus nomenclature where appropriate. (12 pt.)

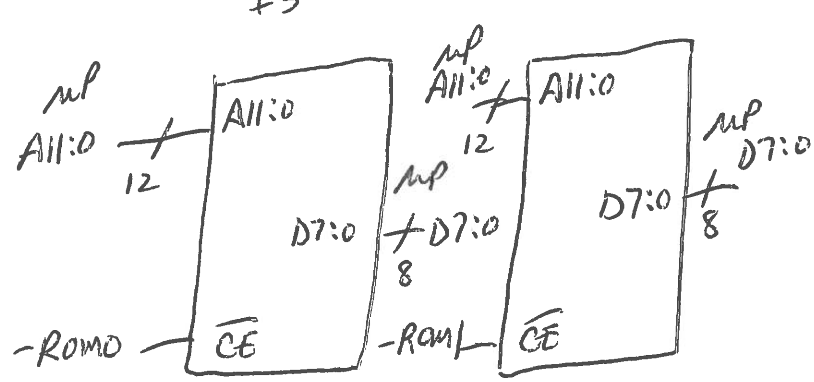
have 4Kx8 Roms ⇒ Need 8Kx8 Rom

16Kx4 SRAMs ⇒ 16Kx8 SRAM

$2^6 \cdot 2^{10} = 2^{16}$ A15:0

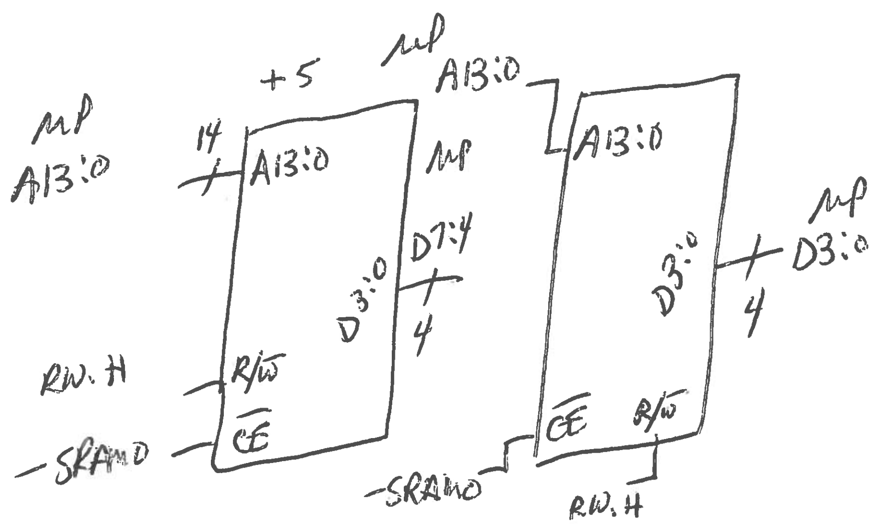
64K





$4K = 2^2 \cdot 2^{10} = 2^{12}$ A11:0

$16K = 2^{14}$ A13:0



9. What are the **address decode equations** and **address ranges** for each device above? (9 pt.)

x3 $-ROM0 = A15 \cdot A14 \cdot A13 \cdot \overline{A12} \cdot DS.L \cdot RW.H$ E000 – EFFF

x3 $-ROM1 = A15 \cdot A14 \cdot A13 \cdot A12 \cdot DS.L \cdot RW.H$ F000 – FFFF

x3 $-SRAM0 = (\overline{A15} \cdot \overline{A14} \cdot A13 + \overline{A15} \cdot A14 \cdot \overline{A13}) \cdot DS.L$ 2000 – 5FFF

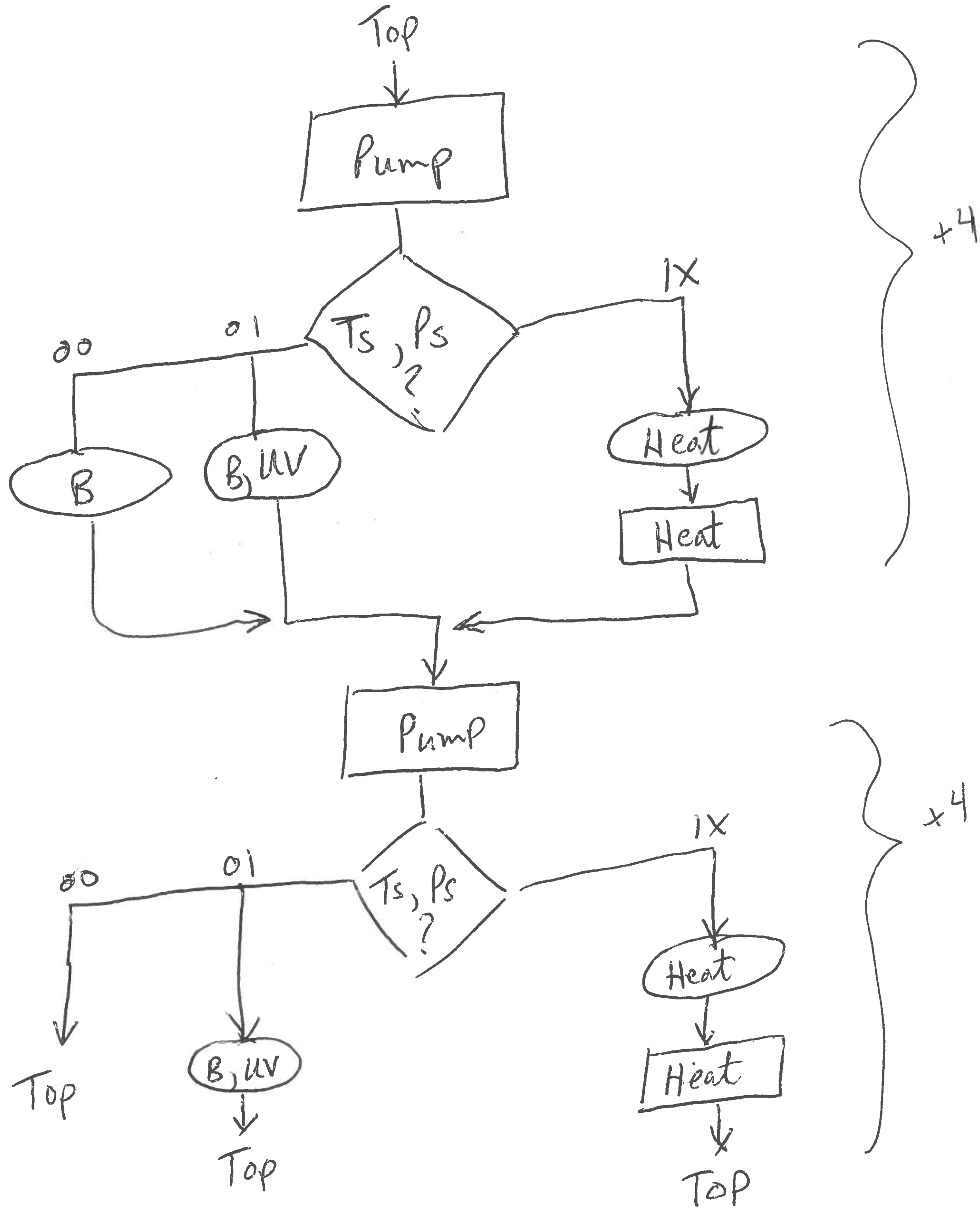
10. What values should be programmed at addresses FFFF and FFFE? (1 pt.) E0, 00

Lowest address of Rom

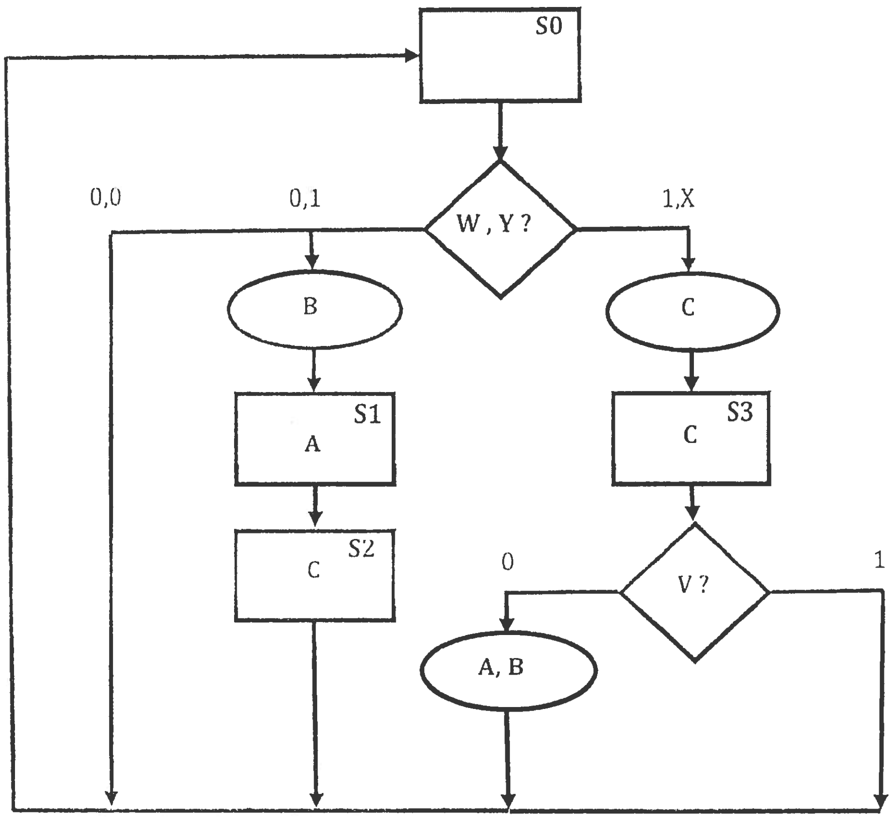
11. In the space provided below, show the ASM Flow Chart required for the Automatic Fish Tank Controller design in **Appendix B**. (8 pt.) The highest points will be awarded for the best design and vice-versa.

Outputs: Heat, Pump, Bubbler, UV-Light

Inputs: Temp Sensor, Photo Sensor



Appendix A. ASM Flow Chart (**V.L, W.L, Y.L, A.L, B.L, C.L**) implement with **JK Flip-Flops!**



Appendix B. System Description – ***Automatic Fish Tank Controller***

We would like to design a flow chart for a **fish tank controller**. Here are the specifications:

Outputs: **Heat** = on/true heats up the water. **Bubbler** = on/true, injects bubbles into the water. **Pump** = on/true, pumps the water through a filter. **UV_Light** = on/true, turns on a bacteria killing UV light.

Inputs: **TempSensor** goes true when ***the temperature in the tank falls below the desired set-point***. i.e. The water is too cold!

PhotoSensor goes true when the water is murky due to excessive bacteria & dirt in the water.

1. The ***period of the clock is three minutes***.

2. The Pump should always be pumping water through the filter at any time.

3. The Bubbler should be on for half of the time of pump operation when the temperature is above set-point for extended periods of time. The Bubbler should also be immediately turned on when murky bad water is detected. At any time, if the temperature falls below set-point, the Bubbler should be immediately shut off.

4. The Heater should immediately go on when the water temperature is below the desired set-point and should stay on for at least three minutes. During this 3 min heat interval, PhotoSensor does not need to be checked.

5. The UV_Light should only go on if both the temperature is above set-point and the PhotoSensor detects murky water. If the PhotoSensor detects clear water or the temperature falls below set-point, UV Light should be immediately shut off.