EEL3701 – Dr. Gugel Last Name_____ First Name _____
Spring 2015
Final Quiz UF ID#_____

Open book/open notes, **90-minute** exam to be done in **non-red** pen. ***No electronic devices permitted.***

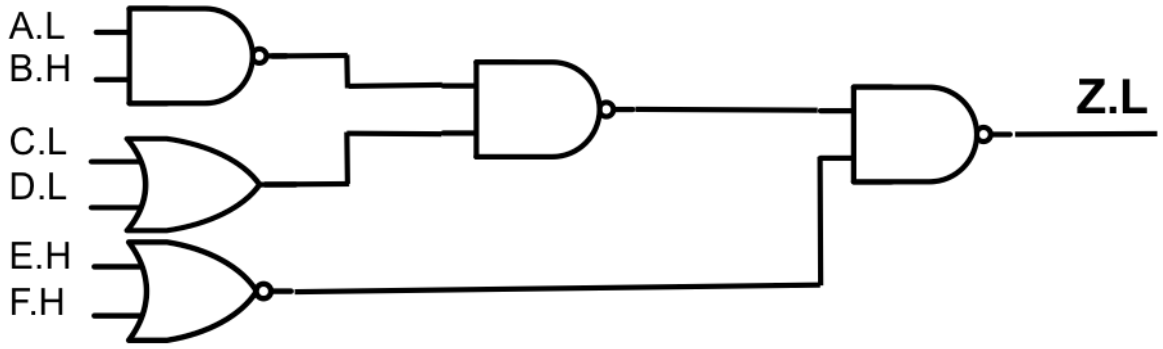
Point System: Page 1 => 10 points _____ Page 2 => 14 points _____

Page 3 => 14 points _____ Page 4 => 12 points_____

TOTAL => _____ (50 pt.)

Grade Review Information: (*NOTE: deadline of request for grade review is the day the exam is returned*.)
_____
_____
_____

1. For the circuit below, derive Z.L. **Do not simplify.** Write all intermediate terms as high true. (5 pt.)



Z.L = _____

2. Implement the logic equation below using 2 Input NOR Gates only. (5 pt.)

$$Y = (\overline{A}*B) + C + (\overline{D*E}) \quad ; \text{A.H, B.L, C.H, D.L, E.H, Y.H}$$

Pg. Score =

3. A student has interfaced a ***8K x 8 ROM*** with the G-CPU ***starting at address zero***. The student also has interfaced an ***16K x 8 RAM that begins immediately after the ROM in the G-CPU memory map***. What is the memory range and logic equation for the RAM device? (4 pt.)

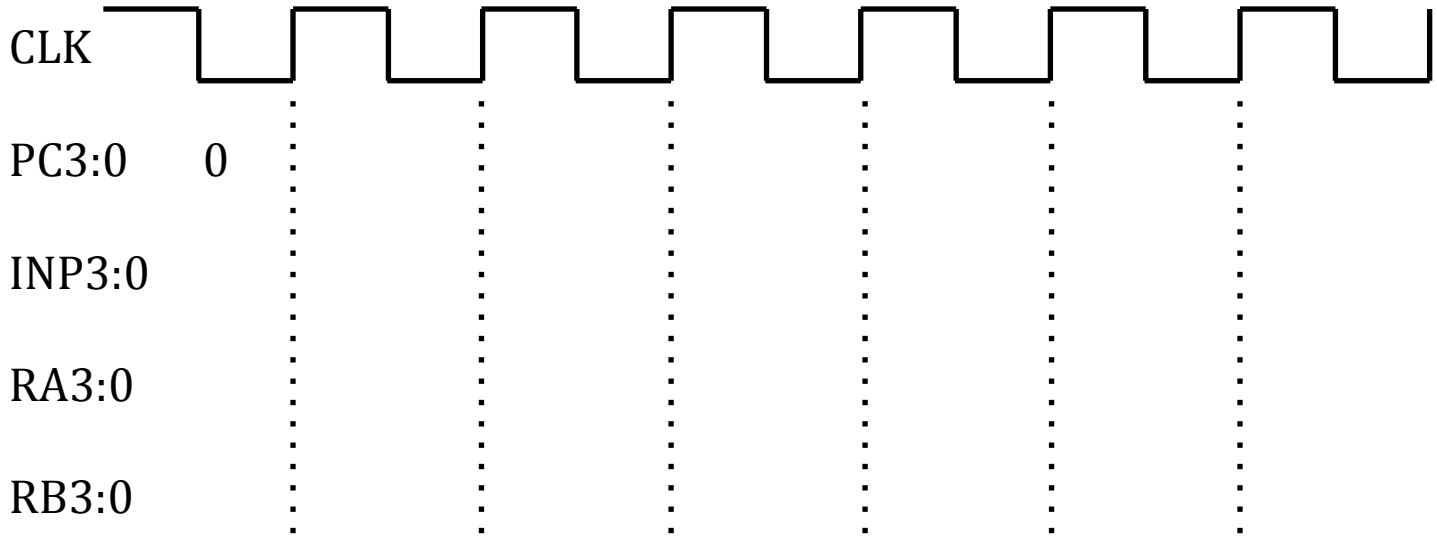
RAM Memory Range (Hex) _____ to _____

RAM Decode Equation = _____

4. A vector starting at address 0x800 in ROM contains an unknown amount of **signed numbers that are 3 bytes in length**. ***The last three byte signed number*** in the array is known to be **-512 decimal**. Write the code to count the number of negative numbers in the array and **store the final result in Y**. (10 pt.)

Page Score =

5. Refer to the CPU, Controller and ROM Contents in Appendix A to complete the Voltage Timing Diagram Below. Use 'X' to indicate an unknown condition and show all answers in **HEX**. (8 pt.)



Note: RA3:0 = Register A, RB3:0 = Register B

6. Using only 2:1 decoders, flip-flops, 2:1 muxes, single bit full adders and any other elementary digital components, design the X Register Block in the G CPU. Label all signals in your design. Note: Several of these signals should match those shown in the G CPU Block Diagram. Best design = Most points. (6 pts.)

Page Score =

7. For the next set of questions, see the G CPU shown in Appendix B. Fill in the cycle table below for the ***second pass*** of the line of code shown below. (7 pt.)

STAB 2,Y

Cycle	Addr Bus	Data Bus	IR	PC	R/-W	B Reg	Y Reg	Dev driving Addr Bus	Dev Driving Data Bus
1									
2									
3									
4									

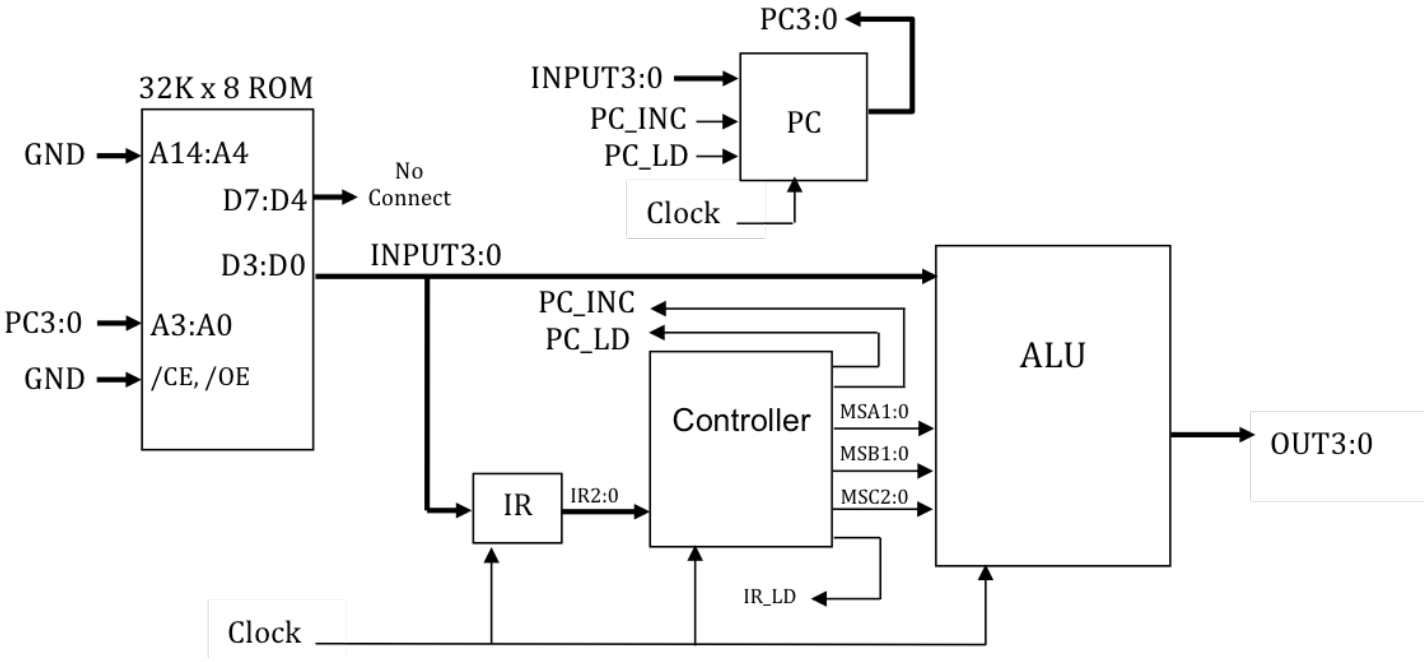
8. Show the modified contents of RAM, after the code has executed in Appendix B. Note: show only the locations modified in RAM at execute (run) time. Show both the modified addresses and data. (2 pt.)

9. Assuming that only one ROM is used in the system for the code in Appendix B, what is the maximum size possible for this ROM? (1 pt.)

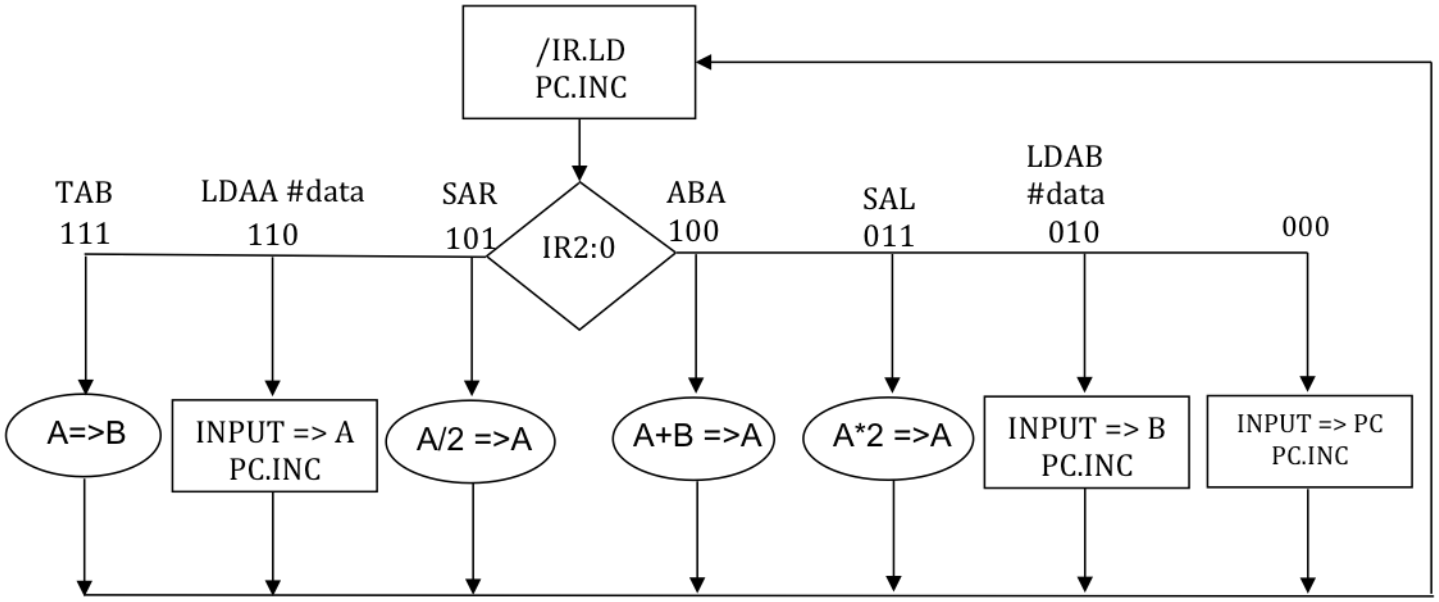
10. How many bits of storage are required if a ROM is used to implement the G CPU Controller? (2 pt.)

Page Score =

Appendix A. *Elementary CPU (Lab #9), Controller ASM and ROM Contents*



Controller ASM:



32K x 8 ROM Contents:

Address	=>	0	1	2	3	4	5	6
Data (Hex)	=>	F6	FA	F5	F2	FC	F4	F7

Page Score =

Appendix B. G-CPU Code for Problem #7 (space on left for hand assembly):

```
                ORG     $0
                LDX     #$0
                LDY     #$4000
                LDAA    #8
                STAA    0,Y

T1              LDAA    2,X
                TAB
                SUM_AB
                STAB    2,Y         ;show 2nd pass of executing this code
                INX
                INY

                LDAA    $4000
                LDAB    #$FE
                SUM_BA
                STAA    $4000
                BNE     T1

END             BRA     END
```


Page Score =