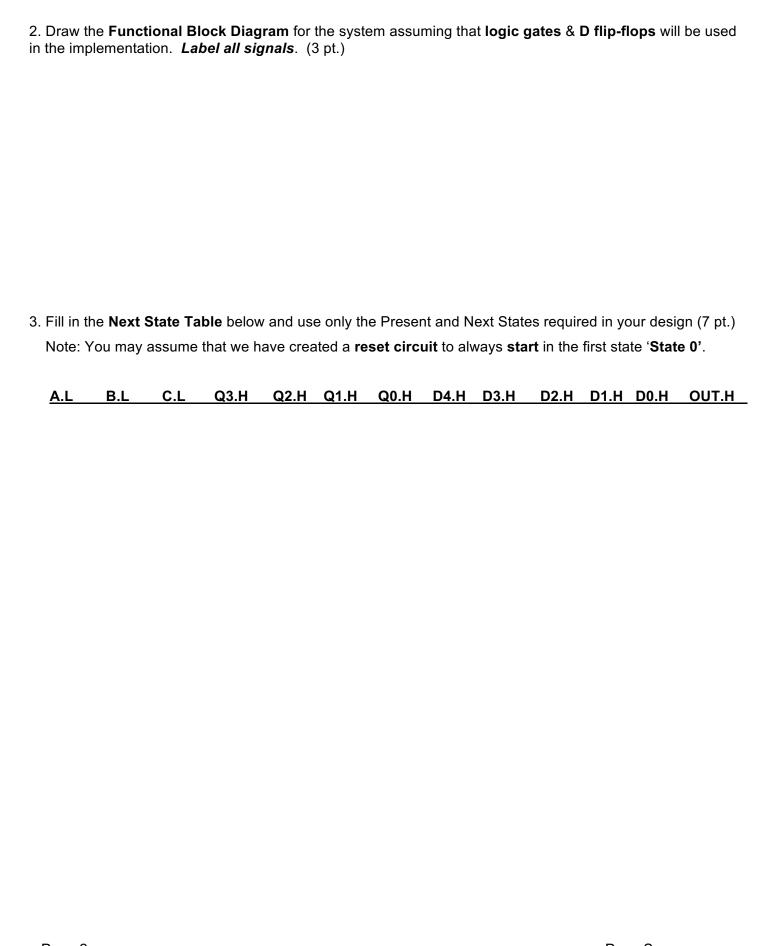
Last Name	First Name				
UF ID#					
Open book/open notes, 90-minute exam. No electronic devices permitted.					
=> 4 points	Page 2 => 10 points				
=> 6 points	Page 4 => 10 points				
=> 15 points	Page 6 => 5 points				
TOTAL => (50 pt.)					
Grade Review Information: (NOTE: deadline of request for grade review is the day the exam is returned.)					
	UF ID#  90-minute exam. No electronic devic  => 4 points  => 6 points  => 15 points  TOTAL =>				

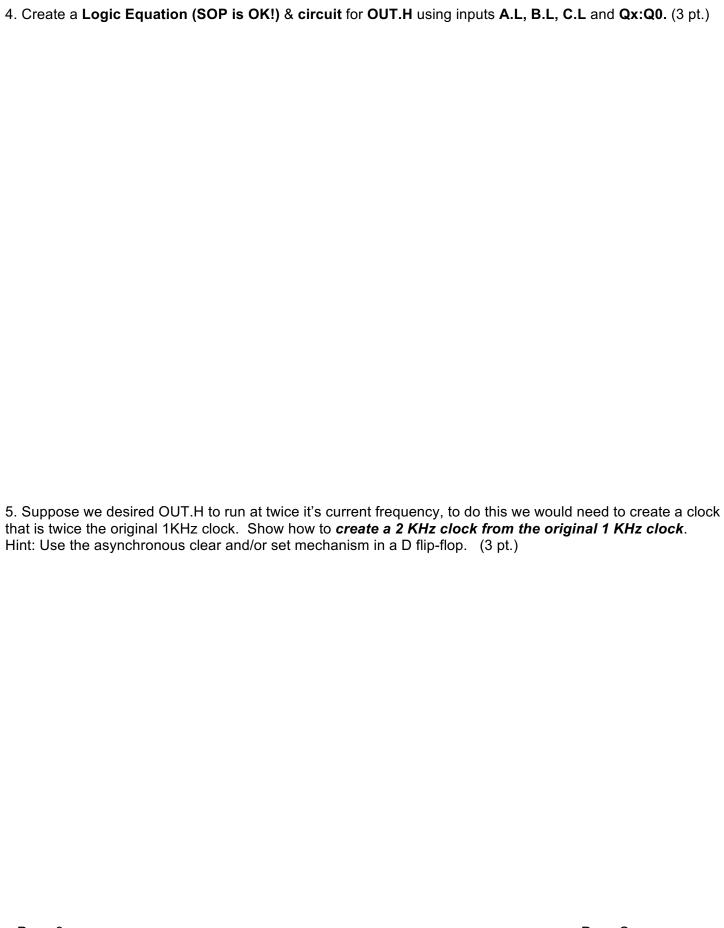
You are given a 1 KHz clock for the following problem. Design a state machine that creates an output (OUT.H) based on three input variables: A.L, B.L and C.L Assume ONE and ONLY one of the three INPUT variables will be TRUE at any given time.

If A = T, output a 500 Hz 50% Duty Cycle square wave. Else If B = T, output a 333.3 Hz 33.3% Duty Cycle square wave. Else if C = T output a 250 Hz 25% Duty Cycle square wave. Recall: Frequency = 1/Period and Duty Cycle = 100% \* (Time High/Period). Best Design = Most pts.

1. Draw the Flow Chart below for the State Machine. Don't forget to number your states! (4 pt.).



Page 2 Page Score =



Page 3 Page Score =

address \$1FFF for your loo		stored in RAM. Use <b>X as</b>	a pointer to the data and
	·····		

Page 4 Page Score =

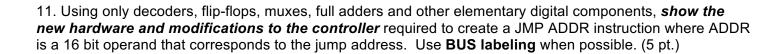
6.	What is the effective address for the LDY #\$0 instruction?	<b>Hex</b> (1 pt.)
7.	What is the effective address for the STAA 0,X instruction the 1 <sup>st</sup> time it is executed?	
		<b>Hex</b> (1 pt.)
8.	How many RAM memory locations are modified by this program?	_ <b>Decimal</b> (2 pt.)
9.	What are the values in RAM when the program has completed? (2 pt.)	
	\$1000 = Hex \$1001 = He	эx

10. In Appendix A, we are now using a **SLOW ROM** to fetch code. This ROM takes **2** cycles per memory fetch. i.e. **2** clock periods instead of **1** to fetch a byte out of memory. Fill in the cycle table below for the **1**<sup>st</sup> loop pass for the lines of code shown below assuming that **2** cycles instead of one will be required to fetch a memory byte out of ROM. RAM still has 1 cycle R/W to/from memory. Label simply "**NEW**" for new states in the controller ASM below. (9 pt.)

OR\_BA ;From Appendix A, show execution of the 1<sup>st</sup> pass of this code STAA 0,X

Cyala	Controller <u>State</u>	Addr Bus	<u>Data Bus</u>	ID I	R/-W	A Reg	Address Mux Sel1:0	Dev Outputting <u>To Data Bus</u>
<u>Cycle</u>	State	Addi bus	Data bus	<u>IR</u>	<u>K/-VV</u>	A Reg	iviux Sei i.u	10 Data Bus
1		000F						
2								
3								
4								
5								
6								
7								
8	<u> </u>							
υ								<u> </u>
9	L	<b>l</b>	<u> </u>	L	<u> </u>	L	L	

Page 5



Page 6 Page Score =

## **Appendix A. G-CPU Code for Problems 6 - 10:**

Note1: 8K ROM starting address \$0 and 8K RAM starting at address \$1000.

Note2: ROM is a slow device that requires TWO cycles to read in a value from it.

	ORG LDAB STAB LDY	\$0 #\$F3 \$2FFF #\$0
	LDX	#\$1000
T1:	LDAA	0,Y
	LDAB	#\$88
	OR_BA	
	STAA	0,X
	INX	
	INY	
	LDAA	\$2FFF
	LDAB	#1
	SUM_BA	
	STAA	#2FFF
	BNE	T1
END1	BEQ	END1

Note: Use the space below to hand assemble instructions as needed in 6 - 10:

Page 7 Page Score =