EEL3701 – Dr. Gugel
Spring 2015
Final Quiz

Last Name _____ First Name KEY

UF ID# _____

Open book/open notes, **90-minute** exam to be done in **non-red** pen. ***No electronic devices permitted.***

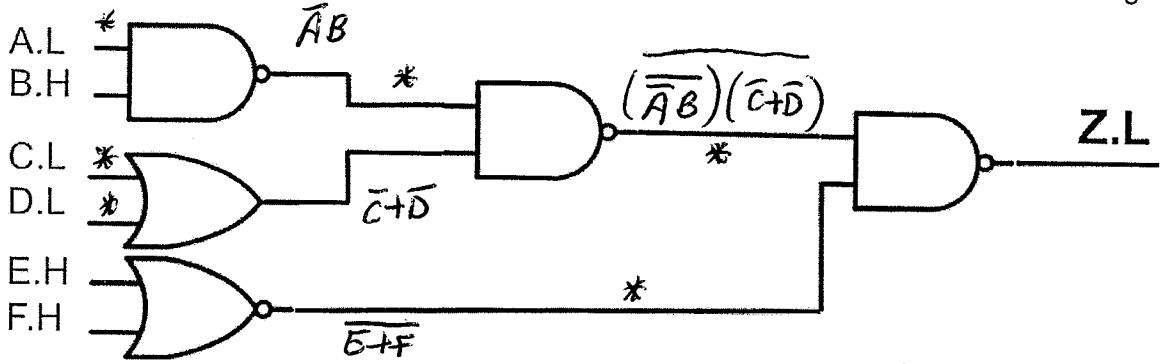
Point System: Page 1 => 10 points _____ Page 2 => 14 points _____

Page 3 => 14 points _____ Page 4 => 12 points _____

TOTAL => _____ (50 pt.)

Grade Review Information: (*NOTE: deadline of request for grade review is the day the exam is returned.*)

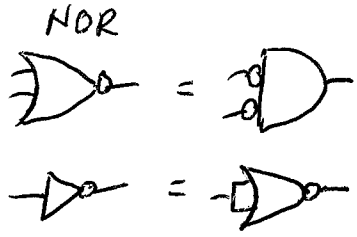
1. For the circuit below, derive Z.L. **Do not simplify.** Write all intermediate terms as high true. (5 pt.)

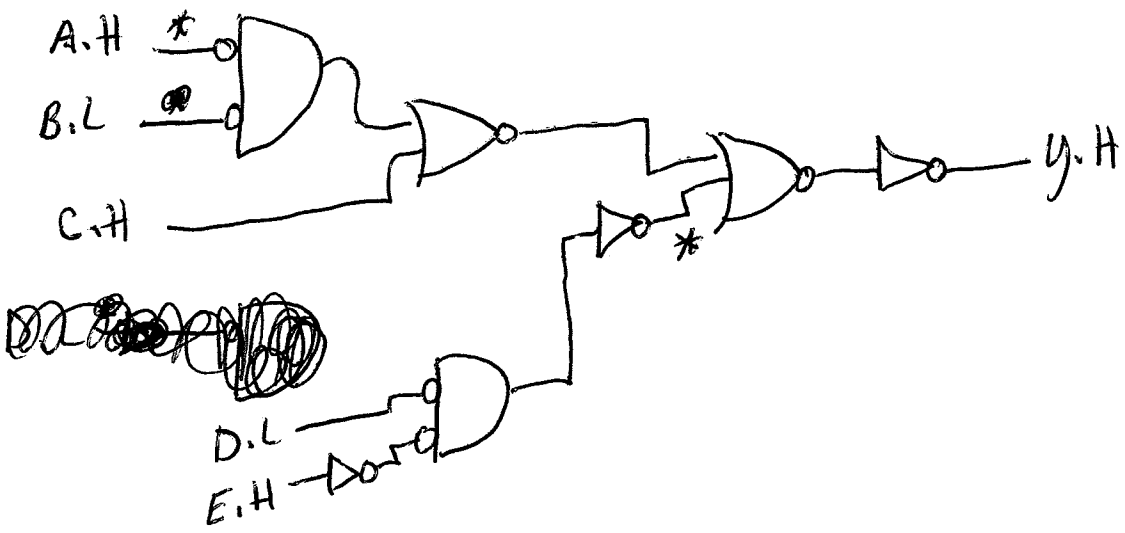


Z.L = $\overline{(\overline{\overline{A}B})(\overline{C}+\overline{D})\cdot(\overline{E}+F)}$

2. Implement the logic equation below using 2 Input NOR Gates only. (5 pt.)

$Y = (\overline{A}*B)+C+\overline{(D*E)}$; A.H, B.L, C.H, D.L, E.H, Y.H





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KEY

3. A student has interfaced a ***8K x 8 ROM*** with the G-CPU ***starting at address zero***. The student also has interfaced an ***16K x 8 RAM that begins immediately after the ROM in the G-CPU memory map***. What is the memory range and logic equation for the RAM device? (4 pt.)

RAM Memory Range (Hex) 2000 to 5FFF

RAM Decode Equation = $\overline{CIK} \cdot \overline{A15}\,(\overline{A14} \cdot A13 + A14 \cdot \overline{A13}) = CIK \cdot \overline{A15}(A13 \oplus A14)$

2000 - 3FFF 001X/XXXX/XXXX/XXXX 010X/XXXX/XXXX/XXXX

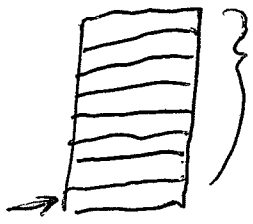
4. A vector starting at address 0x800 in ROM contains an unknown amount of **signed numbers that are 3 bytes in length**. ***The last three byte signed number*** in the array is known to be **-512 decimal**. Write the code to count the number of negative numbers in the array and **store the final result in Y**. (10 pt.)

```
LDX #$0x800 ; X ptr to data
LDY #0      ; init counter

TOP Ldaa 0,X ; get lower byte
    BNE INC_Y ; =0?

    Ldaa 1,X
    Ldab #2
    Sum_ba
    BNE INC_Y

    Ldaa 2,X
    Ldab #1
    Sum_ba
    BNE INC_Y

DONE BEQ DONE
```

-512 = 00/02/00
FF FD FF
+1
FF/FE/00

```
INC_Y: Ldaa 2,X
       BP SKIP
       INY
SKIP   INX
       INX
       INX
       Ldaa #0
       BEQ TOP
```

OK to count or not count -512



RAM 2000 - 3FFF 8K 4000 - 5FFF 8K
ROM 0 - 1FFF

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0 – 1FFF 8K 0010 0000 0000 0000 OXFFFE 20
6 – FFFF8K 1101 1111 1111 1111

3. A student has interfaced a ***8K x 8 ROM*** with the G-CPU ***starting at address zero***. The student also has interfaced an ***16K x 8 RAM that begins immediately after the ROM in the G-CPU memory map***. What is the memory range and logic equation for the RAM device? (4 pt.)

RAM Memory Range (Hex) 2000 to 5fff

RAM Decode Equation = $\overline{A15}\,A14\,\overline{A13} + A15\,A14\,\overline{A13}$

2000 – 3fff 8K

4. A vector starting at address 0x800 in ROM contains an unknown amount of **signed numbers that are 3 bytes in length**. ***The last three byte signed number*** in the array is known to be **-512 decimal**. Write the code to count the number of negative numbers in the array and **store the final result in Y**. (10 pt.) 4-68

```
LDX #$0800   -- just init things
LDY #$0000
~~LDAB #$FE~~

LOOP: (0x0005)
      LDAA $02,X
(0x0009) BP $000D (Check)
      INY    -- if neg, inc Y

(0x000D) -- Check if we are done
Check: LDAB 0xFF01  -- Chek for
      SUM-BA          0xFF
      BNE $0005 (LOOP)

0013  LdAB 0xd0   -- Chek for FE
      LDAA $01,X
      SUM_BA
      BNE $0005 (LOOP)

      LDAA $00,X   -- Chek for 0
001F  INX  -- inc X 3 times
      INX
      INX
      BNE $0005 (LOOP)
END   BEQ END
```


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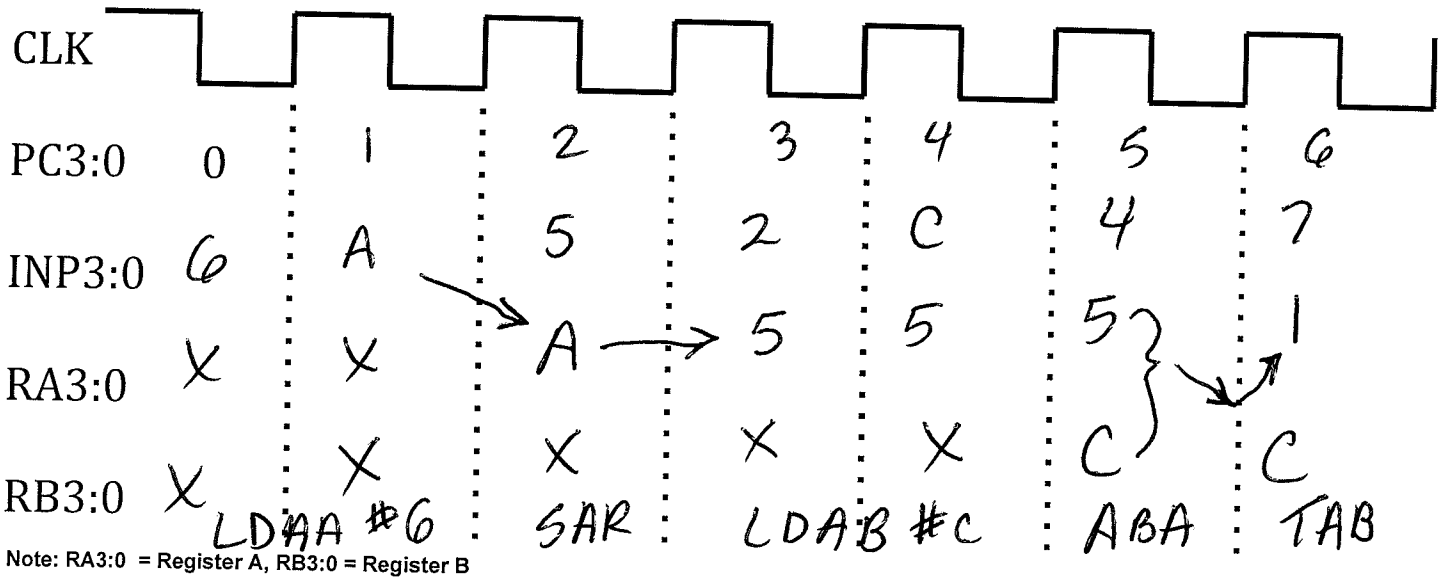
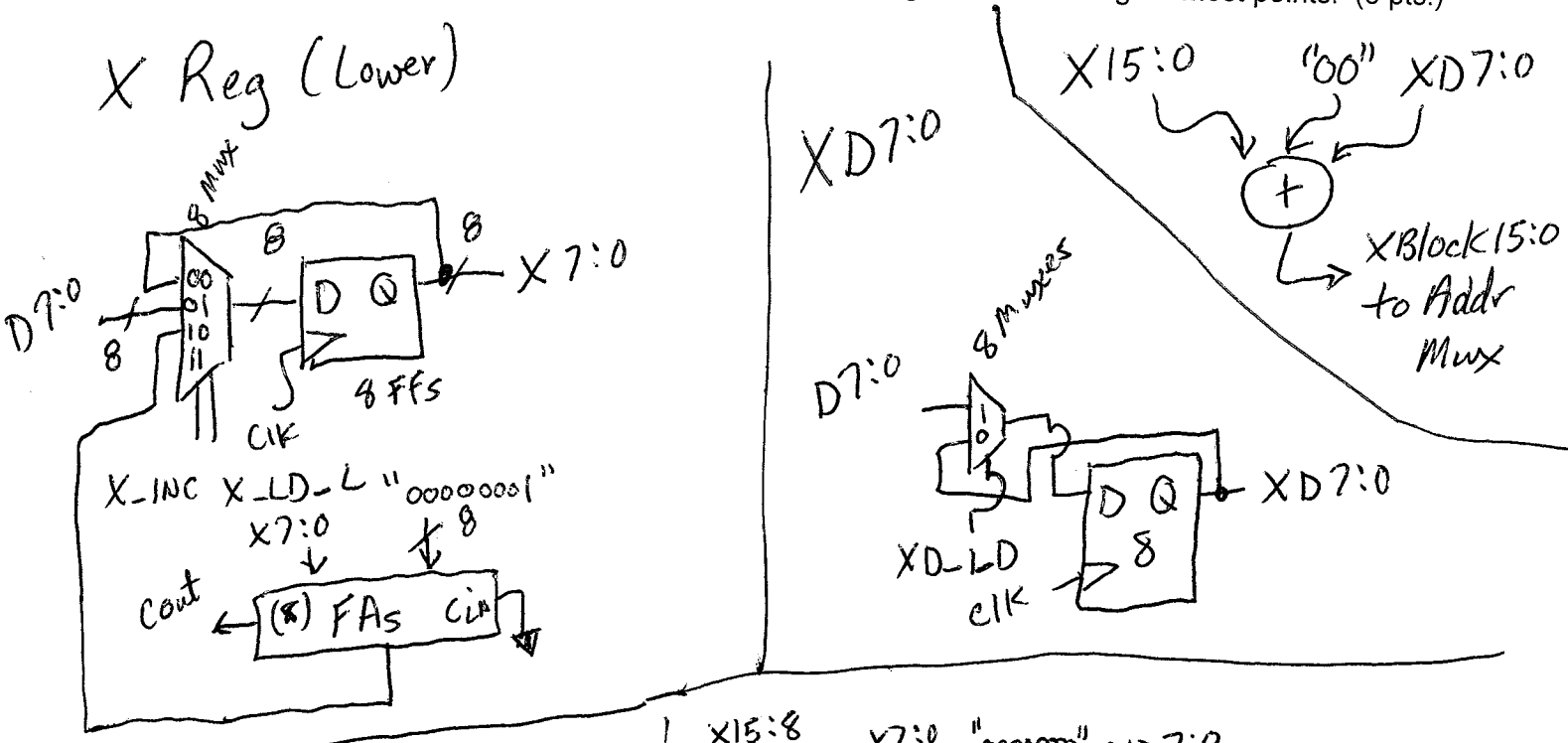
5. Refer to the CPU, Controller and ROM Contents in Appendix A to complete the Voltage Timing Diagram Below. Use 'X' to indicate an unknown condition and show all answers in **HEX**. (8 pt.)



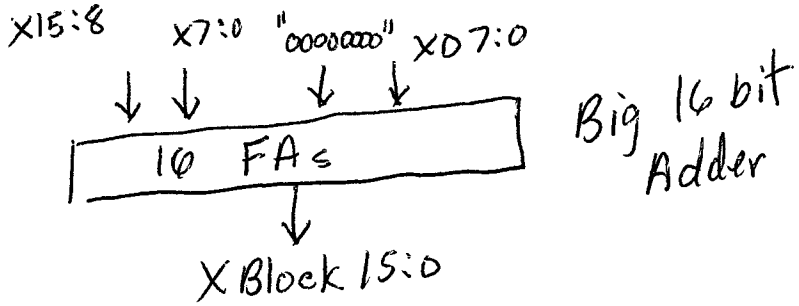
Note: RA3:0 = Register A, RB3:0 = Register B

6. Using only 2:1 decoders, flip-flops, 2:1 muxes, single bit full adders and any other elementary digital components, design the X Register Block in the G CPU. Label all signals in your design. Note: Several of these signals should match those shown in the G CPU Block Diagram. Best design = Most points. (6 pts.)



Same as above
8 new Mux, 8 new F/Fs
8 FAs; replace
X_LD_L with
X_LD_H

Cout → Cin and add "00"
X7:0 → X15:8



Big 16 bit Adder

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7. For the next set of questions, see the G CPU shown in Appendix B. Fill in the cycle table below for the ***second pass*** of the line of code shown below. (7 pt.)

STAB 2,Y

Cycle	Addr Bus	Data Bus	IR	PC	R/-W	B Reg	Y Reg	Dev driving Addr Bus	Dev Driving Data Bus
1	000E	13	15	000E	1	12	4001	PC	Rom
2	000E	13	13	000E	1	12	4001	PC	ROM
3	000F	02	13	000F	1	12	4001	PC	Rom
4	4003	12	13	0010		12	4001	Y Block	CPU

8. Show the modified contents of RAM, after the code has executed in Appendix B. Note: show only the locations modified in RAM at execute (run) time. Show both the modified addresses and data. (2 pt.)

4000 [00] 4002 [00] 4003 [12]

4004 [00] 4005 [80]

9. Assuming that only one ROM is used in the system for the code in Appendix B, what is the maximum size possible for this ROM? (1 pt.)

0 - 3FFF

2^{14} => 16K x 8

10. How many bits of storage are required if a ROM is used to implement the G CPU Controller? (2 pt.)

$2^8 \times 18$ or 256×18 } +2

256×26 } +2.5 extra 0.5!

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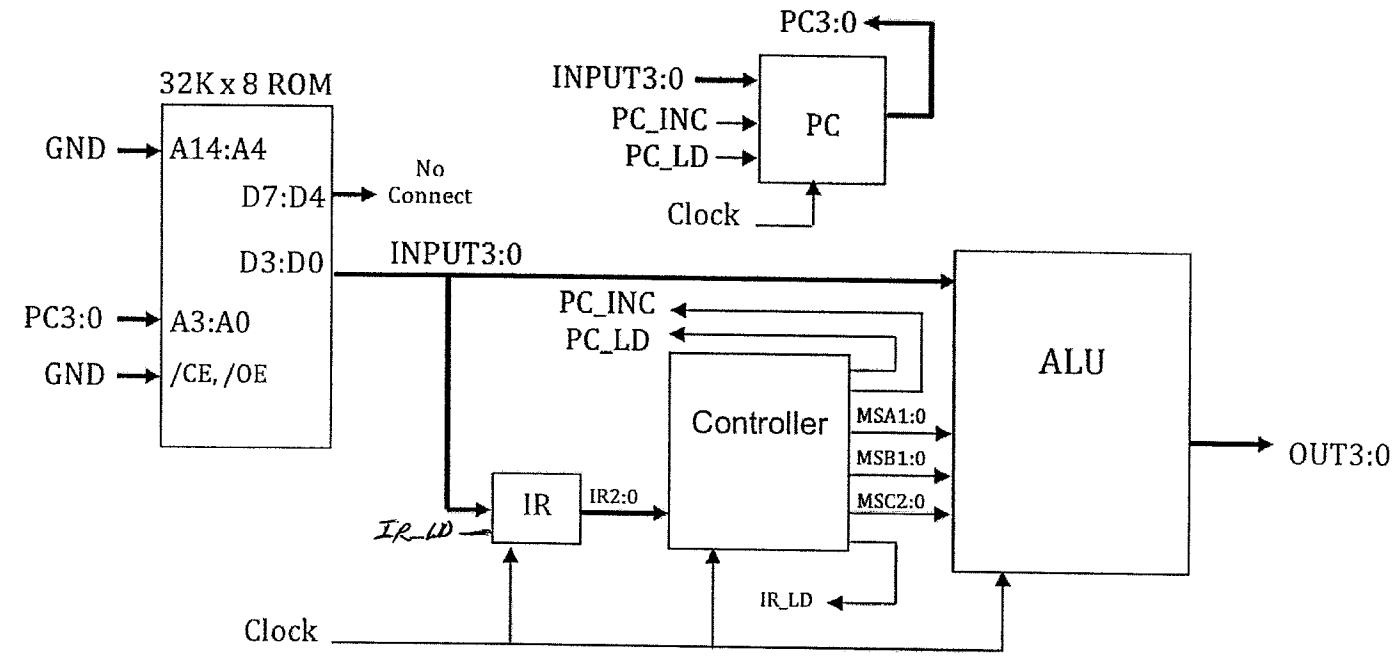
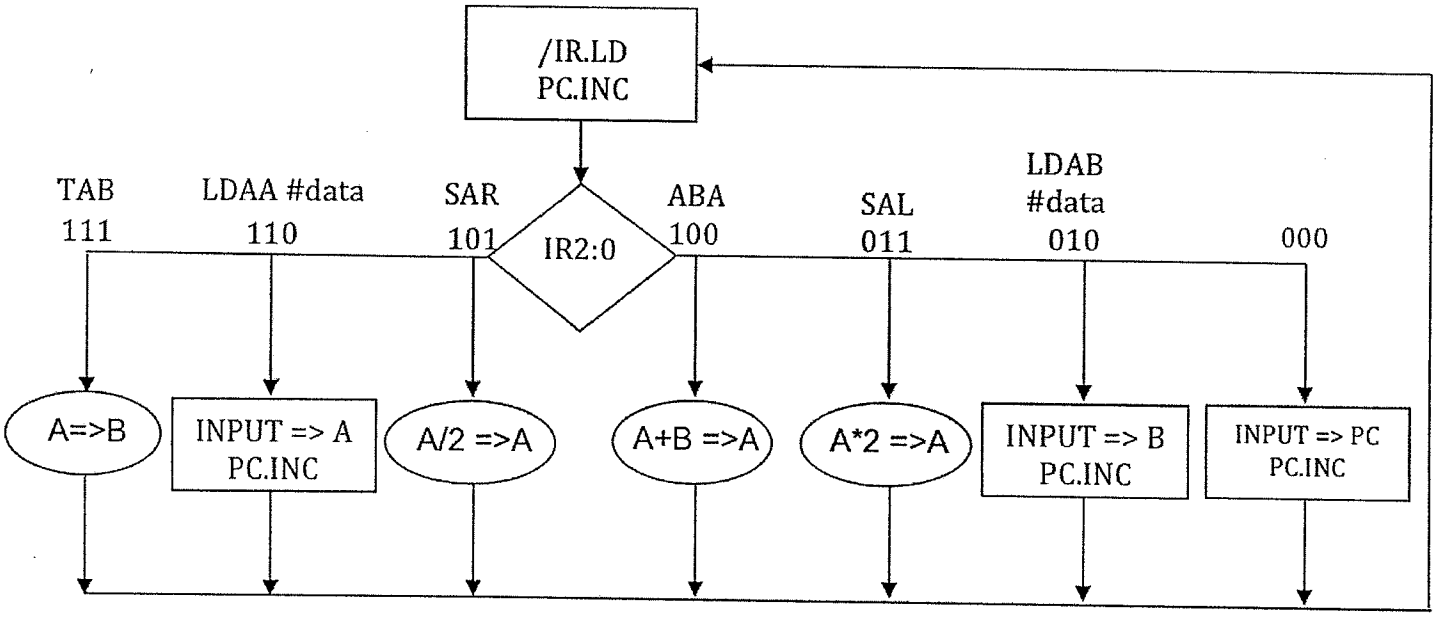
Appendix A. *Elementary CPU (Lab #9), Controller ASM and ROM Contents*



Controller ASM:



32K x 8 ROM Contents:

Ldaa #6 ; 2cy.
SAR ; 1cy.
LDAB #C ; 2cy.
ABA ; 1cy.
TAB ; 1cy

Address	=>	0	1	2	3	4	5	6
Data (Hex)	=>	F6	FA	F5	F2	FC	F4	F7

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Appendix B. G-CPU Code for Problem #7 (space on left for hand assembly):

```
            ORG     $0
            LDX     #$0
            LDY     #$4000
            LDAA    #8
            STAA    0,Y

T1          LDAA    2,X
            TAB
            SUM_AB
            STAB    2,Y
            INX
            INY

            LDAA    $4000
            LDAB    #$FE
            SUM_BA
            STAA    $4000
            BNE     T1

END         BRA     END
```

;show 2nd pass of executing this code

1st Pass	2nd Pass
X=0	X=1
y=4000	y=4001
A=B=00	A=B=9
Sum=0	Sum=12
4002[00]	4003[12]

3rd Pass	4th Pass
X=2	X=3
Sum=00	Sum=80

Addr	Data	
0	08	LDX #0
1	00	
2	00	
3	09	LDY #$4000
4	00	
5	40	
6	02	LDAA #8
7	08	
8	11	STAA 0,Y
9	00	
A	0C	LDAA 2,X
B	02	

Addr	Data	
C	00	TAB
D	15	SUM_AB
E	13	STAB 2,Y
F	02	

4000[00] 4002[00] 4003[12]

4004[00] 4005[80]

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