Exam 1P

May the Schwartz be with you!

Go Gators!

Last Name, First Name

UF CIMAR/MIL AV (Robot) Indy (Race Car) Challenge

Good luck!

Please read carefully.

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may **not** use any notes, HW, labs, other books, scratch paper, or calculators.*
- *This exam counts for 27% of your total course grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **10** distinct pages. Sign your name and add the date below. (If we struggle to read your name, **you will lose points**.)*
- *For circuit diagrams, use **labels** to identify physical connections instead of drawing lines (wires). Failure to do so will cost you one point per problem.*
- *For anything undefined, if necessary, state a reasonable assumption.*
- *Failure to follow the below rules will result in **NO** partial credit.*
  - *The **base** (radix) of all number must be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MU… …rs, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (9 Oct 2019) _____

Regrade comments below: Give page # and problem # and reason for the petition.
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Problems	Available	Points
1	13	
2	10	
3-4	11	
5	12	
6	13	
7	14	
8	16	
9	11	
TOTAL	100	

Exam 1P

Last Name, First Name

[13%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 5 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $\mathbf{311}_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 3 min b) Determine the **10-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number $\mathbf{-311}_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 3 min c) What is $256_{10} - 311_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $256 = 2^8$. You must **show all work.**

$(\mathbf{256_{10} - 311_{10}})_{2\text{ 10-bit 2's comp}}$: _____

Exam 1P

Last Name, First Name

(3%) 3 min 1. d) What is $-256_{10} - 311_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $256 = 2^8$. You must **show all work**

$(-256_{10} - 311_{10})_{2\ 10\text{-bit 2's comp}}$: _____

[10%] 7 min 2. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. Use only **NOR** gates (**or** their mixed-logic equivalent). Minimize the **total number of gates**. You are free to choose the activation levels ; but the chosen activation-levels should optimize your solution. **Check twice** that you correctly read the equation!

$$UF = \overline{\left[\left(\overline{N + \overline{U}}\right) + M\right] * \left(\overline{O * \overline{N} + E}\right)}$$

N( )___

U( )___

M( )___

O( )___ _____UF( )

E( )___

Exam 1P

Last Name, First Name

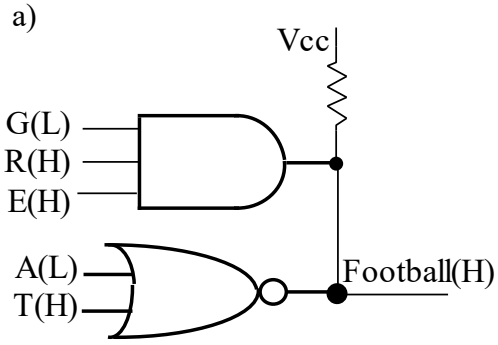
[5%] 5 min

3. **Simplify** the following logic equation using **only Boolean identities, laws, or theorems**. Show all work. Give the solution in MSOP or MPOS form in **lexical** order. **Check twice** that you correctly read the equation!

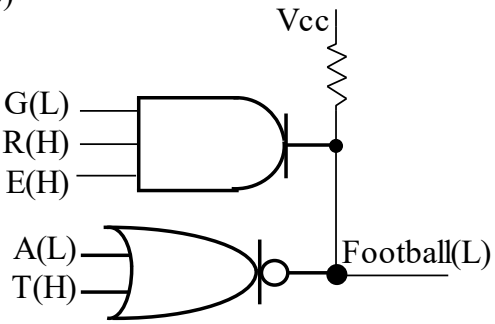
$$UF = \overline{\left(\overline{\bar{I} + S}\right) * \left[\overline{\left(B + \bar{E}\right)} + \bar{S} + T\right]}$$

[6%] 4. Analyze the below circuits **carefully**. What are the equations for the outputs of the two similar circuits of parts a and b? Give the solution in **MSOP** or **MPOS** form in **lexical** order.

(%) 3 min a)



(%) 3 min b)

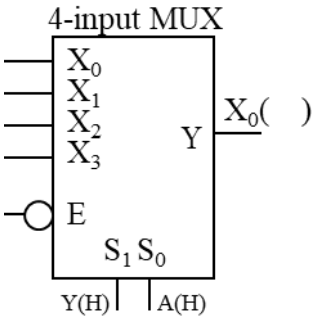


Exam 1P

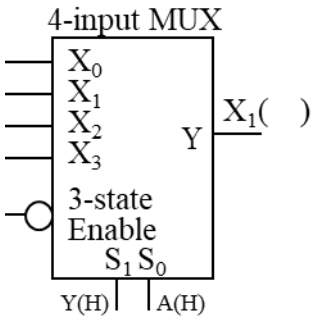
Last Name, First Name

[12%] 2 min 5. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The three below problems are **independent** of each other, but the equations are identical [other than the subscripts on X].)

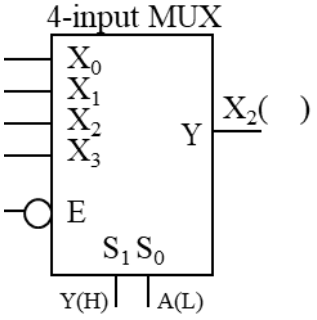
(%) 6 min a) $X_0 = \overline{W}\,C + Y * \overline{(B * \overline{A})}\,C$ (Note the **NON** tri-state enable.)



(%) 3 min b) $X_1 = \overline{W}\,C + Y * \overline{(B * \overline{A})}\,C$ (Note the **tri-state** enable.)



(%) 2 min c) $X_2 = \overline{W}\,C + Y * \overline{(B * \overline{A})}\,C$ (Note the **NON** tri-state enable.)



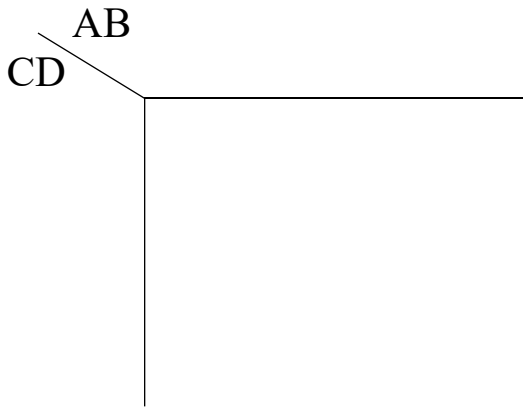
Exam 1P

Last Name, First Name

[13%] 6. Use the below equation for this problem.

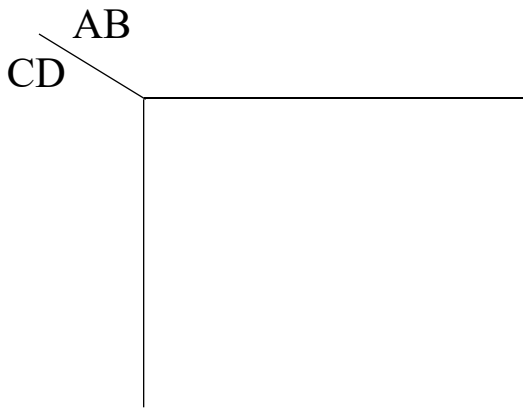
$$Y = (\bar{A} + B + \bar{C} + D)(A + \bar{C} + \bar{D}) * (\bar{A} + C + D) * (A + \bar{C} + D) * (\bar{B} + C + D) * (A + C + D)$$

(8%) 8 min a) Use a K-Map to simplify the above equation. Give the result in **MPOS** form and lexical order. Label **ALL** circles.



Y_{MPOS} =

(4%) 3 min b) If the terms ABCD=0001 and ABCD=1011, i.e., the textbook's d(1) and d(11), are **DON'T CAREs (X)**, determine the new **MSOP** equation, in lexical order. Label **ALL** circles.



Y_{MSOP} =

(1%) 1 min c) Are the above equations (in parts a and b) **equivalent**? Why or why not?

_____

_____

_____

Exam 1P

Last Name, First Name

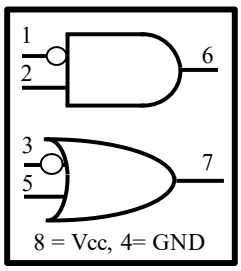
[14%] 7. In this problem, you will design a mixed-logic circuit diagram and some input and output circuits.

(6%) 5 min

a) Draw the **mixed-logic circuit** diagram to directly implement these two equations using parts from the 74'UF chip shown. These should be **circuit diagrams,** not layout diagrams. Choose the optimal (best) activation-levels for A and B. **Label the pin numbers** on your circuit diagram. X must be **active-high**, i.e., **X(H)**.

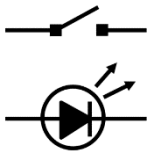
$$X = \overline{A + B}$$
$$Y = A * B$$

74'UF



(8%) 3 min

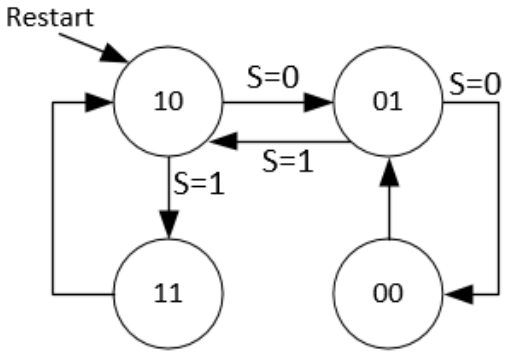
b) Draw the required switch **circuits** and LED **circuits** to complete the circuit design for this problem. (These should be **circuit diagrams, not** layout diagrams.) Draw the switches in their **true** positions. Both a switch and an LED circuit symbol are shown here. (The switch shown is in its open position.) Do **not** draw unnecessary components.



Exam 1P

Last Name, First Name

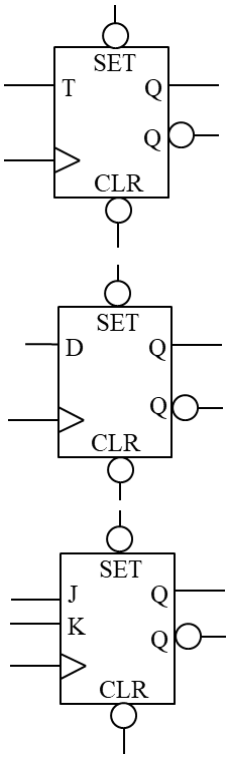
[16%] 3 min 8. Design a system that counts with two bits as shown, using the minimum number of flip-flops necessary. The system must **asynchronously** go to state "10" when **Restart** (**active-low**) goes true. The input **S** is **active-low**. Use a **T-FF** for the **least** significant bit of your design, a **JK-FF** for the **most** significant bit, and **D-FF**(s) for **any other** bits that you think are necessary. The two count outputs should be active-high, **Q_1(H)** and **Q_0(H)**. An active-low output, **Y(L)**, should only be true when the count is 01. Note: All the given FFs have **asynchronous** clear and set inputs as shown.



(2%) 5 min a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into** or **out of** the **box**, on the left or right, respectively. This is **not** a circuit diagram.

Inputs

Outputs



6 min (7%) b) Complete the next-state **truth** table (**in counting order**).

Exam 1P

Last Name, First Name

(3%) 5 min

8. c) Find the required **simplified** (MSOP or MPOS) equations for **ONLY** the following signals: the **T-FF input** and the **Y output**. If necessary (i.e., not done already done in the functional block diagram), also determine the equations necessary to **asynchronously** go to state **10** when **Restart** (**active-low**) goes true.

(4%) 5 min

d) Design the complete circuit, using the T-FF, D-FF(s), and JK-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronously** go to state **10** when **Restart** (**active-low**) goes true. Equations not calculated should be shown as an empty box with the necessary inputs and outputs.

Inputs

Outputs

Exam 1P

Last Name, First Name

[11%] 9. In this problem you will design a 6-input MUX with no enable.

(1%) 3 min

a) Draw a functional block diagram for a 6-input MUX with no enable. Use select lines labeled S_I and inputs labeled X_J (with the normally used subscripts). All S_I and X_J are active-high, as is the output Y.

(5%) 4 min

b) Use a single 4-input MUX and a single 2-input MUX, both with single tri-state enables, to design a 6-input MUX with no enable. For each of these MUXes, use select lines labeled S_I and inputs labeled X_J (with the normally used subscripts). All S_I and X_J are active-high, as are these MUX outputs. Use the **minimum number** of additional SSI component. Choose the activation levels of the enables to **minimize** your additional SSI components.

(5%) 5 min

c) Use a single 4-input MUX and as many 2-input MUXes as needed (but the minimum number), all with single **non**-tri-state enables, to design a 6-input MUX with no enable. For each of these MUXes, use select lines labeled S_I and inputs labeled X_J (with the normally used subscripts). All S_I and X_J are active-high, as are these MUX outputs. Use the **minimum number** of additional SSI component. Choose the activation levels of the enables to **minimize** your additional SSI components.