# Exam 1P

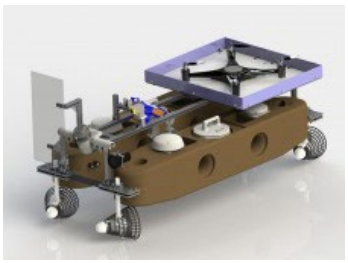
*10-Jun-19 -- 5:41 PM*

*May the Schwartz be with you!*

Last Name, First Name

*Instructions:*

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may not use any notes, HW, labs, other books, scratch paper, or calculators.*
- *This exam counts for 28% of your total course grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of 11 distinct pages. Sign your name and add the date below. (If we struggle to read your name, **you will lose points**.)*
- *For anything undefined, if necessary, state a reasonable assumption.*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & $D_3$ before $D_2$).*



*PropaGator 1: World Champion, 2013 RoboBoat Competition*

***Good luck!***

***Please read carefully.***

***Go Gators!***

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (27 Feb 2019) _____

| Regrade comments below: Give page # and problem # and reason for the petition. |
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| Pages | Available | Points |
|---|---|---|
| 2-3 | 19 | |
| 4 | 10 | |
| 5 | 11 | |
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| 7 | 10 | |
| 8-9 | 17 | |
| 10 | 15 | |
| 11 | 8 | |
| TOTAL | 100 | |

# Exam 1P

Last Name, First Name

[13%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $415_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 3 min b) Determine the **<u>10-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number $-415_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 3 min c) What is $-415_{10} - 128_{10}$ in **<u>10-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Hint: $128 = 2^7$. You must **show <u>all</u> work.**

**$(-415_{10} - 128_{10})_{2\text{ 10-bit 2's comp}}$**: _____

# Exam 1P

Last Name, First Name

(3%) 3 min 1. d) What is $-415_{10} - 64_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $64 = 2^6$. You must **show all work**

**$(-415_{10} - 64_{10})_{2\ 10\text{-bit}\ 2\text{'s comp}}$**: _____

[6%] 6 min 2. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. Use only gates of the type shown here (**or** its mixed-logic equivalent). Minimize the **total number of gates**. You are free to choose the activation levels that are not already specified and that will optimize your solution. **Check twice** that you are correctly reading the equation!

$$UF = \overline{\left\{\left[\overline{(B + \bar{A})} * S * \bar{E}\right] + B * \bar{A}\right\} * \bar{L}}$$

B( )___

A(H)___

S( )___

E( )___ _____UF( )

L( )___

# Exam 1P

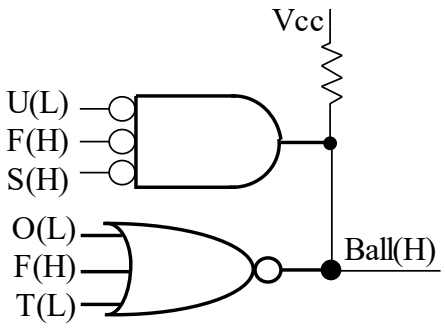
Last Name, First Name

[4%] 6 min 3. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. (Note that this equation is **NOT** the same as in the previous problem. Show all steps. Give the solution in MSOP or MPOS form in **lexical** order.

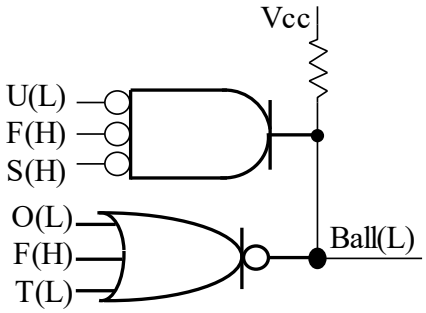
$$UF = \overline{\left\{\left[\overline{(B + \bar{A})} * S * \bar{E}\right] + \overline{(B * \bar{A})}\right\} * \bar{L}}$$

[6%] 4. Analyze the below circuits **carefully**. What are the equations for the outputs of the two similar circuits of parts a and b? Give the solution in MSOP or MPOS form in **lexical** order.

( %) 3 min a)




( %) 3 min b)



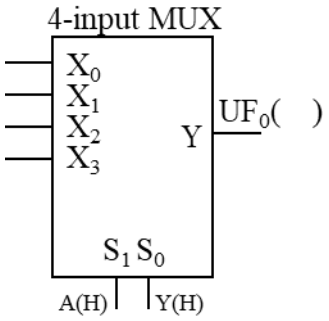
# Exam 1P

Last Name, First Name

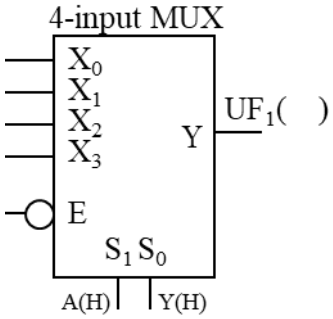
[11%] 5. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The four below problems are **independent**, but the equations are identical.)

2 min

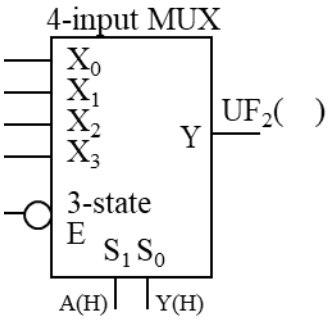
(4%) 6 min a) $\boldsymbol{UF_0 = (G + \bar{Y}) * \bar{M} + Y * (N * A) * \bar{M}}$



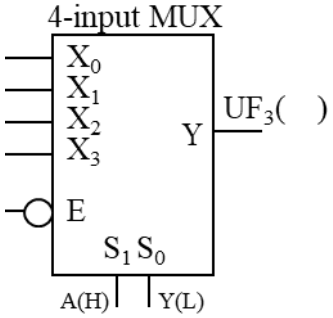

(3%) 3 min b) $\boldsymbol{UF_1 = (G + \bar{Y}) * \bar{M} + Y * (N * A) * \bar{M}}$ (Note the **NON** tri-state enable.)




(2%) 2 min c) $\boldsymbol{UF_2 = (G + \bar{Y}) * \bar{M} + Y * (N * A) * \bar{M}}$ (Note **TRI**-state enable.)




(2%) 4 min d) $\boldsymbol{UF_3 = (G + \bar{Y}) * \bar{M} + Y * (N * A) * \bar{M}}$ (Note the **NON** tristate enable.)



# Exam 1P

Last Name, First Name

[11%] 6. Use the below equation for this problem.

$$Y = (\bar{A} + B + \bar{C} + \bar{D}) * (A + \bar{B} + C + \bar{D}) * (A + B + \bar{D}) * (B + \bar{C} + D) * (B + C + D)$$

(7%) 6 min a) Simply the above equation and put the result in **MPOS** form, in lexical order. Label **ALL** circles.

AB
CD

**$Y_{MPOS}$ =**

(3%) 3 min b) If the terms ABCD=0111 and ABCD=1000, i.e., the textbook's d(7) and d(8), are **DON'T CAREs (X)**, determine the new **MSOP** equations, in lexical order. Label **ALL** circles.

AB
CD

**$Y_{MSOP}$ =**

(1%) 1 min c) Are the above equations (in parts a and b) **equivalent**? Why or why not?

# Exam 1P

Last Name, First Name

[10%] 7. Use the below circuit for this problem.

(5%) 5 min a) Draw the **mixed-logic circuit** diagram to directly implement (i.e., do **NOT** simplify) the below equation using parts from any **one single chip**, with **A active-high**. Use the **minimum number of gates** from this **single** chip. (This should be a **circuit diagram,** not a layout diagram.)

$$X = \overline{\overline{A} + B} * \overline{C}$$

(3%) 3 min b) Draw the required switch circuits and LED circuits to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

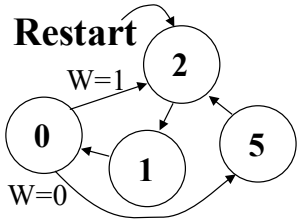
(2%) 2 min c) Draw a **voltage timing** simulation diagram of the output of the **A** switch circuit when **the switch is moved** from **open to close**. Be sure to label both axes with appropriate scales including units.

# Exam 1P

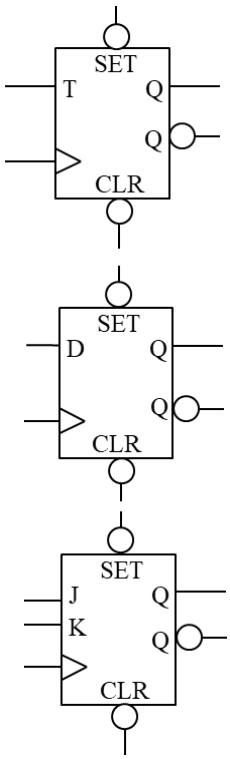
Last Name, First Name

[17%] 8. Design a system that "counts" as shown. The system must **asynchronously** go to state "2" when **Restart** (**active-high**) goes true. **W** is an **active-low** signal that determines the next "count" after "0," as shown in the figure. Use a **T-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and **D-FF**(s) for **any other** bits you might need. An **active-low** output, **Y** should be true when the "count" is "5." All other outputs should be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.

3 min




(2%) 4 min a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.




Inputs

Outputs

(7%) 6 min b) Complete the next-state **truth** table (**in counting order**).

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# Exam 1P

Last Name, First Name

(4%) 5 min 8. c) Find the required **simplified** (MSOP or MPOS) equations for **T**, **K**, and **Y**. For the other equations, you do **not** need MSOP or MPOS equations, but you **must provide** correct SOP or POS for each.

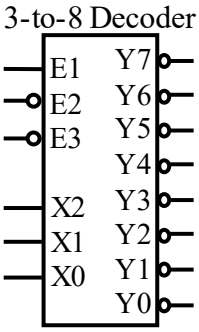
(4%) 5 min d) Design the complete circuit, using the T-FF, D-FF(s), and JK-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronous** go to state "**2**" when **Restart** (**active-high**) goes true.

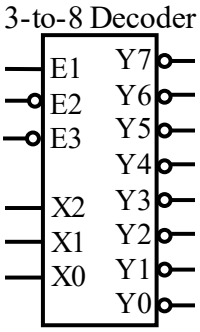
**Inputs** **Outputs**

# Exam 1P

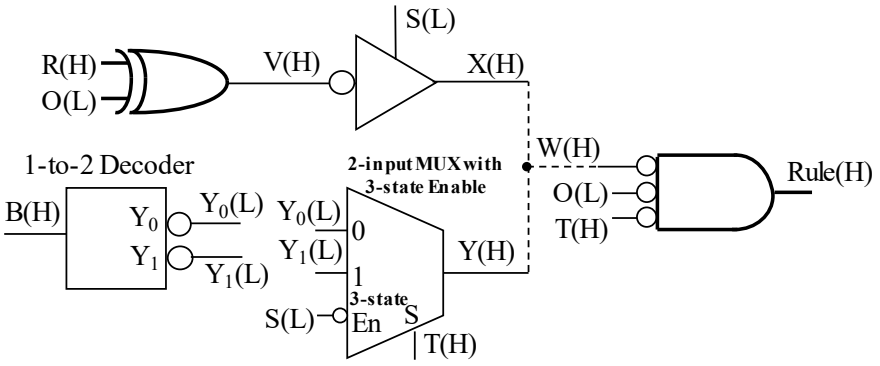
Last Name, First Name

[6%] 5 min 9. Design a 4-to-16 decoder with a single enable using only, if possible, the two below parts. If this is not possible, add a minimum number of only SSI gates in your design.




[9%] 10. Determine each of the below equations **in lexical order**. For parts a through d, assume that the dashed line is **not there**.




(1%) 2 min a) $V = f_0(R,O)$

$V =$

(2%) 3 min b) $X = f_2(V, S)$

$X =$

(1%) 2 min c) $Y_0 = f_3(B)$ and $Y_1 = f_4(B)$

$Y_0 =$

$Y_1 =$

(2%) 3 min d) $Y = f_5(Y_0, Y_1, S, T)$

$Y =$

(3%) 3 min e) If X(H) and Y(H) are connected (as shown with the dashed lines) and the combined signal is called W(H), what is the equation for $W = f_6(V, Y_0, Y_1, S, T)$.

$W =$

# Exam 1P

Last Name, First Name

[8%] 11. In this problem you will design two different 6-input multiplexers.

(1%) 2 min a) Draw a functional block diagram of a **6-input multiplexer with a single active-high enable**. All other inputs and outputs are also active-high. The inputs are X and S (with the normally used subscripts), the output is Y.

(3%) 4 min b) Design a **6-input multiplexer with a non-tri-state enable.** Use **two 2-input MUXes and one 4-input MUX**. Assume that each of these MUXes have **all** the **non**-tri-state enables (with any activation level) that you need, but do **not** use more than you need. Use no additional parts. If you can **not** solve it this way, use additional necessary parts for a **significant point reduction**.

(4%) 4 min c) Design a **6-input multiplexer with a tri-state enable.** Use the **minimum number of 2-input MUXes and 4-input MUXes**. Assume that each of these MUXes have **all** the tri-state enables (with any activation level) that you need, but do **not** use more than you need. Use no additional parts. If you can **not** solve it this way, use additional necessary parts for a **significant point reduction**.