Exam 1P

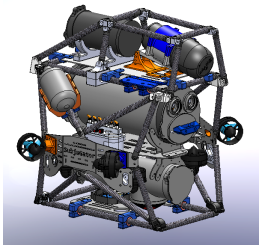
May the Schwartz be with you!

Go Gators!

Last Name, First Name

gInstructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may not use any notes, HW, labs, other books, scratch paper, or calculators.*
- *This exam counts for 28% of your total course grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of 11 distinct pages. Sign your name and add the date below. (If we struggle to read your name, **you will lose points**.)*
- *For anything undefined, if necessary, state a reasonable assumption.*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number must be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*



SubjuGator 8: Early CAD for 2019 RoboSub Competition

Good luck!

Please read carefully.

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (2 July 2019) _____

Regrade comments below: Give page # and problem # and reason for the petition.

Pages	Available	Points
2-3	19	
4	10	
5	11	
6	11	
7	8	
8-9	17	
10	11	
11	13	
TOTAL	100	

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[13%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 5 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $\mathbf{347}_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 3 min b) Determine the **10-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number $\mathbf{-347}_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 3 min c) What is $-347_{10} + 384_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $384=256+128 = 2^8+2^7$. You must **show all work.**

$\mathbf{(-347_{10} + 384_{10})}_{2\text{ 10-bit 2's comp}}$: _____

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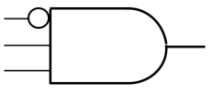
(3%) 3 min 1. d) What is $-347_{10} - 128_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $128 = 2^7$. You must **show all work**

$(-347_{10} - 128_{10})_{2\text{ 10-bit 2's comp}}$: _____

[6%] 6 min 2. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. Use only gates of the type shown here (**or** its mixed-logic equivalent). Minimize the **total number of gates**. You are free to choose the activation levels that are not already specified and that will optimize your solution. **Check twice** that you correctly read the equation!



$$USA = \left[W * \left(\overline{S + \bar{O} + C}\right)\right] * \overline{\left[\left(\overline{\bar{C} + E}\right) * R\right]}$$

W(H)___

S(L)___

O( )___

C( )___ _____USA(L)

E(H)___

R(L)___

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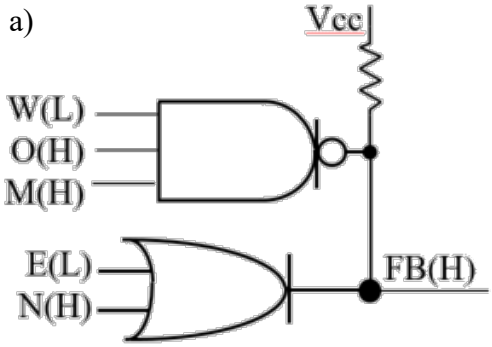
[4%] 5 min

3. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. (Note that this equation is **NOT** the same as in the previous problem. Show all steps. Give the solution in MSOP or MPOS form in **lexical** order. **Check twice** that you correctly read the equation!

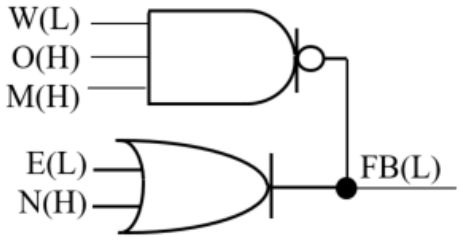
$$USA = \overline{\left[W * \left(\overline{S + \bar{O} + C}\right)\right] * \left[\left(\overline{\bar{C} + E}\right) * R\right]}$$

[6%] 4. Analyze the below circuits **carefully**. What are the equations for the outputs of the two similar circuits of parts a and b? Give the solution in MSOP or MPOS form in **lexical** order.

(%) 3 min a)



(%) 3 min b)



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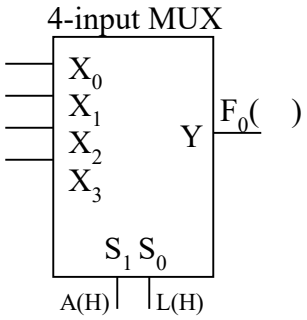
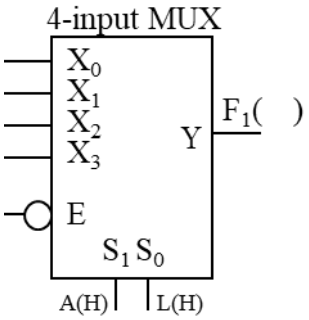
[11%] 2 min 5. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The four below problems are **independent** of each other, but the equations are identical.)

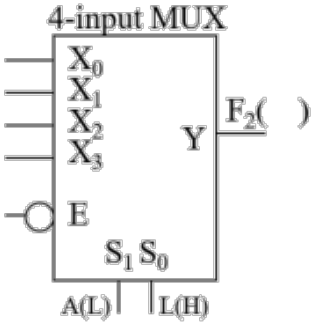
(4%) 6 min a) $\boldsymbol{F_0 = (\bar{U} + T) * B * \overline{(A * \bar{L})}}$



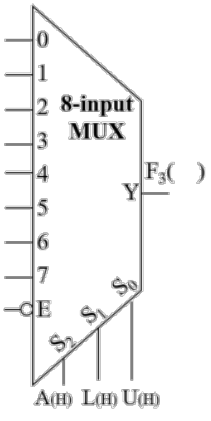
(2%) 3 min b) $\boldsymbol{F_1 = (\bar{U} + T) * B * \overline{(A * \bar{L})}}$ (Note the **NON** tri-state enable.)



(2%) 2 min c) $\boldsymbol{F_2 = (\bar{U} + T) * B * \overline{(A * \bar{L})}}$ (Note the **NON** tri-state enable.)



(3%) 4 min d) $\boldsymbol{F_3 = (\bar{U} + T) * B * \overline{(A * \bar{L})}}$ (Note the **NON** tristate enable.)



[11%] 6. Use the below equation for this problem.

$$Y = \bar{A} * \bar{B} * C * D + A * \bar{B} * D + A * B * \bar{C} + A * B * C * D + A * \bar{C} * D + B * C * \bar{D}$$

(7%) 7 min a) Simplify the above equation and put the result in **MSOP** form and lexical order. Label **ALL** circles.

AB
CD

$\mathbf{Y_{MSOP}}$ =

(3%) 3 min b) If the terms ABCD=0110 and ABCD=1010, i.e., the textbook's d(6) and d(10), are **DON'T CAREs (X)**, determine the new **MPOS** equations, in lexical order. Label **ALL** circles.

AB
CD

$\mathbf{Y_{MPOS}}$ =

(1%) 1 min c) Are the above equations (in parts a and b) **equivalent**? Why or why not?

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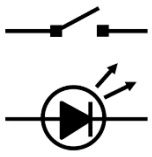
[8%] 7. In this problem, you will design a mixed-logic circuit diagram and some input and output circuits.

(5%) 5 min a) Draw the **mixed-logic circuit** diagram to directly implement these two equations with the **minimum number of <u>real</u> gates**. (Real SSI gates were defined in class as all inputs having the same activation levels.) These should be **circuit diagrams,** not layout diagrams. The B input and X output must be active-high, and Y must be active-low, i.e., B(H), X(H), and Y(L). Choose the optimal (best) activation-level for A.

$$X = A + \bar{B}$$
$$Y = \overline{\bar{A} * B}$$

(3%) 3 min b) Draw the required switch **circuits** and LED **circuits** to complete the circuit design for this problem. (These should be **circuit diagrams, not** layout diagrams.) Draw the switches in their **<u>true</u>** positions. Both a switch and an LED circuit symbol are shown here. (The switch shown is in its open position.) Do **not** draw unnecessary components.



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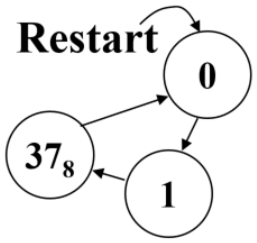
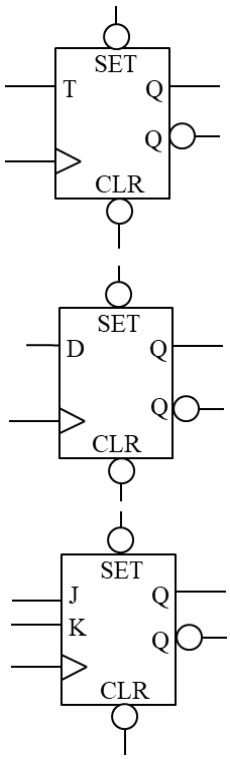
[17%] 3 min 8. Design a system that "counts" as shown, using the minimum number of flip-flops necessary. The system must **asynchronously** go to state "0" when **Restart** (**active-low**) goes true. Use a **T-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and **D-FF**(s) for **any other** bits that you think are necessary. Note that the third state has 6 outputs, corresponding to the octal number $37_8 = 011\ 111_2$; therefore this state machine has six outputs: Y_5, Y_4, …, Y_0. These outputs must be **active-low**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.



(2%) 4 min a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

Inputs

Outputs



5 min (7%) b) Complete the next-state **truth** table (**in counting order**).

(4%) 5 min 8. c) Find the required **simplified** (MSOP or MPOS) equations for this circuit.

(4%) 5 min d) Design the complete circuit, using the T-FF, D-FF(s), and JK-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronously** go to state "**0**" when **Restart** (**active-low**) goes true.

Inputs

Outputs

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[11%] 9. Determine the appropriate equations in **lexical order** for each of the below circuits. Both of these circuits have MUXes with **tri-state** enables. All equations must be in lexical order.

(2%) 3 min a) For Figure 1, if S(L) is **true**, determine the equation for $X = f_a(A,T,R)$, i.e., as a function of A, T, and R.

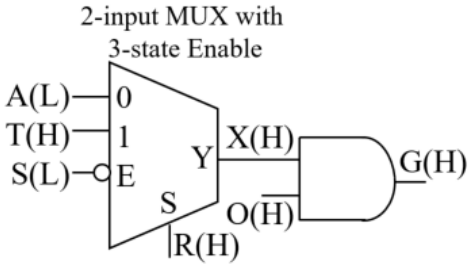

Fig 1: Circuit for parts a) – e).

(0.5%) 1 min b) For Figure 1, if S(L) is **true**, determine the equation for $G = f_b(X,O)$, if S(L) is **true**.

(0.5%) 2 min c) For Figure 1, if S(L) is **true**, determine the equation for $G = f_c(A,T,O,R)$.

(2%) 2 min d) For Figure 1, if S(L) is **false**, determine the equation for $X = f_d(A,T,R)$, i.e., as a function of A, T, and R.

(1%) 2 min e) For Figure 1, determine the equation for $G = f_e(A,T,O,R)$, i.e., as a function of A, T, O, and R, if S(L) is **false**.

(4%) 3 min f) Determine the equation for $X = f_f(\cancel{C},A,T,\cancel{O},R,B,E,S,\cancel{I})$, for the circuit to the right. Hint: First find equations for the top and bottom X's.

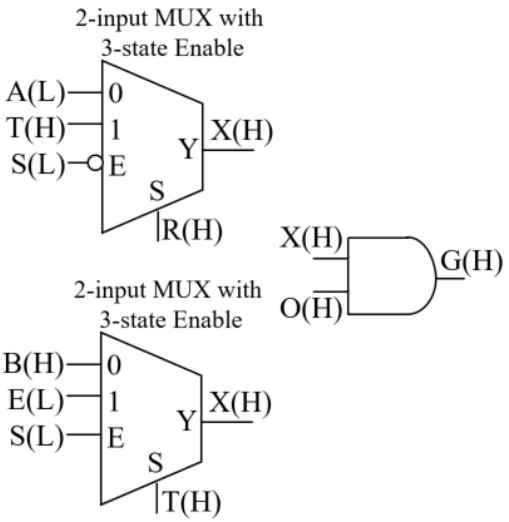

Fig 2: Circuit for parts f) – g).

(1%) 2 min g) Determine the equation for $G = f_g(X,O)$.

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[7%] 5 min

10. Design a 4-input MUX with an **active-low NON-tristate** enable, E(L). Use the **minimum number** of 2-input MUXes and **no other parts** in your design. You may assume that the 2-input MUXes have one or more enables, of any activation-levels that you need. Label the MUX inputs as $\mathbf{X_i(H)}$ and the MUX select lines as $\mathbf{S_j(H)}$, and the output as **Y(H)**.

[6%] 5 min

11. Design a 2-to-4 decoder with an **active-low** enable, E(L). Use the **minimum number** of 1-to-2 decoders and **no other parts** in your design. You may assume that the 1-to-2 decoders have one or more enables, of any activation- levels that you need. Label the decoder inputs as $\mathbf{X_i(H)}$ and the decoder outputs as $\mathbf{Y_j(L)}$.