Exam 1

_____

Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may **not** use any notes, HW, labs, books, or calculators.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *The point values for problems may be changed at prof's discretion.*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *For each mixed-logic circuit design, equations must **not** be used as replacements for circuit elements. Label inputs of **each gate** with the appropriate logic equations.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*

Good Evening!
Welcome!

Good luck &
Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (4 October 2010)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2	10	
3	8	
4	8	
5-6	18	
7	13	
8	14	
9	11	
10	8	
11	10	
TOTAL	100	

Exam 1

_____
Last Name, First Name

[10%] 1. Do the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 3 min

a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 111_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 3 min

b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -111_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 3 min

c) What is $74_{10} - 111_{10}$ in 8-bit 2's complement? You must use binary numbers to derive the solution (not decimal). Remember that you must **show <u>all</u> work.**

$(74_{10} - 111_{10})_{2\text{ 8-bit 2's comp}}$: _____

Exam 1

Last Name, First Name

(3%) 1. d) What is $74_{10} + 111_{10}$ in 8-bit 2's complement? You must use binary numbers to derive and determine the solution (not decimal). Remember that you must **show <u>all</u> work**.

3 min

$(74_{10} + 111_{10})_{2\ 8\text{-bit 2's comp}}$: _____

[2%] 2. Divide the following **unsigned binary** numbers. Only three digits to the right of the binary point are required. The answer should be of the same type (i.e., unsigned binary).

4 min

```
1000 1001 ÷ 1101
```

[3%] 3. Add the following **8-bit 2's complement** numbers. (Show all **carries** and work below.) What is the result in **8-bit 2's complement and in hexadecimal**? What is the result **in decimal?**

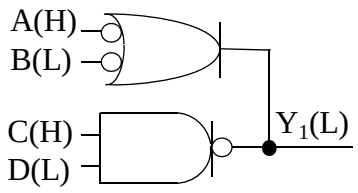
2 min

```
 0100 1001
+1111 1100
```

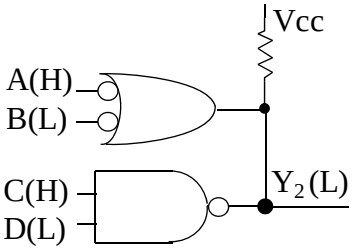
Exam 1

Last Name, First Name

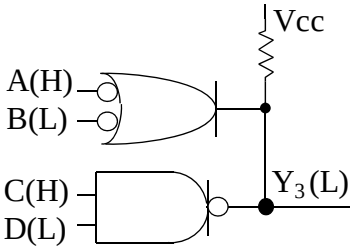
[8%] 8 min 4. Determine the SOP **or** POS equations for the output Y in each of the below circuits. Please **look carefully** at each of the circuits.



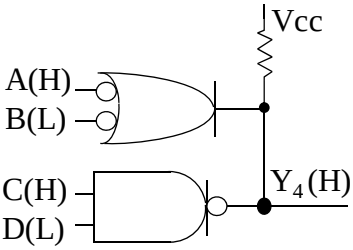
$Y_1 =$ _____



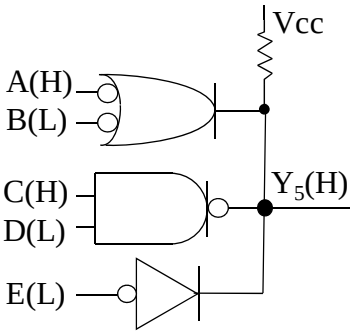
$Y_2 =$ _____



$Y_3 =$ _____



$Y_4 =$ _____



$Y_5 =$ _____

Exam 1

Last Name, First Name

[18%] 5. Design a 1-to-2 decoder with an active-low (**non**-tri-state) enable. **All** other signals should be **active-high**.

(%) 1 min a) Draw a functional block diagram (showing all inputs and outputs) of the required decoder. I suggest you use subscripted variables where appropriate.

1-to-2 decoder Functional Block Diagram

(%) 2 min b) Draw the truth table for this decoder.

(%) 2 min c) Determine the MSOP **or** MPOS equation(s) of this decoder.

(%) 2 min d) Draw the mixed-logic circuit diagram to implement this circuit.

(%) 4 min e) Draw a functional block diagram of a **2-to-4** decoder **WITHOUT** enable. Then design this decoder using **ONLY** 1-to-2 decoders (with active-low enables), if possible. If not possible, use a minimum of **SSI** gates in addition to 1-2 decoders.

Exam 1

Last Name, First Name

(%) 5. f) Draw a functional block diagram of a **2-to-4** decoder **WITH** active-low **enable**. Then design this decoder using 1-to-2 decoders (with active-low enables) and a **minimum** number of SSI gates. (Assume that each SSI gate costs 5¢ and each 1-to-2 decoder cost 10¢ ~~20¢~~.).

4 min

(%) g) Design a 3-to-8 decoder **WITH** active-low enable, using only **2-to-4** decoders **with enables** and a minimum number of SSI gates. (Assume that each SSI gate costs 5¢ and each 2-to-4 decoder cost 20¢ ~~50¢~~.)

4 min

Exam 1

Last Name, First Name

[4%] 6. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

4 min

$$Y = \overline{\overline{A + \overline{B \times \overline{C}} \times \overline{\left(\overline{C} + D\right)}} \times \overline{E + \overline{F + \overline{G}} \times \overline{F}}}$$

Y = /{ /[/(A + /(B*/C)) * /(/C + D)] * /[E + /(F + /G)] * /F }

Y = _____

[9%] 7. Determine the MSOP **and** MPOS equivalent of the below Boolean expression.

6 min

W = (/A + B + /D)*(A+/B+/C+D)*(A+B+/C)*(A+B+C+/D)*(A+/C+/D)

W_{MSOP} = _____

W_{MPOS} = _____

Exam 1

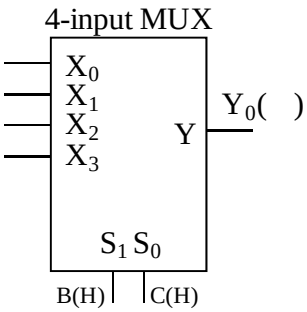
Last Name, First Name

[15%] 8. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The four below problems are independent.)

2 min

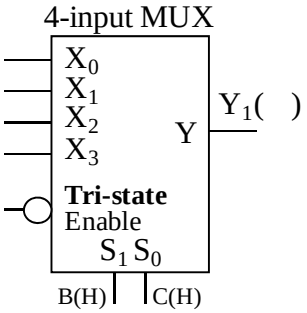
(%) a) **Y_0 = /A*B*/C + /A B C /D**

3 min



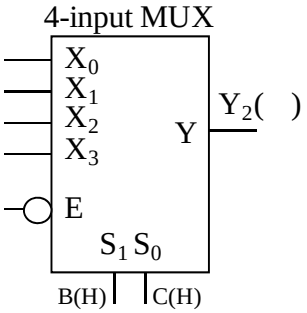
(%) b) **Y_1 = /A*B*/C + /A B C /D** (Note the **tri-state** enable.)

3 min



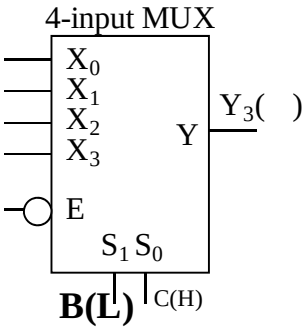
(%) c) **Y_2 = /A*B*/C + /A B C /D** (Note the **NON** tri-state enable.)

3 min



(%) d) **Y_3 = /A*B*/C + /A B C /D** (Note the **NON** tri-state enable.)

3 min



Exam 1

Last Name, First Name

[8%] 5 min

9. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simply the equation!) Use only one type gate, i.e., use as many of the **SAME** chips as needed (but with a minimum number of gates). Use the appropriate mixed-logic symbols. Pick whatever activation levels you want for the inputs and output, except **I** must be **active-high** and O must be **active-low**.

$$Go = \left[\overline{\left(I * \overline{E}\right) + E} + \left(E * \overline{B}\right)\right]\overline{\left(O + \overline{T}\right)}$$

Go = { /[(I*/E) + E] + E*/B }* /(O + /T)

I(H)____

E( )___

____Go( )

B( )___

O(L)___

T( )___

[3%] 4 min

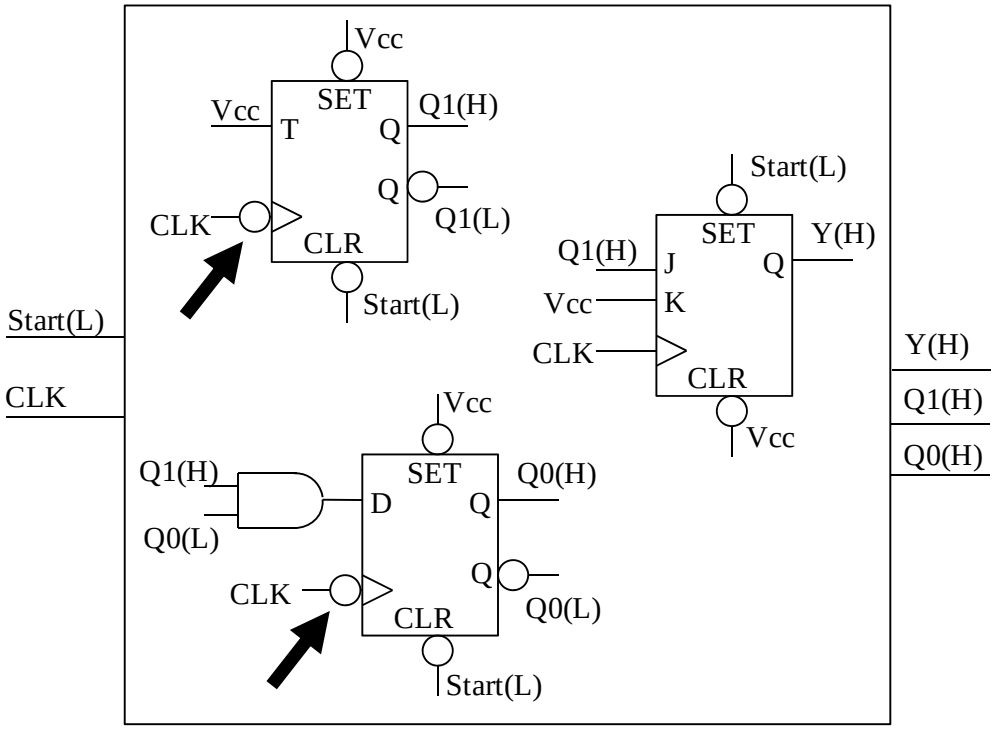
10. Create next-state truth tables for the D-, T- and J-K Flip-Flops. These will help you in the next problem.

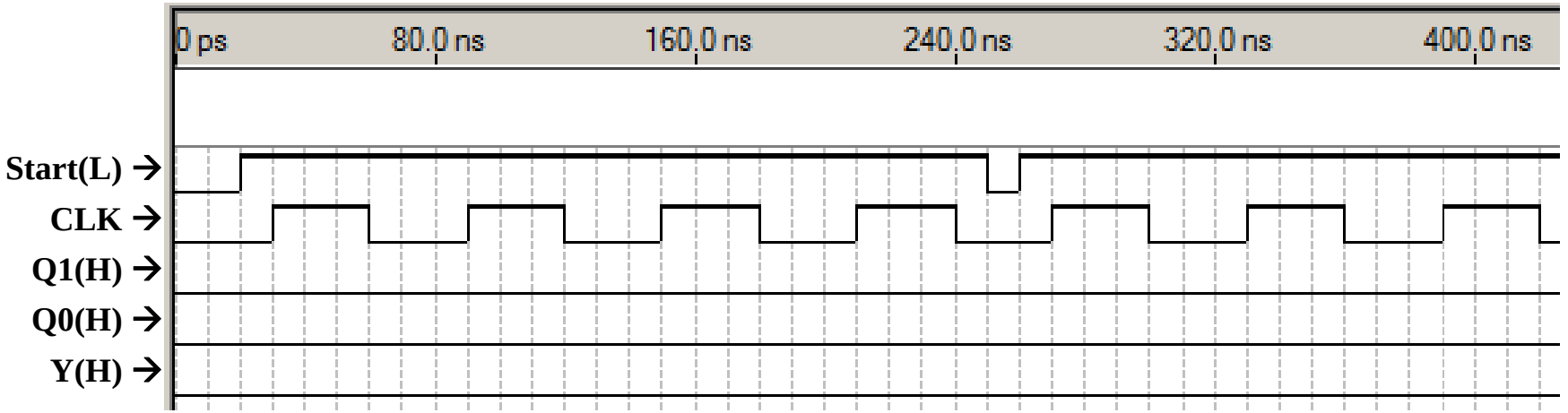
Exam 1

Last Name, First Name

[8%] 11. Complete the timing diagram for the given circuit, i.e., fill in the values of Q1, Q0, and Y. Note that the T-FF and D-FF **both have bubbles** at the CLK input. Assume all propagation delays are 10ns (one grid). All SET and CLR inputs are asynchronous.

9 min

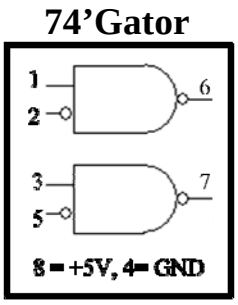




Exam 1

Last Name, First Name

[10%] 12. Use the given drawing of the **8-pin 74'Gator** chip to solve the below problems.



(5%) 4 min

a) Draw the **mixed-logic circuit** diagram to implement the below two equations using parts from the 74'Gator chip shown. Also draw the required switch circuits and LED circuits. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions. A must be **active-high**, i.e., A(H).

X = /A + /B

Y = A * B

(5%) 5 min

b) Now draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. Label the wires for each of the inputs and outputs (A, B, X and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.