Exam 1

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Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good afternoon! Welcome!

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (3 October 2011)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2-3	19	
4	14	
5	9	
6	9	
7	10	
8-10	26	
11	13	
TOTAL	100	

Exam 1

Last Name, First Name

[15%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 3 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 137_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>8-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -137_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 2 min c) Determine the **<u>9-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -137_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

Noticeable

Exam 1

Last Name, First Name

(3%) 1. d) What is 137_{10} - 64_{10} in **9-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

3 min

$(137_{10}\text{-}64_{10})_{2\ 9\text{-bit 2's comp}}$: _____

(2%) e) What is 137_{10} + 137_{10} in **9-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

2 min

$(137_{10}+137_{10})_{2\ 9\text{-bit 2's comp}}$: _____

[4%] 2. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

5 min

$$Subs = \overline{\left[\overline{\left(O * \overline{\overline{N}} * T\right)} * V\right] * \overline{(O + \overline{N})}}$$

Subs = _____

Exam 1

Last Name, First Name

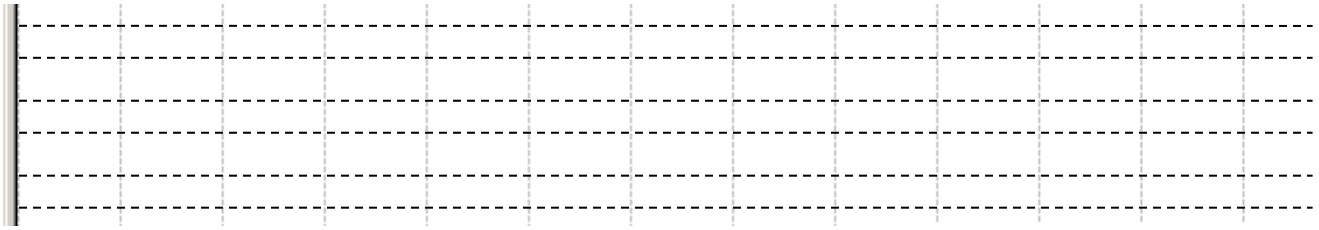
[14%] 3. Answer the following questions.

(3%) 2 min

a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation Y = /(/A + B) with A(H), B(L), Y(H) using the **minimum number** of gates.

(3%) 3 min

b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

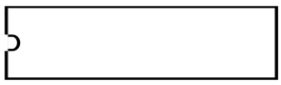


(4%) 2 min

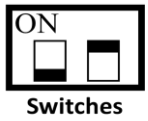
c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(4%) 5 min

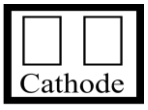
d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want, along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.



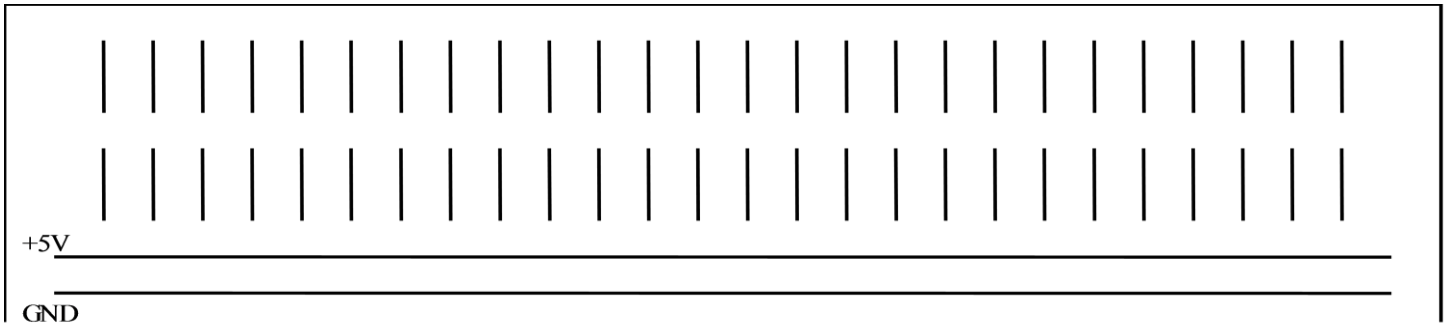
14-pin Chip



Switches



LEDs

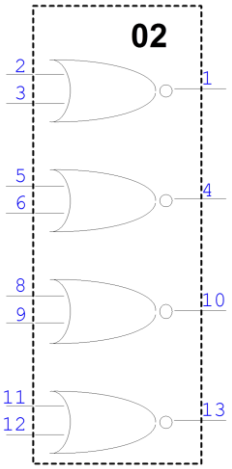


Exam 1

Last Name, First Name

[9%] 5 min

4. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of the 74HC02 (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels. Label the pin **numbers** for your circuit design.



$$Mow = \left[\overline{\overline{(\bar{T} * E)} * A + \overline{(M + \bar{W})}}\right] * (O * \bar{N})$$

T( )___

E( )___

A( )___

M( )___ _____Mow( )

W( )___

O( )___

N( )___

Exam 1

Last Name, First Name

[9%] 5. Use only open-collector gates (of any SSI-type gate) to directly implement the below equation. (Do **NOT** simply the equations.) **Show your work!**

(5%) a) $Y = \overline{(\bar{A} * B)} + (C + \bar{D})$

3 min

(2%) b) $Y = \overline{\overline{(\bar{A} * B)} + (C + \bar{D})}$

2 min

(2%) c) $Y = \overline{\overline{(\bar{A} * B)} + (C + \bar{D})} * E$

2 min

Exam 1

Last Name, First Name

[10%] 6. Use the below equation for this problem.

$$Y = (\bar{A} + \bar{B} + D) * (\bar{A} + B + \bar{C}) * (\bar{A} + B + \bar{D}) * (A + \bar{B} + C + D) * (A + B + \bar{C}) * (A + \bar{C} + D)$$

(7%) 7 min a) Simply the above equation and put the result in MPOS **and** MSOP form. Are the solutions equivalent? Explain why or why not.

AB
CD

AB
CD

Y_{MPOS} =

Y_{MSOP} =

Equivalent?:

(3%) 3 min b) If the term ABCD=0100, i.e., the textbook's d(4), is a **DON'T CARE (X)**, determine the new MPOS and MSOP equations. Are the solutions equivalent? Explain why or why not.

AB
CD

AB
CD

Y_{MPOS} =

Y_{MSOP} =

Equivalent?:

Exam 1

Last Name, First Name

[19%] 7. In this problem you will design several multiplexers (MUX's)

(2%) 3 min

a) Draw a truth table (with wild cards [-] or don't cares [X], if necessary) and a functional block diagram of a 2-input MUX with a **NON**-tristate enable. The inputs should be labeled X and S (for select lines), both with proper subscripts, if necessary, and the enable E. The output should be labeled Y. All signals are active-high except E.

(3%) 2 min

b) Design a 2-input MUX with a **NON**-tristate enable using only SSI devices.

(1%) 2 min

c) Draw a truth table and a functional block diagram of a 2-input MUX with a **tristate** enable. The inputs should be labeled X and S (for select lines), both with proper subscripts, if necessary, and the tristate enable E_{TS}. The output should be labeled Y. All signals are active-high except E_{TS}.

(2%) 2 min

d) Design a 2-input MUX with a **tristate** enable using only SSI devices and a single MSI device, if necessary.

Exam 1

Last Name, First Name

(3%) 7. e) Design a 4-input MUX with an active-low **NON**-tristate enable using **ONLY** 2-input MUX's with **NON**-tristate enables.

4 min

(2%) 7. f) Design a 4-input MUX with an active-low **tristate** enable using **ONLY** 2-input MUX's with **tristate** enables.

4 min

(2%) 7. f) Design a 4-input MUX with **NO** enable using **ONLY** 2-input MUX's with **tristate** enables and SSI components. Assume that each MUX costs 25¢ and each SSI costs 10¢. Minimize the cost of your design.

4 min

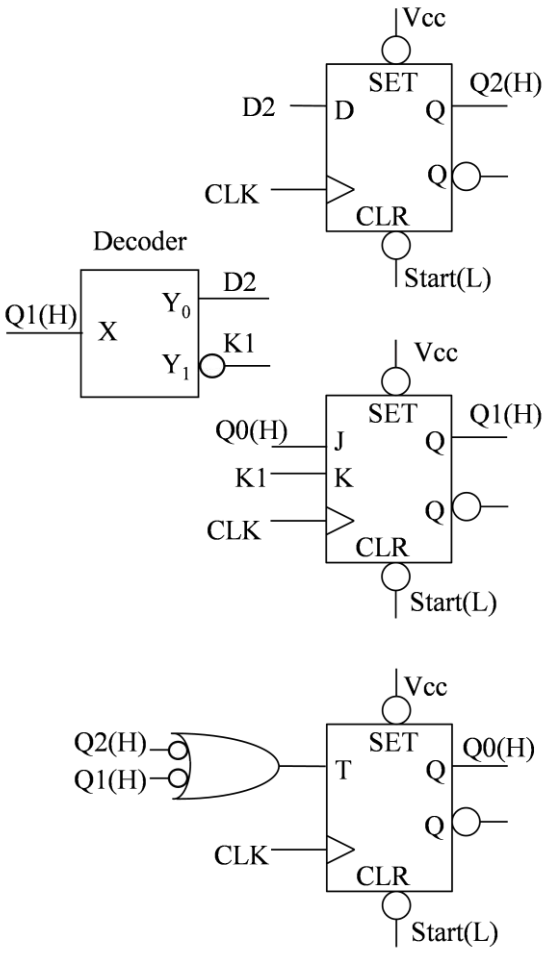
Exam 1

Last Name, First Name

(4%) 6 min 7. g) Design an 8-input MUX with an active-low **tristate** enable using **ONLY** 2-input MUX's, of **either** type previously specified.

[7%] 12 min 8. Consider the below circuit with inputs CLK and Start(L), and active-high outputs Q_2 Q_1 Q_0. Determine the sequence of output Q_2 Q_1 Q_0 for a sequence of 6 clock (CLK) pulses. (The columns to the right are for your use if you need them.) Assume that Start(L) is true to initialize the circuit (for the first row) and then Start(L) is false for the next 6 clock pulses.

#	Q2	Q1	Q0					
0								
1								
2								
3								
4								
5								
6								



Exam 1

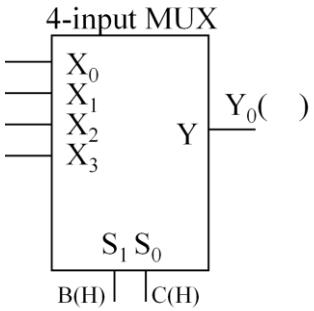
Last Name, First Name

[13%] 9. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The four below problems are independent.)

2 min

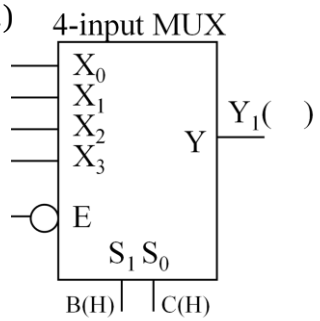
(%) a) **Y_0 = (A+B+/D)*(A+/C)*(B+C)*D**

3 min



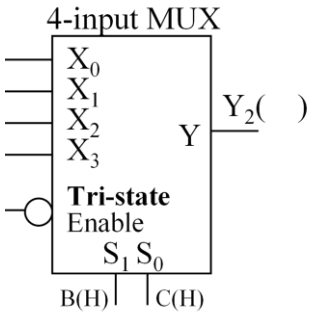
(%) b) **Y_1 = (A+B+/D)*(A+/C)*(B+C)*D** (Note the **NON** tri-state enable.)

3 min



(%) c) **Y_2 = (A+B+/D)*(A+/C)*(B+C)*D** (Note the **tri-state** enable.)

3 min



(%) d) **Y_3 = (A+B+/D)*(A+/C)*(B+C)*D** (Note the **NON** tri-state enable.)

3 min