Exam 1

_____

Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **12** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, **label inputs of each gate** with the **appropriate logic equations** or **NO** partial credit.*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good afternoon! Welcome!

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (4 October 2012)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2-3	18	
4	13	
5	10	
6	8	
7	10	
8	12	
9	6	
10	9	
11	9	
12	5	
TOTAL	100	

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[15%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 3 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 79_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>8-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -79_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 3 min 1. c) What is 42_{10} - 79_{10} in **<u>8-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Remember that you must **show <u>all</u> work.**

$(42_{10}-79_{10})_{2\text{ 8-bit 2's comp}}$: _____

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(2%) 2 min

e) What is 42_{10} + 79_{10} in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

$(42_{10}+79_{10})_{2\ 8\text{-bit 2's comp}}$: _____

(2%) 2 min

f) What is -79_{10} in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

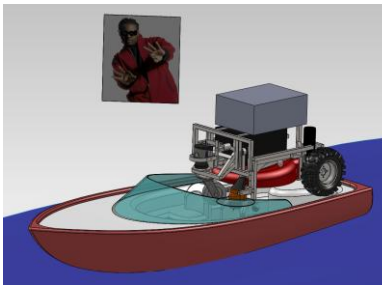
$(-79_{10})_{2\ 10\text{-bit 2's comp}}$: _____

[4%] 5 min

2. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

$$Robo = \left(B\,\bar{O} + \overline{\bar{A}\,T}\right)\overline{[\,(O + \bar{A})\,\overline{(\bar{B} + T)}}$$

Robo = _____



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[13%] 3. Answer the following questions.

(3%) 2 min

a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation Y = /(/A * B) with A(H), B(L), Y(H) using the **minimum number** of gates.

(3%) 3 min

b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

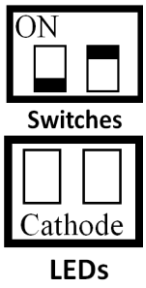
(4%) 2 min

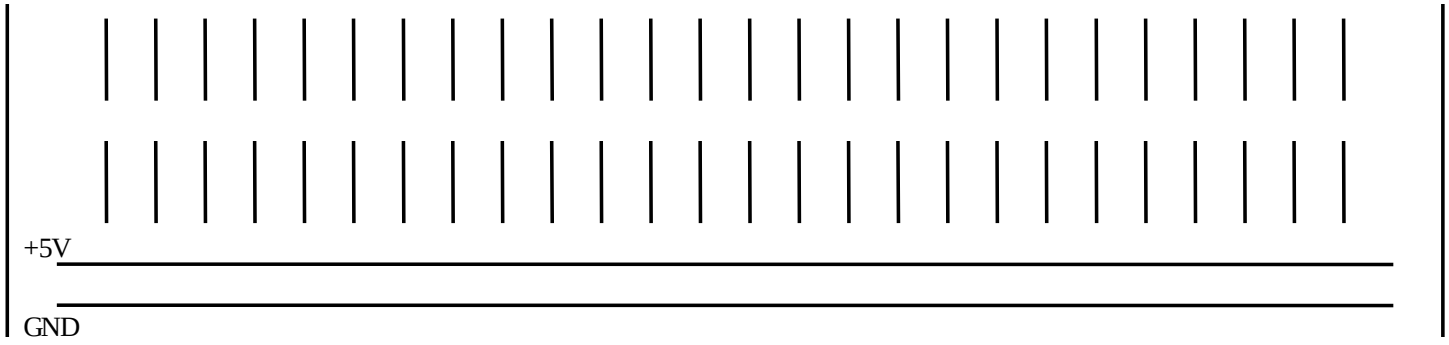
c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(3%) 5 min

d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want, along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.

14-pin Chip





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[10%] 4. Shown is a GAT-OR gate. Note the bubble at one input and the output.

(%) a) Design a level-shifter using the GAT-OR gate for an active-low input X(L), with output X(H).

2 min

(%) b) Design another level-shifter using the GAT-OR gate for an active-high input Y(H), with output Y(L).

2 min

6 min c) Directly implement (i.e., design a circuit to realize) the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only GAT-OR gates (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for signals that are not already specified.

$$B = \left[\left(\overline{\bar{E}A + \bar{T}}\right) + L\right] * \left(\overline{S * \bar{U}}\right)$$

E(H)___

A( )___

T( )___

L(H)___ _____B(H)

S( )___

U(L)___

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8 min

[8%] 5. Answer the following questions about the below circuit. Give MSOP or MPOS equations.

(1%) a) What is the logic equation of E(L) in terms of A and B? E = _____

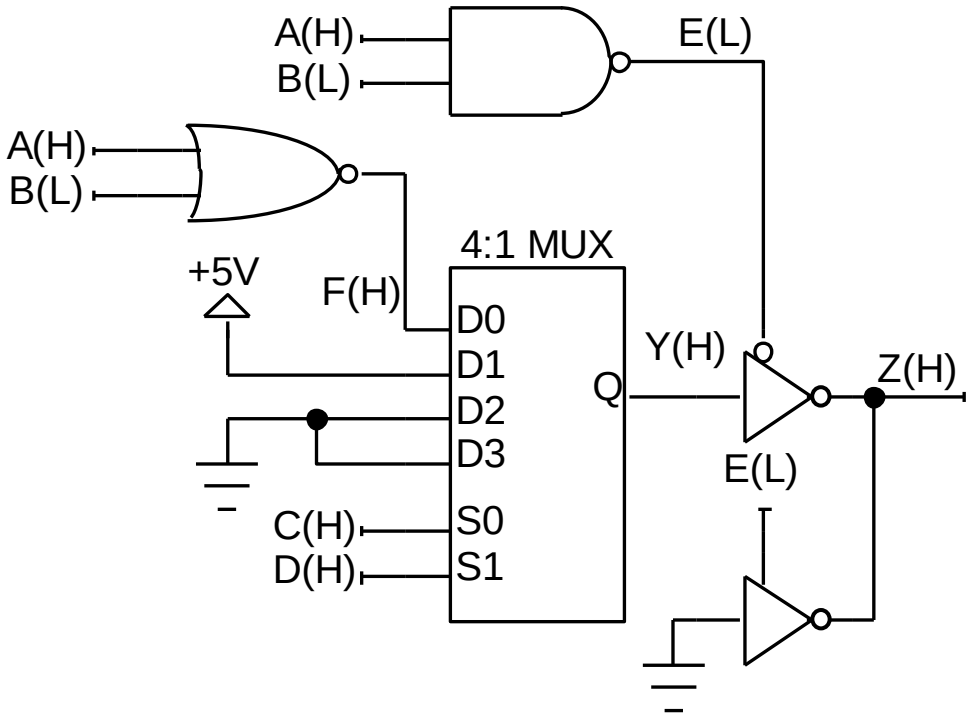
(1%) b) What is the logic equation of F(H) in terms of A and B? F= _____

(3%) c) What is the logic equation of Y(H) in terms of F, C and D?

Ans: Y= _____

(3%) e) What is the logic equation of Z(H) in terms of E and Y?

Ans: Z= _____



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2 min

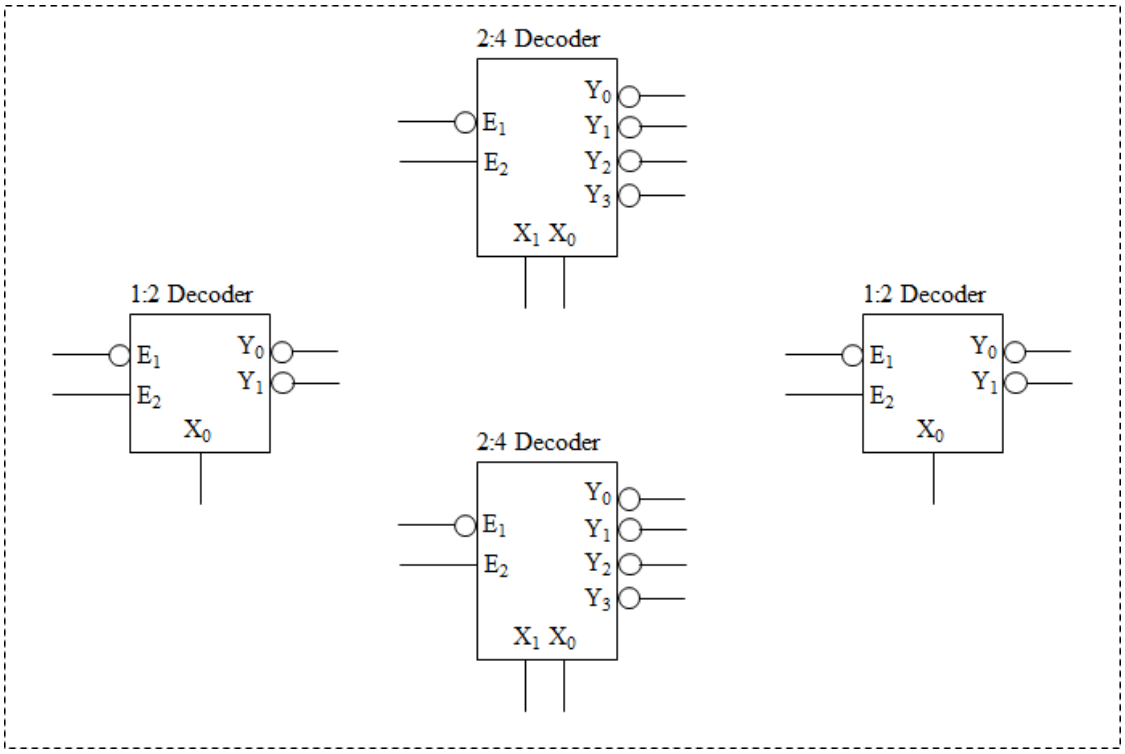
[10%] 6. In this problem you will design a 3-to-8 decoder with a single active-low enable. Two 2-to-4 and two 1-2 decoders, all with two enables, one active-high and one active-low, are shown below.

(%) a) Draw a functional block diagram of a **3-to-8 decoder with a single active-low enable**

2 min

(%) b) Design the **3-to-8 decoder with a single active-low enable** below, using the below parts. (If you can **not** solve it this way, add additional necessary parts.)

8 min



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3 min

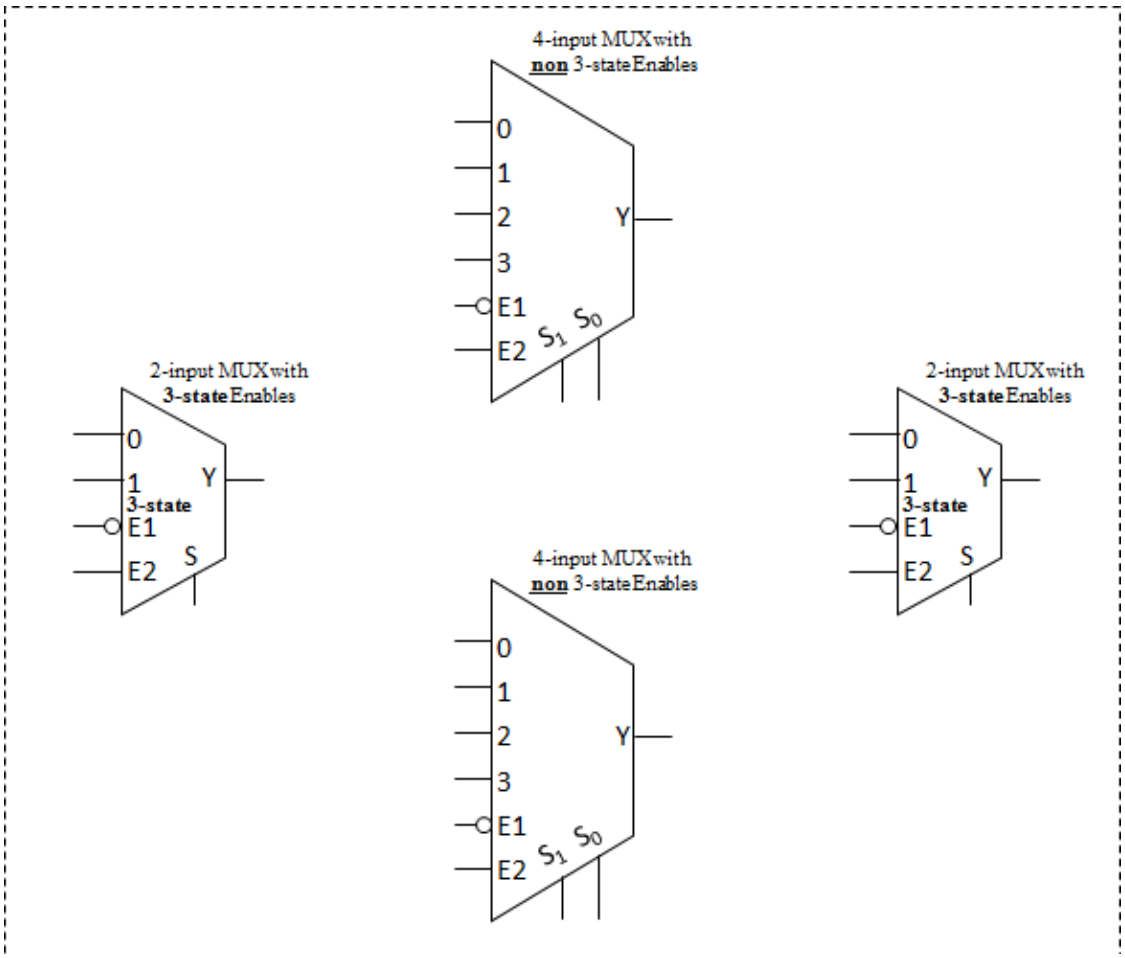
[12%] 7. In this problem you will design an 8-input multiplexer with a single active-low tri-state enable. Two 4-input multiplexers, each with 2 **non tri-state** enables (one active-high and one active-low), are shown below. Two 2-input multiplexers, each with 2 tri-state enables (one active-high and one active-low), are shown.

(%) a) Draw a functional block diagram of an **8-input multiplexer with a single active-low tri-state enable**. All other inputs and outputs are active-high. The inputs are X and S (with subscripts), the output is Y.

2 min

(%) b) Design the **8-input multiplexer with a single active-low tri-state enable** below, using the below parts. (If you can **not** solve it this way, add additional necessary parts.)

9 min



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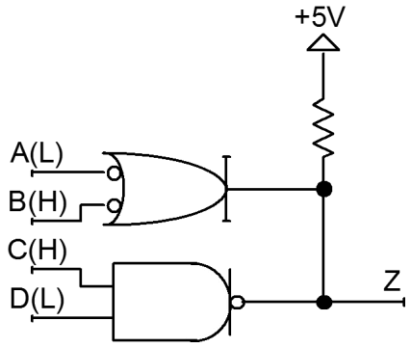
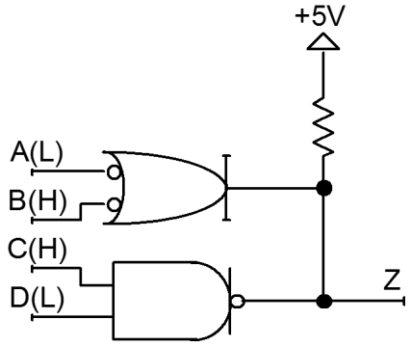
[6%] 8. Analyze this open-collector circuit (drawn twice for your convenience).

(3%) 3 min a) Determine the equation if Z is **active-low**. Give the MSOP **or** MPOS solution (not both).



When Z(L), Z = _____

(3%) 3 min b) Determine the equation if Z is **active-high**. Give the MSOP **or** MPOS solution (not both).



When Z(H), Z = _____

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[9%] 9. Use the K-maps below, find the minimum sum of products (**MSOP**) and minimum product of sum (**MPOS**) solutions. (Use proper lexical ordering.). Label each grouping with the appropriate SOP or POS equation.

(4%) 4 min a) Use these K-maps to find the MSOP (left) and MPOS (right) solution? Label each grouping.

AB \ C	0	1
00	1	0
01	1	X
11	1	0
10	X	1

AB \ C	0	1
00	1	0
01	1	X
11	1	0
10	X	1

Y_{MSOP} = _____

Y_{MPOS} = _____

(0.5%) 1 min b) Are these solutions equivalent? Circle one: YES NO **Why or why not?**

(4%) 4 min c) Use these K-maps to find the MSOP (left) and MPOS (right) solution? Label each grouping.

AB \ C	0	1
00	1	1
01	0	1
11	1	0
10	1	X

AB \ C	0	1
00	1	1
01	0	1
11	1	0
10	1	X

Y_{MSOP} = _____

Y_{MPOS} = _____

(0.5%) 1 min d) Are these solutions equivalent? Circle one: YES NO **Why or why not?**

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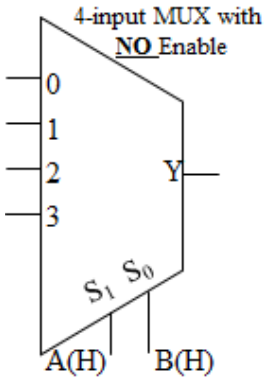
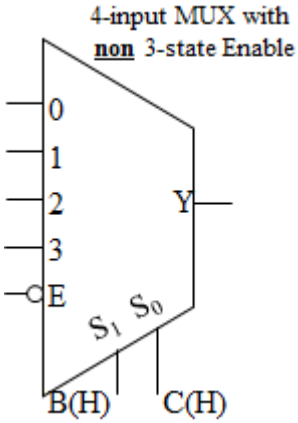
[9%] 10. Use the given 4-input multiplexers to solve each of the below problems. Choose a **single** activation level for each of the inputs and outputs for each problem. Use the **minimum** number of additional components. Show all work.

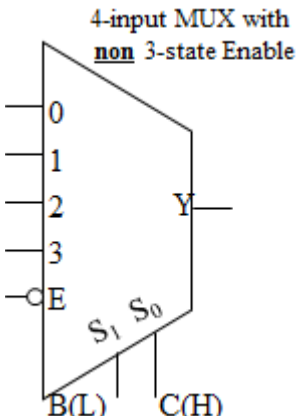
(3%) 3 min a) $Z_0 = A*B + A*C*/D$



(3%) 3 min b) $Z_1 = A*B + A*C*/D$ (Notice the **NON** tri-state enable available on this MUX.)



(3%) 3 min c) $Z_2 = A*B + A*C*/D$ (Notice the **NON** tri-state enable available on this MUX.)



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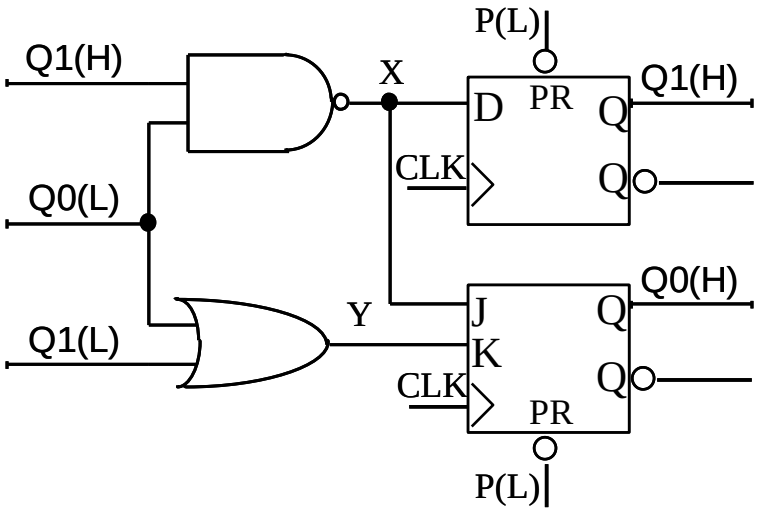
[5%] 11. Use the below circuit to answer the following questions. PR stands for PreSet (i.e., set). The preset is asynchronous.

8 min



Complete the voltage table (using **H** and **L** only) for the following circuit. For both flip-flops, the Preset input has priority over all other inputs and is asynchronous. The symbol ↑ means rising edge of the clock signal. (Note: Do **not** use 0 and 1 in the table. Use **H** and **L**!)

CLK	P(L)	Q_1(H)	Q_0(H)	X	Y	Q_1^+	Q_0^+
↑	L	L	L				
↑	L	L	H				
↑	L	H	L				
↑	L	H	H				
↑	H	L	L				
↑	H	L	H				
↑	H	H	L				
↑	H	H	H				