Instructions:

• Turn off all cell phones, beepers and other noise making devices.
• Show all work on the front of the test papers. Box each answer. If you need more room, make a clearly indicated note on the front of the page, “MORE ON BACK”, and use the back. The back of the page will not be graded without an indication on the front.
• This exam counts for 20% of your total grade.
• Read each question carefully and follow the instructions.
• You may not use any notes, HW, labs, other books, or calculators.
• The point values for problems may be changed at prof’s discretion.
• You must pledge and sign this page in order for a grade to be assigned.
• Put your name at the top of this test page (and, if you remove the staple, all others). Be sure your exam consists of 12 distinct pages. Sign your name and add the date below.
• For each circuit design, equations must not be used as replacements for circuit elements.
• For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations or NO partial credit.
• Truth tables and voltage tables must be in counting order.
• Label the inputs and outputs of each circuit with activation-levels.
• Boolean expression answers must be in lexical order, (i.e., /A before A, A before B, & D_3 before D_2).
• For K-maps, label each grouping with the appropriate equation.

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME
DATE (4 October 2012)

Regrade comments below: Give page # and problem # and reason for the petition.

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1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

   (4%) a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 79<sub>10</sub>.

   Binary: ____________________  
   Octal: ____________________  
   Hex: _____________________  
   BCD: _____________________  

   (3%) b) Determine the 8-bit signed magnitude, 1’s complement, and 2’s complement representations of the decimal number -79<sub>10</sub>.

   Signed Mag: ________________  
   1’s Comp: ________________  
   2’s Comp: ________________  

   (3%) c) What is 42<sub>10</sub> - 79<sub>10</sub> in 8-bit 2’s complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work**.

   \[(42_{10} - 79_{10})_{2} 8\text{-bit 2’s comp}: \] ________________
(2%) e) What is \(42_{10} + 79_{10}\) in \textbf{8-bit} 2’s complement? You must use binary numbers to \textit{derive} and determine the solution (not decimal). Remember that you must \textit{show all work}.

\[
(42_{10} + 79_{10})_8 \text{ bit 2’s comp:}
\]

(2%) f) What is \(-79_{10}\) in \textbf{10-bit} 2’s complement? You must use binary numbers to \textit{derive} and determine the solution (not decimal). Remember that you must \textit{show all work}.

\[
(-79_{10})_8 \text{ bit 2’s comp:}
\]

[4%] 2. Find the MSOP or MPOS equivalent of the below Boolean expression. Show \textit{ALL} work.

\[
Robo = (B \quad \overline{O} + \quad \overline{A} \quad T) \quad [ \quad (O + \quad \overline{A}) \quad (\overline{B} + \quad T) \quad ]
\]

Robo =  

____________________________

Last Name, First Name
3. Answer the following questions.

(a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation \( Y = / (/A \ast B) \) with \( A(H) \), \( B(L) \), \( Y(H) \) using the minimum number of gates.

(b) Draw a complete timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

(c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be circuit diagrams, not layout diagrams.) Draw the switches in their true positions.

(d) Draw a layout of the entire above circuit including each of the switch and LED circuits for part c and the logic from part a. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don’t know what chip you used, so assume whatever pin numbers you want, along with the normal power and ground pins. Label the pin numbers in part a. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you use labels to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch’s closure state. Draw the switches in their true positions.
4. Shown is a GAT-OR gate. Note the bubble at one input and the output.

(a) Design a level-shifter using the GAT-OR gate for an active-low input X(L), with output X(H).

(b) Design another level-shifter using the GAT-OR gate for an active-high input Y(H), with output Y(L).

c) Directly implement (i.e., design a circuit to realize) the below equation with a mixed-logic circuit diagram. (Do NOT simplify the equation.) Use only GAT-OR gates (or their mixed-logic equivalents). Use the minimum number of gates required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for signals that are not already specified.

\[ B = \left( \left( \overline{E}A + \overline{T} \right) + L \right) \ast \left( \overline{S} \ast \overline{U} \right) \]

E(H)___

A(  )___

T(  )___

L(H)___

_______B(H)

S(  )___

U(L)___
5. Answer the following questions about the below circuit. Give MSOP or MPOS equations.

(1%) a) What is the logic equation of \( E(L) \) in terms of \( A \) and \( B \)?
\[ E = \]

(1%) b) What is the logic equation of \( F(H) \) in terms of \( A \) and \( B \)?
\[ F = \]

(3%) c) What is the logic equation of \( Y(H) \) in terms of \( F, C \) and \( D \)?
Ans: \[ Y = \]

(3%) e) What is the logic equation of \( Z(H) \) in terms of \( E \) and \( Y \)?
Ans: \[ Z = \]
6. In this problem you will design a 3-to-8 decoder with a single active-low enable. Two 2-to-4 and two 1-2 decoders, all with two enables, one active-high and one active-low, are shown below.

(a) Draw a functional block diagram of a 3-to-8 decoder with a single active-low enable

(b) Design the 3-to-8 decoder with a single active-low enable below, using the below parts. (If you can not solve it this way, add additional necessary parts.)
7. In this problem you will design an 8-input multiplexer with a single active-low tri-state enable. Two 4-input multiplexers, each with 2 non tri-state enables (one active-high and one active-low), are shown below. Two 2-input multiplexers, each with 2 tri-state enables (one active-high and one active-low), are shown.

a) Draw a functional block diagram of an 8-input multiplexer with a single active-low tri-state enable. All other inputs and outputs are active-high. The inputs are X and S (with subscripts), the output is Y.

b) Design the 8-input multiplexer with a single active-low tri-state enable below, using the below parts. (If you can not solve it this way, add additional necessary parts.)
8. Analyze this open-collector circuit (drawn twice for your convenience).

\[ (3\%) \quad a) \quad \text{Determine the equation if } Z \text{ is active-low. Give the MSOP or MPOS solution (not both).} \]

\[ \text{When } Z(L), Z = \quad \text{____} \]

\[ (3\%) \quad b) \quad \text{Determine the equation if } Z \text{ is active-high. Give the MSOP or MPOS solution (not both).} \]

\[ \text{When } Z(H), Z = \quad \text{____} \]
9. Use the K-maps below, find the minimum sum of products (MSOP) and minimum product of sum (MPOS) solutions. (Use proper lexical ordering.). Label each grouping with the appropriate SOP or POS equation.

a) Use these K-maps to find the MSOP (left) and MPOS (right) solution? Label each grouping.

\[
\begin{array}{c|cc}
\text{C} & 0 & 1 \\
\hline
\text{AB} & 00 & 01 \\
00 & 1 & 0 \\
01 & 1 & X \\
11 & 1 & 0 \\
10 & X & 1 \\
\end{array}
\]

\[
\begin{array}{c|cc}
\text{C} & 0 & 1 \\
\hline
\text{AB} & 00 & 01 \\
00 & 1 & 0 \\
01 & 1 & X \\
11 & 1 & 0 \\
10 & X & 1 \\
\end{array}
\]

\[Y_{\text{MSOP}} = \text{__________}\]

\[Y_{\text{MPOS}} = \text{__________}\]

b) Are these solutions equivalent? Circle one: YES NO Why or why not?

(4%) c) Use these K-maps to find the MSOP (left) and MPOS (right) solution? Label each grouping.

\[
\begin{array}{c|cc}
\text{C} & 0 & 1 \\
\hline
\text{AB} & 00 & 01 \\
00 & 1 & 1 \\
01 & 0 & 1 \\
11 & 1 & 0 \\
10 & 1 & X \\
\end{array}
\]

\[
\begin{array}{c|cc}
\text{C} & 0 & 1 \\
\hline
\text{AB} & 00 & 01 \\
00 & 1 & 1 \\
01 & 0 & 1 \\
11 & 1 & 0 \\
10 & 1 & X \\
\end{array}
\]

\[Y_{\text{MSOP}} = \text{__________}\]

\[Y_{\text{MPOS}} = \text{__________}\]

(0.5%) d) Are these solutions equivalent? Circle one: YES NO Why or why not?

1 min
10. Use the given 4-input multiplexers to solve each of the below problems. Choose a single activation level for each of the inputs and outputs for each problem. Use the minimum number of additional components. Show all work.

(3%) a) \( Z_0 = A \cdot B + A \cdot C/D \)

(3%) b) \( Z_1 = A \cdot B + A \cdot C/D \) (Notice the NON tri-state enable available on this MUX.)

(3%) c) \( Z_2 = A \cdot B + A \cdot C/D \) (Notice the NON tri-state enable available on this MUX.)
11. Use the below circuit to answer the following questions. PR stands for PreSet (i.e., set). The preset is asynchronous.

Complete the voltage table (using H and L only) for the following circuit. For both flip-flops, the Preset input has priority over all other inputs and is asynchronous. The symbol ↑ means rising edge of the clock signal. (Note: Do not use 0 and 1 in the table. Use H and L!)

<table>
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<th>CLK</th>
<th>P(L)</th>
<th>Q1(H)</th>
<th>Q0(H)</th>
<th>X</th>
<th>Y</th>
<th>Q1↑</th>
<th>Q0↑</th>
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<tr>
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<td>L</td>
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