Exam 1

Last Name, First Name

CongreGators: UF MIL's Swarm Robots.

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (8 Oct 2013) _____

Regrade comments below: Give page # and problem # and reason for the petition.

Pages	Available	Points
2-3	19	
4	13	
5	7	
6	11	
7	10	
8	11	
9	11	
10	12	
11	6	
TOTAL	100	

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[15%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 287_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 3 min b) Determine the **<u>10-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -287_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $-256_{10} - 287_{10}$ in **<u>10-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). You must **show <u>all</u> work.**

$(-256_{10} - 283_{10})_{2\ 10\text{-bit 2's comp}}$: _____

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(2%) 1. d) What is $384_{10} - 287_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

4 min

$(384_{10} - 283_{10})_{2\text{ 10-bit 2's comp}}$: _____

(4%) 1. e) Perform the requested operations in binary. If necessary,

4 min

```
  10 0101
×    101
```

```
10 0101 ÷ 101
```
(Show 3 digits after the binary point)

[4%] 2. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

5 min

$$Beat = \overline{\left[\overline{L * \bar{S}} * U\right]} + \overline{\left[\overline{(\bar{L} + S)} * U\right]}$$

Beat = _____

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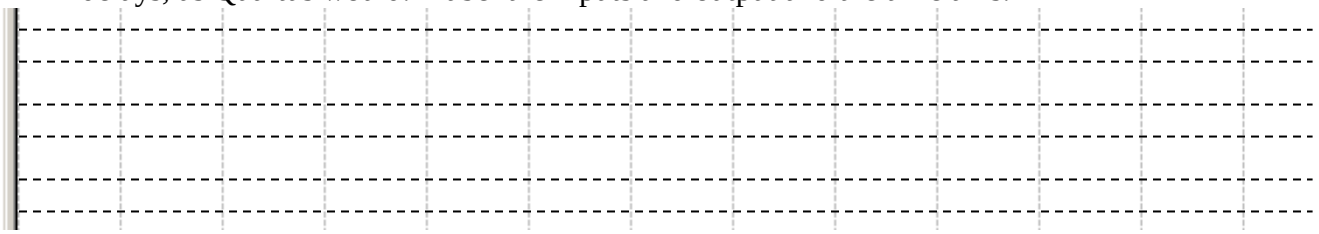
[13%] 3. Answer the following questions.

(3%) 2 min

a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation Y = (/A * B) with A(H), B(L), Y(L) using the **minimum number** of gates.

(3%) 3 min

b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

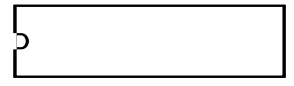


(4%) 2 min

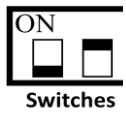
c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(3%) 5 min

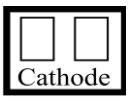
d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part d** and the logic from **part b**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part b**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.



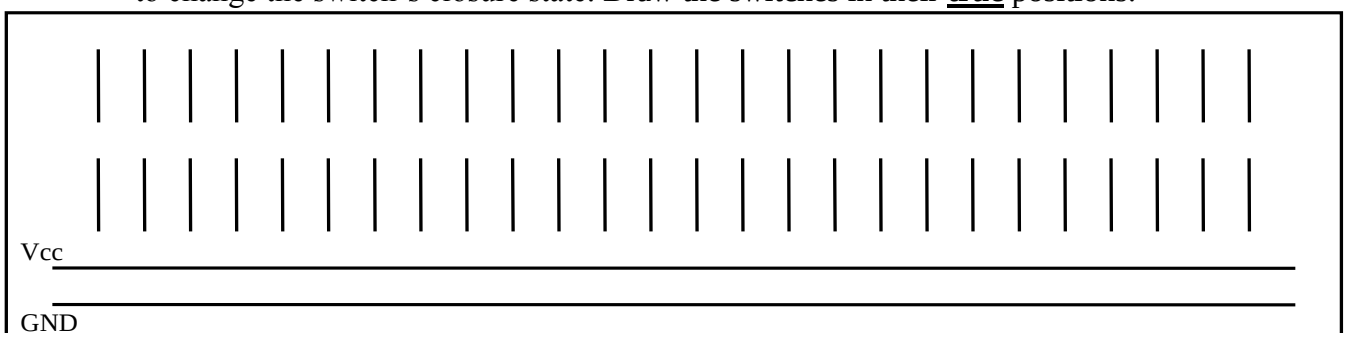
14-pin Chip



Switches



LEDs



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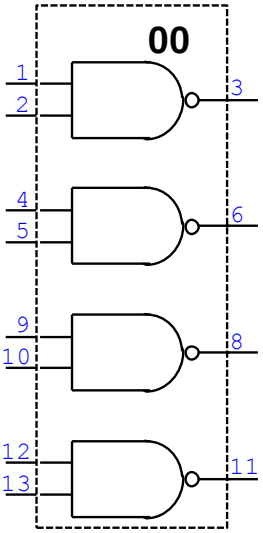
[7%] 5 min

4. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of the 74HC00 (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for all signals . Label the parts and pin **numbers** for your circuit design.



$$Congr = \overline{(A + \bar{G}) * \left\{\left[A * \overline{(T * \bar{O})}\right] + R * \bar{S}\right\}}$$

A( )

G( )___

T( )___ __Congr( )

O( )___

R( )___

S( )___

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[6%] 5. Use only open-collector gates (of any **real** SSI-type gate) to directly implement the below equation. (Do **NOT** simply the equations.) **Show your work!**

(3%) a) $G = (\bar{O} * U) + \bar{F}$, with **O(H)** required.

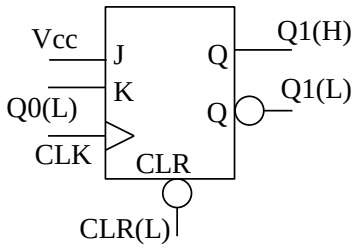
3 min

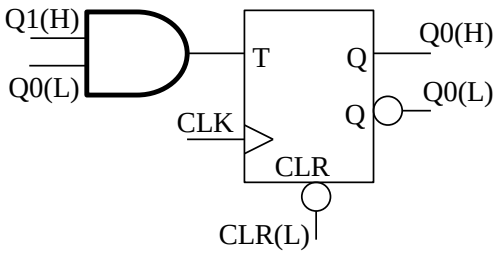
(3%) b) $G = (O + \bar{U}) * F$, with **O(H)** required.

3 min

[5%] 6. Determine the sequence of outputs, for Q_1(H) and Q_0(H), starting at Q_1Q_0=00. Assume the asynchronous clear, CLR(L), is false and a series of clocks (CLK) occur to create the sequence of outputs. Show **ALL** work. List the next 6 values in the sequence.

5 min





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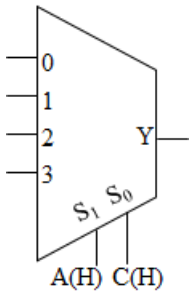
[10%] 7. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The four below problems are **independent**.)

2 min

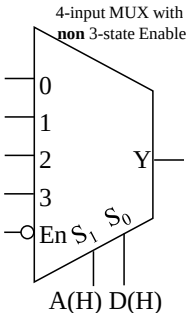
3 min

(3%) a) $\mathbf{Y_0 = A*/B + /B*/C*D + /B*C*D}$



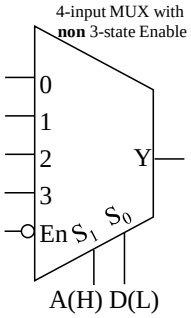
3 min

(3%) b) $\mathbf{Y_1 = A*/B + /B*/C*D + /B*C*D}$ (Note the **enable**.)



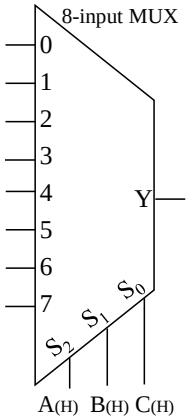
3 min

(2%) c) $\mathbf{Y_2 = A*/B + /B*/C*D + /B*C*D}$ (Note the **enable** and **D(L)**.)



(2%) d) $\mathbf{Y_3 = A*/B + /B*/C*D + /B*C*D}$ (Note the mux **size**)

3 min



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[11%] 8. Solve the following Karnaugh Map Boolean Algebraic simplifications problems.

(6%) a) Simply the below equation and put the result in MSOP **and** form MPOS.

5 min

AB \ CD	00	01	11	10
00	1	1	0	1
01	0	0	1	1
11	1	0	1	1
10	1	1	0	1

AB \ CD	00	01	11	10
00	1	1	0	1
01	0	0	1	1
11	1	0	1	1
10	1	1	0	1

Y_{MSOP} =

Y_{MPOS} =

(5%) b) If the terms ABCD=0001, 1001, and 1011, i.e., the textbook's d(1,9,11), are **DON'T CAREs (X)**, determine the new MSOP **and** MPOS equations. Are the two **below** solutions equivalent? Explain why or why not.

5 min

AB \ CD	00	01	11	10
00	1	X	0	1
01	0	0	1	1
11	1	0	1	1
10	1	X	X	1

AB \ CD	00	01	11	10
00	1	X	0	1
01	0	0	1	1
11	1	0	1	1
10	1	X	X	1

Y_{MSOP} =

Y_{MPOS} =

Are the above equations **Equivalent**? Why or why not?

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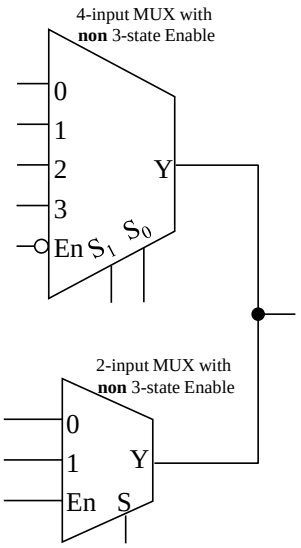
[11%] 9. Describe the function of two below circuits in parts a and b. Fill in appropriate mixed-logic signal names to clarify your description, to make the circuits mixed-logic circuit diagrams, and to complete the intended design.

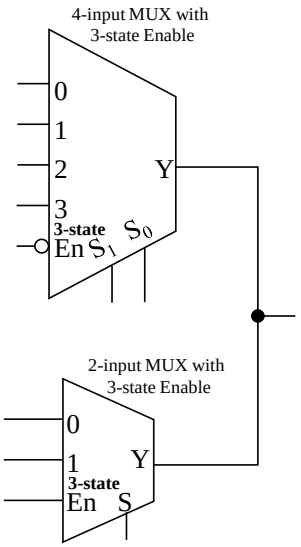
(4%) a) The enables in this problem are **NOT** 3-state.

4 min



(4%) b) The enables in this problem **ARE** 3-state.

4 min



(3%) c) If adding an overall system enable on either the above circuits makes sense, then add (in a box or boxes **above**) SSI circuit(s) to create a system enable of the same type as the MUXes of the given problem (i.e., non 3-state or 3-state).

3 min

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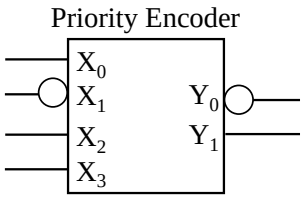
[12%] 10. In this problem you will design several decoders.

(4%) 5 min

a) Determine the truth table for the below **priority** encoder (where a higher subscript has a higher priority)? Also create a **functional** block diagram from the given block diagram.



(4%) 6 min

b) Determine the equations for the encoder (use space above). Simplify the equations. Design a circuit (use space below) to implement this design. Use only SSI gates.

(4%) 3 min

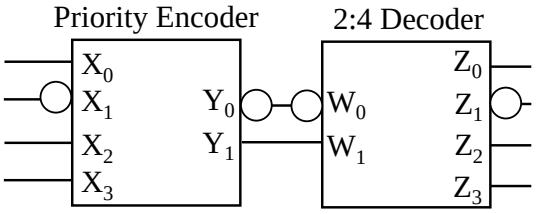
c) Which (if any) of the Z_i outputs are **true** for each of the following? Choose the normal (matching) activation-levels for the inputs and outputs (as you did in your MSI labs).

1) $X_3X_2X_1X_0 = 0001$

2) $X_3X_2X_1X_0 = 0000$

3) $X_3X_2X_1X_0 = 1000$

4) $X_3X_2X_1X_0 = 1011$



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[6%] 11. Complete the timing diagram for the below JK-Flip flop with **asynchronous clear** and **synchronous set**.

7 min