Instructions:
- **Turn off all cell phones and other noise making devices and put away all electronics.**
- **Show all work on the front of the test papers. Box each answer.** If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.
- This exam counts for 20% of your total grade.
- Read each question **carefully** and **follow the instructions**.
- You may **not** use any notes, HW, labs, other books, or calculators.
- The point values for problems may be changed at prof’s discretion.
- You must pledge and sign this page in order for a grade to be assigned.
- Put your name at the top of this test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below.
- For each circuit design, equations must **not** be used as replacements for circuit elements.
- For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations.
- Truth tables and voltage tables must be in **counting** order.
- Label the inputs and outputs of each circuit with activation-levels.
- Boolean expression answers must be in **lexical order** (i.e., /A before A, A before B, & D3 before D2).
- For K-maps, label each grouping with the appropriate equation.

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

Please read carefully.

Good luck & Go Gators!!!
1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number \(287_{10}\).

- **Binary:** 
- **Octal:** 
- **Hex:** 
- **BCD:**

(b) Determine the 10-bit signed magnitude, 1’s complement, and 2’s complement representations of the decimal number \(-287_{10}\).

- **Signed Mag:** 
- **1’s Comp:** 
- **2’s Comp:**

(c) What is \(-256_{10} - 287_{10}\) in 10-bit 2’s complement? You must use binary numbers to **derive** and determine the solution (not decimal). You must **show all work.**

\((-256_{10} - 283_{10})_{2\text{-bit \text{2’s comp}}} = \) 

\(\)
(2%) 1. d) What is $384_{10} - 287_{10}$ in 10-bit 2’s complement? You must use binary numbers to derive and determine the solution (not decimal). Remember that you must show all work.

$$(384_{10} - 283_{10})_{2}$$. 10-bit 2’s comp: ___________________________

(4%) 1. e) Perform the requested operations in binary. If necessary,

$$
\begin{align*}
10 \ 0101 & \div 101 \\
\times \ 101 & \\
\end{align*}
$$

(Show 3 digits after the binary point)

[4%] 2. Find the MSOP or MPOS equivalent of the below Boolean expression. Show ALL work.

$$Beat = [L \overline{S} U] + [(\overline{L} + S) U]$$

Beat = ___________________________
3. Answer the following questions.

(a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation $Y = (\bar{A} \cdot B)$ with $A(H)$, $B(L)$, $Y(L)$ using the minimum number of gates.

(b) Draw a complete timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

(c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be circuit diagrams, not layout diagrams.) Draw the switches in their true positions.

(d) Draw a layout of the entire above circuit including each of the switch and LED circuits for part d and the logic from part b. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don’t know what chip you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the normal power and ground pins. Label the pin numbers in part b. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you use labels to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch’s closure state. Draw the switches in their true positions.
[7%] 4. Directly implement the below equation with a mixed-logic circuit diagram. (Do NOT simplify the equation.) Use only gates of the 74HC00 (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for all signals. Label the parts and pin numbers for your circuit design.

\[
Congr = (A + \overline{G}) \cdot \left\{ A \cdot (T \cdot \overline{O}) + R \cdot \overline{S} \right\}
\]

A(  )

G(  )

T(  )

O(  )

R(  )

S(  )

____Congr(  )
5. Use only open-collector gates (of any \textbf{real} SSI-type gate) to directly implement the below equation. (Do \textbf{NOT} simply the equations.) \textbf{Show your work!}

\[(3\%) \ a) \ G = (\overline{O} \ast U) + \overline{F}, \text{ with } O(H) \text{ required.} \]

\[(3\%) \ b) \ G = (O + \overline{U}) \ast F, \text{ with } O(H) \text{ required.} \]

6. Determine the sequence of outputs, for \(Q_1(H)\) and \(Q_0(H)\), starting at \(Q_1Q_0=00\). Assume the asynchronous clear, CLR(L), is false and a series of clocks (CLK) occur to create the sequence of outputs. \textbf{Show ALL work. List the next 6 values in the sequence.}
7. Use the given multiplexers to design mixed-logic circuit diagrams that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to minimize the number of additional parts required. Use the minimum number of additional SSI gates. Show all work. (The four below problems are independent.)

(a) \( Y_0 = \overline{A} \cdot \overline{B} + \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot C \cdot D \)

(b) \( Y_1 = \overline{A} \cdot \overline{B} + \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot C \cdot D \) (Note the enable.)

(c) \( Y_2 = \overline{A} \cdot \overline{B} + \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot C \cdot D \) (Note the enable and \( D(L) \).)

(d) \( Y_3 = \overline{A} \cdot \overline{B} + \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot C \cdot D \) (Note the mux size)
8. Solve the following Karnaugh Map Boolean Algebraic simplifications problems.

(a) Simply the below equation and put the result in MSOP and form MPOS.

\[
\begin{array}{c|cccc}
  CD & 00 & 01 & 11 & 10 \\
  \hline
  AB & 00 & 01 & 11 & 10 \\
  00 & 1 & 1 & 0 & 1 \\
  01 & 0 & 0 & 1 & 1 \\
  11 & 1 & 0 & 1 & 1 \\
  10 & 1 & 1 & 0 & 1 \\
\end{array}
\]

\[Y_{\text{MSOP}} = \quad Y_{\text{MPOS}} =\]

(b) If the terms \(ABCD=0001, 1001,\) and \(1011,\) i.e., the textbook’s \(d(1,9,11),\) are DON’T CAREs \((X),\) determine the new MSOP and MPOS equations. Are the two below solutions equivalent? Explain why or why not.

\[
\begin{array}{c|cccc}
  CD & 00 & 01 & 11 & 10 \\
  \hline
  AB & 00 & 01 & 11 & 10 \\
  00 & 1 & \times & 0 & 1 \\
  01 & 0 & 0 & 1 & 1 \\
  11 & 1 & 0 & 1 & 1 \\
  10 & 1 & \times & \times & 1 \\
\end{array}
\]

\[Y_{\text{MSOP}} = \quad Y_{\text{MPOS}} =\]

Are the above equations Equivalent? Why or why not?
9. Describe the function of two below circuits in parts a and b. Fill in appropriate mixed-logic signal names to clarify your description, to make the circuits mixed-logic circuit diagrams, and to complete the intended design.

a) The enables in this problem are **NOT** 3-state.

b) The enables in this problem **ARE** 3-state.

c) If adding an overall system enable on either the above circuits makes sense, then add (in a box or boxes above) SSI circuit(s) to create a system enable of the same type as the MUXes of the given problem (i.e., non 3-state or 3-state).
10. In this problem you will design several decoders.

(4%) a) Determine the truth table for the below priority encoder (where a higher subscript has a higher priority)? Also create a functional block diagram from the given block diagram.

```
<table>
<thead>
<tr>
<th>X0</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>Y0</th>
<th>Y1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

```
Priority Encoder
```

(4%) b) Determine the equations for the encoder (use space above). Simplify the equations. Design a circuit (use space below) to implement this design. Use only SSI gates.

(4%) c) Which (if any) of the $Z_i$ outputs are true for each of the following? Choose the normal (matching) activation-levels for the inputs and outputs (as you did in your MSI labs).

1) $X_3X_2X_1X_0 = 0001$
2) $X_3X_2X_1X_0 = 0000$
3) $X_3X_2X_1X_0 = 1000$
4) $X_3X_2X_1X_0 = 1011$
11. Complete the timing diagram for the below JK-Flip flop with asynchronous clear and synchronous set.

[6%] 7 min