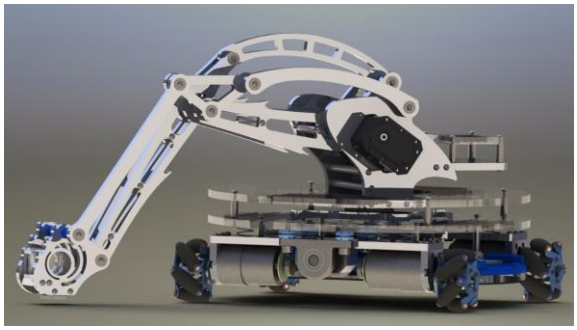
Exam 1

Last Name, First Name

May the Schwartz be with you!

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **12** distinct pages. Sign your name and add the date below.*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*



UF IEEE's SoutheastCon 2015 robot for Hardware Competition

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME

Regrade comments below: Give page # and problem # and reason for the petition.

Pages	Available	Points
2-3	14	
4	3	
5	13	
6	7	
7	13	
8	12	
9	11	
10	11	
11-12	16	
TOTAL	100	

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[14%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 567_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 3 min b) Determine the **12-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -567_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(1%) 1 min c) What is -8_{10} in **4-bit** 2's complement? (Hint: $2^3 = 8$.) You must **show all work.**

$(-8)_{2\ 4\text{-bit}\ 2\text{'s comp}}$: _____

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(2%) 1. c) What is $-2048_{10} - 567_{10}$ in **12-bit** 2's complement? (Hint: $2^{11} = 2048$.) You must use binary numbers to **derive** and determine the solution (not decimal). You must **show all work.**

3 min

$(-2048_{10} - 567_{10})_{2\ 12\text{-bit 2's comp}}$: _____

(2%) 1. d) What is $1024_{10} - 567_{10}$ in **12-bit** 2's complement? ? (Hint: $2^{10} = 1024$.) You must use binary numbers to **derive** and determine the solution (not decimal). You must **show all work.**

3 min

$(1024_{10} - 567_{10})_{2\ 12\text{-bit 2's comp}}$: _____

(2%) 1. e) Perform the requested operations in binary. Show 4 digits after the binary point and 1 digit after the hex point. What is the answer in both **binary** and **hex**?

4 min

1101.11 ÷ 100

Quotient = _____

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[3%] 5 min

2. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. Show all steps. Give the solution in MSOP form.

$$Ga = \overline{\left(T + \overline{O} + R\right)} * \overline{\left(\overline{T} + \overline{S}OR\right)}$$

$Ga =$ _____

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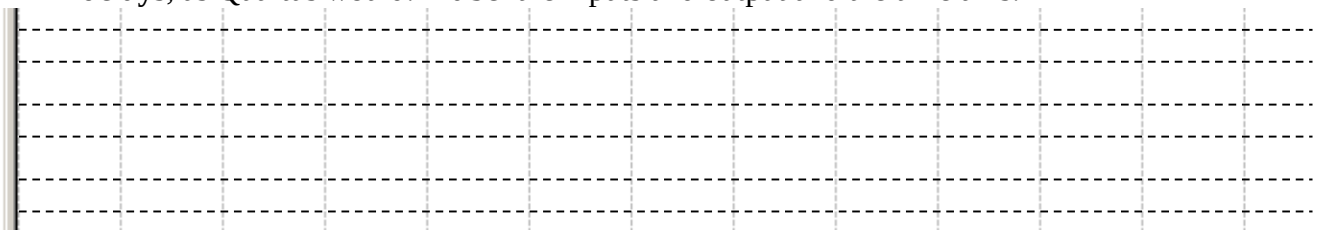
[13%] 3. Answer the following questions.

(3%) 4 min

a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation Y = /(A + /B) with A(H), B(L), Y(H) using the **minimum number** of gates.

(3%) 3 min

b) Draw a **complete** timing diagram, exactly as Quartus would; **include 10ns propagation delays**, as Quartus would. **Label** the inputs and output and the time axis.

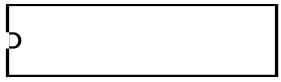


(4%) 2 min

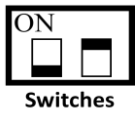
c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(3%) 5 min

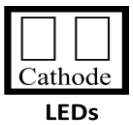
d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part b**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.



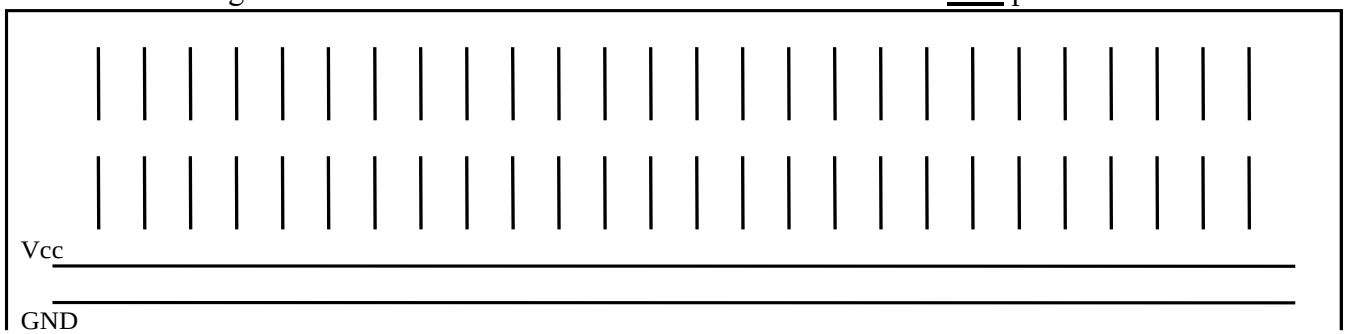
14-pin Chip



Switches



LEDs



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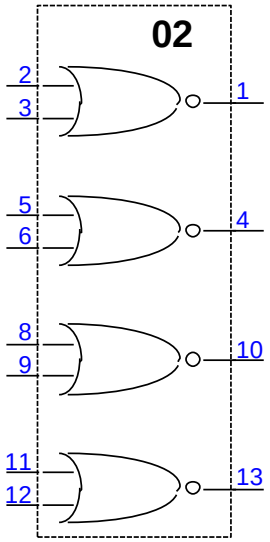
[7%] 5 min

4. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of 74HC02 chips (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for all signals except that **Gat** (the output) must be **active-low**. Label the parts and pin **numbers** for your circuit design.



$$Gat = \overline{\left(\left\{\overline{[(O + \bar{R}) * \bar{G}]} + \bar{R}\right\} * \overline{[O * \bar{W}]}\right) + L}$$

O( )

R( )___

G( )___ ____Gat(L)

R( )___

O( )___

W( )___

L( )___

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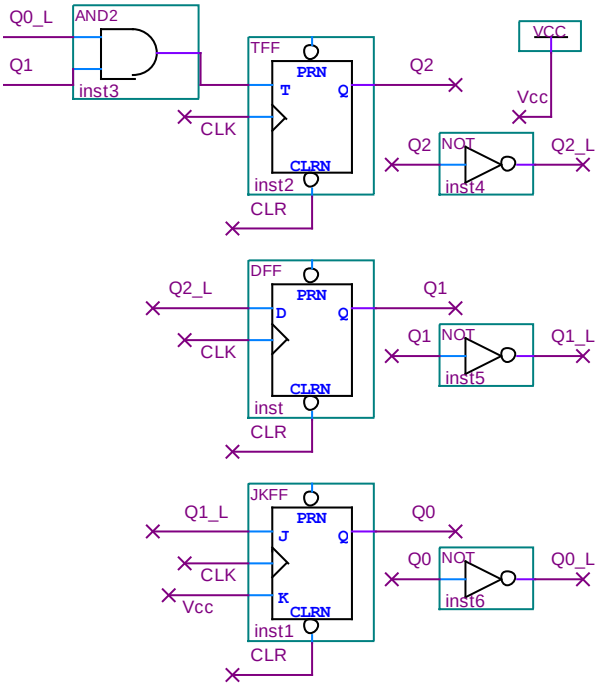
[5%] 5. Use **only** open-collector gates (of any **real** SSI-type gate) to directly implement the below equation. (Do **NOT** simply the equation.) **Show your work!** *M* must be active-high and *U* must be active-low, but you may chose all other activation levels.

4 min

$$Beat = (M + \bar{I} + \bar{Z}) * \overline{(Z + \bar{O} + U)}$$

[8%] 6. Determine the sequence of outputs, for Q_2(H), Q_1(H), and Q_0(H), starting at $Q_2Q_1Q_0$=000. Assume the asynchronous clear, CLR(L), is false and a series of clocks (CLK) occur to create the sequence of outputs. Show **ALL** work. List the next **7 values** in the sequence.

7 min



Sequence = _____

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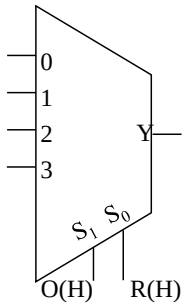
[12%] 7. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The four below problems are **independent**.)

2 min

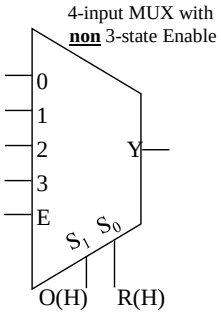
3 min

(3%) a) **Gog_0 = A*/T (O + /R /S + /O S)**



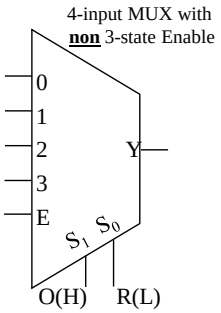
3 min

(3%) b) **Gog_1 = A*/T (O + /R /S + /O S)** (Note the **enable**.)



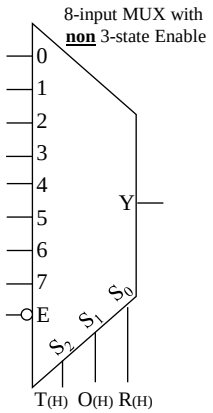
3 min

(3%) c) **Gog_2 = A*/T (O + /R /S + /O S)** (Note the **enable**.)



(3%) d) **Gog_3 = A*/T (O + /R /S + /O S)** (Note the mux **size** and **enable**)

3 min



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[11%] 8. Solve the following Karnaugh Map Boolean Algebraic simplifications problems.

(6%) 8 min a) Simply the below equation and put the result in MSOP **and** form MPOS. **Label your circles!**

$$\boldsymbol{Y = (\overline{A} + \overline{B} + \overline{C} + D) * (\overline{A} + B + D) * (A + \overline{B} + \overline{C}) * (A + \overline{C} + D) * (\overline{B} + \overline{C} + \overline{D}) * (A + B + C)}$$

CD
AB

CD
AB

Y_{MSOP} =

Y_{MPOS} =

(4%) 4 min b) If the terms ABCD=1000, 1001, and 1101, i.e., the textbook's d(8,9,13), are **DON'T CAREs (X)**, determine the new MSOP **and** MPOS equations.

CD
AB

CD
AB

Y_{MSOP} =

Y_{MPOS} =

(1%) 2 min c) Are the above equations (in part b) **equivalent**? Why or why not?

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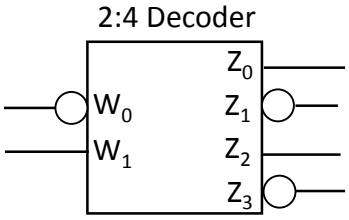
[11%] 9. Solve the below decoder-related problems.

(4%) 5 min

a) Determine the truth table for the below **decoder**. Also create a **functional** block diagram from the given block diagram.



(4%) 6 min

b) Determine the equations for the decoder (use space above). Simplify the equations. Design a circuit (use space below) to implement this design. Use only SSI gates.

(3%) 3 min

c) Add an active-low enable to the above truth table (on the left) and complete the table. (It is not necessary to put this **augmented table** in counting order.). Add to (but do **NOT** modify) the above circuit for the new design. Use the signal names in part b in your design below. Rename the **new** outputs P_3 through P_0.

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[16%] 10. Design the following specified multiplexers.

(4%) 4 min

a) Create a **functional block diagram and then design** a **4-input** multiplexer (with **no enable**). For this design, use only 2-input multiplexers with no enables. **Only** if necessary, you may use SSI parts to complete your design. Use the minimum number of MUXs.

(4%) 4 min

b) Create a **functional block diagram and then design** a **4-input** multiplexer with a **non tri-state enable**. For this design, use only 2-input multiplexers with **non tri-state enables**. (All enables can have any activation-level.) **Only** if necessary, you may use SSI parts to complete your design. Use the minimum number of MUXs.

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(4%) 4 min

10 c) Create a **functional block diagram and then design** a **4-input** multiplexer with **no enable**. For this design, use only 2-input multiplexers **with tri-state enables**. (All enables can have any activation-level.) **Only** if necessary, you may use SSI parts to complete your design. Use the minimum number of MUXs.

(4%) 4 min

d) Create a **functional block diagram and then design** a **4-input** multiplexer with a **tri-state enable**. For this design, use only 2-input multiplexers with **tri-state enables**. (All enables can have any activation-level.) **Only** if necessary, you may use SSI parts to complete your design. Use the minimum number of MUXs.