# Exam 1

*May the Schwartz be with you!*

Last Name, First Name

UF's RobotX concept vehicles.

*Instructions:*

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & $D_3$ before $D_2$).*

***Please read carefully.***

***Good luck & Go Gators!!!***

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (14 Oct 2015) _____

| Regrade comments below: Give page # and problem # and reason for the petition. |
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| Pages | Available | Points |
|---|---|---|
| 2-3 | 16 | |
| 4 | 11 | |
| 5 | 9 | |
| 6 | 15 | |
| 7 | 10 | |
| 8 | 11 | |
| 9 | 10 | |
| 10-11 | 19 | |
| TOTAL | 101 | |

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[11%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $119_{10}$.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 4 min b) Determine the **8-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number $-119_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $82_{10} - 119_{10}$ in 8-bit 2's complement? You must **show all work.**

$(82_{10}-119_{10})_2$: _____

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(2%) 1. d) What is $82_{10} + 119_{10}$ in 8-bit 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). You must **show all work.**

3 min

$(82_{10} + 119_{10})_2$ **8-bit 2's comp**:

[2%] 2. What is the difference in a functional compilation/simulation of a Quartus design and a full compilation/timing simulation?

2 min

[3%] 3. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. Show all steps. Give the solution in MSOP or MPOS form.

5 min

$$Boats = \overline{\left[\overline{\left(A * \overline{\overline{T}} * U\right)} * F\right]} * \overline{(A + \overline{\overline{T}})}$$

***Boats*** =

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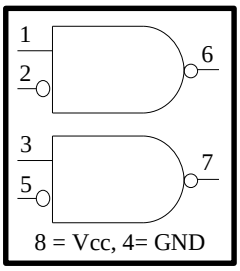
[11%] 4. Use the below circuit for this problem.

**74'Gator**




(4%) 4 min

a) Draw the **mixed-logic circuit** diagram to implement the below two equations using parts from the 74'Gator chip show. (These should be **circuit diagrams,** not layout diagrams.) **Label the pin numbers** on your circuit diagram. A must be active-high, i.e., A(H).

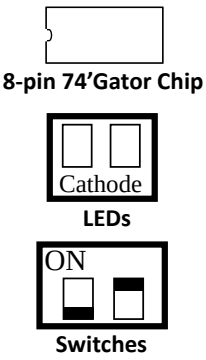
**X = A * B**
**Y = A + B**

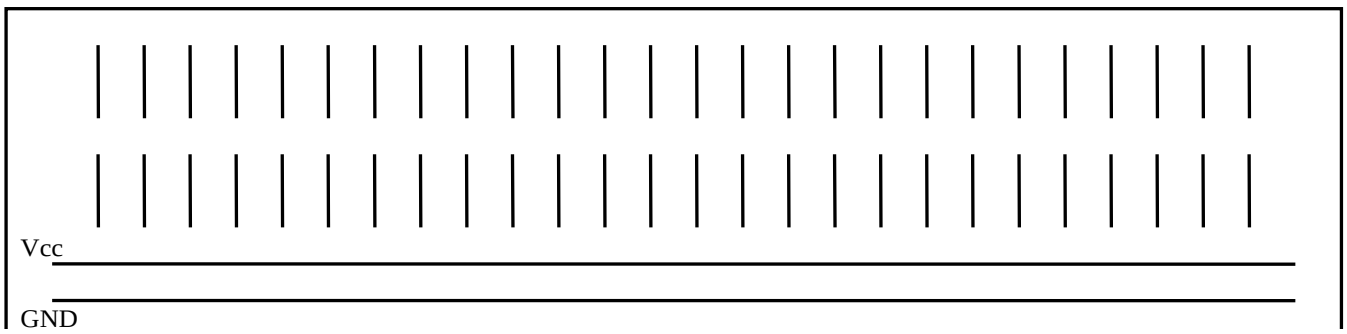
(4%) 2 min

b) Draw the required switch circuits and LED circuits to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(3%) 5 min

c) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** from **part b** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. Label the wires for each of the inputs and outputs (A, B, X, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure to the right are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions. For any other required parts, you may use any size parts that you need.



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[9%] 5. Use only open-collector gates (of any SSI-type gate) to directly implement the below equation. (Do **NOT** simply the equations.) **Show your work!**

(5%) a) $Y = \overline{(\bar{A} * B)} + (C + \bar{D})$

5 min

(2%) b) $Y = \overline{\overline{(\bar{A} * B)} + (C + \bar{D})}$

2 min

(2%) c) $Y = \overline{\overline{(\bar{A} * B)} + (C + \bar{D})} * E$

2 min

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[7%] 5 min

6. Directly implement the below equation with a mixed-logic circuit diagram. Use **only one type** of SSI gate, i.e., use as many of the **SAME** chips as needed (but with a minimum number of gates). Use the appropriate mixed-logic symbols. Pick whatever activation levels you want for the inputs and output, except **S** and **U** must be **active-high**.

$$Go = \overline{(\bar{S} * \bar{U} + B) + \overline{(T * \bar{E})} * (A + M)}$$

S(H)___

U(H)___

B( )

T( )___ ___Go( )

E( )___

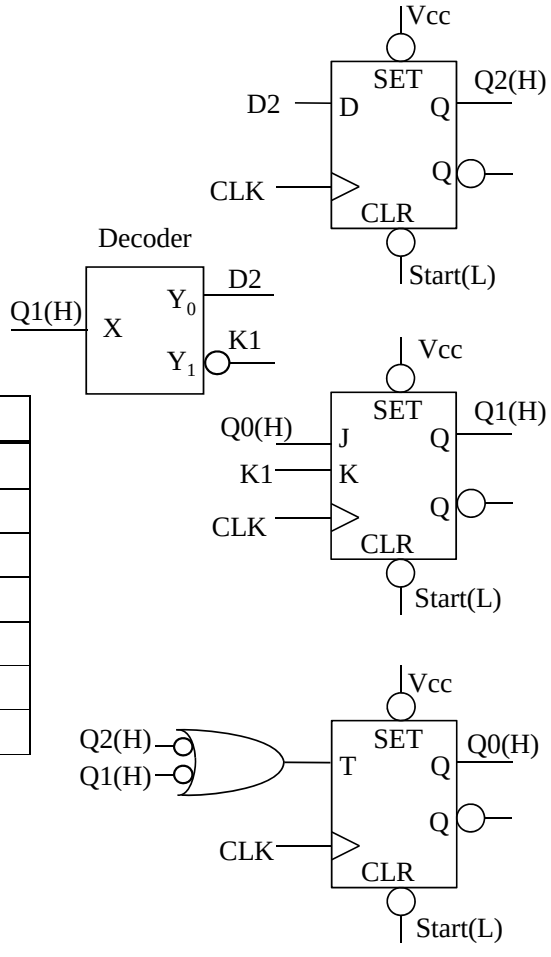
A( )___

M( )___

[8%] 12 min

7. Consider the below circuit with inputs CLK and Start(L), and active-high outputs $Q_2$ $Q_1$ $Q_0$. Determine the sequence of output $Q_2$ $Q_1$ $Q_0$ for a sequence of 6 clock (CLK) pulses. (The columns to the right are for your use if you need them.) Assume that Start(L) is true to initialize the circuit (for the first row) and then Start(L) is false for the next 6 clock pulses.

| # | Q2 | Q1 | Q0 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | |
| 1 | | | | | | | | | | | |
| 2 | | | | | | | | | | | |
| 3 | | | | | | | | | | | |
| 4 | | | | | | | | | | | |
| 5 | | | | | | | | | | | |
| 6 | | | | | | | | | | | |



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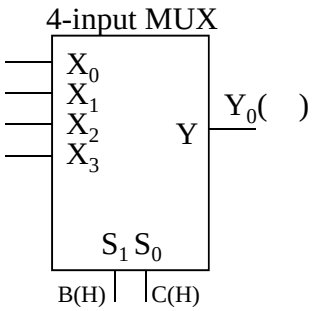
[10%] 8. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The four below problems are **independent**.)

2 min

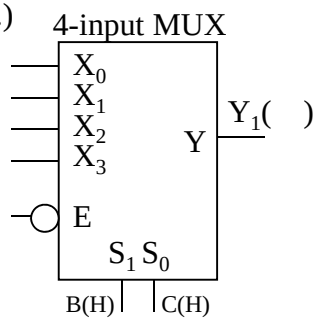
( %) a) **$Y_0$ = (A+B+/D)*(A+/C)*(B+C)*D**

3 min



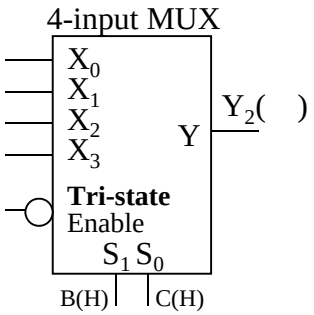

( %) b) **$Y_1$ = (A+B+/D)*(A+/C)*(B+C)*D** (Note the **NON** tri-state enable.)

3 min



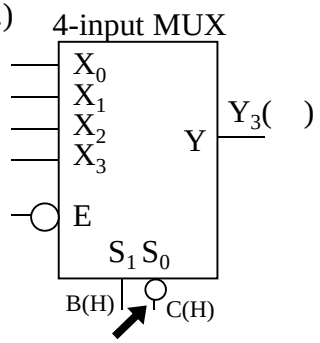

( %) c) **$Y_2$ = (A+B+/D)*(A+/C)*(B+C)*D** (Note the **tri-state** enable.)

3 min




( %) d) **$Y_3$ = (A+B+/D)*(A+/C)*(B+C)*D** (Note the **NON** tri-state enable.)

3 min



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[11%] 9. Use the below equation for this problem.

$$Y = (\bar{A} + \bar{B} + D) * (\bar{A} + B + \bar{C}) * (\bar{A} + B + \bar{D}) * (A + \bar{B} + C + D) * (A + B + \bar{C}) * (A + \bar{C} + D)$$

(7%) 8 min a) Simply the above equation and put the result in MPOS **and** MSOP form. Are the solutions equivalent? Explain why or why not.

AB
CD

AB
CD

$Y_{MPOS}$ =

$Y_{MSOP}$ =

Equivalent?:

(3%) 3 min b) If the term ABCD=0100, i.e., the textbook's d(4), is a **DON'T CARE (X)**, determine the new MPOS and MSOP equations. Are the solutions equivalent? Explain why or why not.

AB
CD

AB
CD

(1%) 1 min c) Are the above equations (in part b) **equivalent**? Why or why not?

$Y_{MPOS}$ =

$Y_{MSOP}$ =

Equivalent?:

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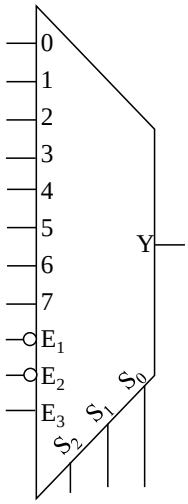
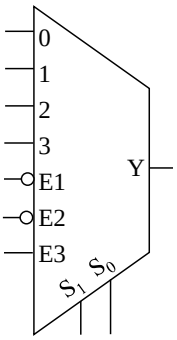
[10%] 10. Design the following multiplexers.

(6%) 5 min

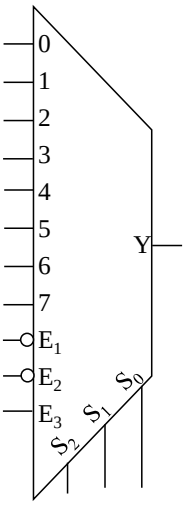
a) Design an **11-input MUX** with a **NON** tri-state enable using only MUXes of the two types given. Use the minimum number of required MUXes (but you can use more than one of each, if necessary). Use **nothing** else! For this problem, assume that the MUX enables are all **NON tri-state enables**. Note that all enables must be true for a MUX to be enabled.

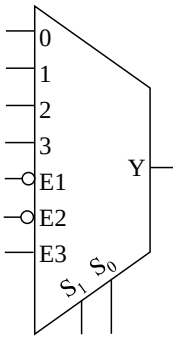



(4%) 4 min

b) Design an 11-input MUX with a **tri-state** enable using only MUXes of the two types given. Use the minimum number of required MUXes (but you can use more than one of each if necessary). Use **nothing** else! For this problem, assume that the MUX enables are all **tri-state enables**. Note that all enables must be true for a MUX to be enabled.



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[10%] 11. A 2-to-4 decoder has inputs A and B and outputs labeled $X_0$, $X_1$, $X_2$, and $X_3$.

(3%) 5 min

a) Describe an experiment to determine the proper names for A and B (and then suggest **proper names** for these two inputs). Draw a block diagram (below right) of the solution.

(b+c=5%) 4 min

b) Give the equations for each of the $X_i$ outputs as a function of the **new** input signal **names**.

(b+c=5%) 3 min

c) If one of the inputs and $X_3$ and $X_0$ are active-high the other input and $X_2$ and $X_1$ is active-low, design a complete mixed-logic circuit diagram for this decoder. Use your new input signal names. Use a **minimum number** of gates; only SSI devices are allowed.

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(2%) 2 min 11. d) If the decoder has an active-low (**non** tri-state) enable, write a new equation and design a new circuit for **only** $X_3$. Use a minimum number of gates; only SSI devices are allowed.

[9%] 12. In this **NEW** problem (**not** related to the prior problem), you will design a 3-to-6 decoder.

(5%) 5 min a) Design a 3-to-6 decoder (with no enable) using a 2-to-4 decoder (with a non tri-state enable) and as many 1-to-2 decoders (each with a non tri-state enable) as necessary. Assume that the decoders have **active-high** inputs and outputs, except that the enable can have **any activation** level that you desire. Use no other parts, if possible, and the minimum number of 1-to-2 decoders.

a)

**Part a design**

**Part b design (modifications)**

(4%) 4 min b) Modify (or redesign) the above design to give the 3-to-6 decoder an **active-low enable**. Use a minimum number of gates for the modification, but use only SSI gates or more 1-to-2 decoders. Either draw a new solution or draw arrows and modify your old solution (keeping the original solution for part a clear as well).