Exam 1

Last Name, First Name _____

May the Schwartz be with you!

UF's NaviGator at Lake Wauburg.

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (13 Oct 2016)

Regrade comments below: Give page # and problem # and reason for the petition.

Pages	Available	Points
2-3	15	
4	12	
5	13	
6-7	19	
8	10	
9	13	
10-11	18	
TOTAL	100	

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[13%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 337_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 4 min b) Determine the **10-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -337_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $256_{10} + 337_{10}$ in 10-bit 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $256 = 2^8$. You must **show all work.**

$(256_{10} + 337_{10})_2$ **10-bit 2's comp**: _____

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(2%) 1. d) What is $256_{10} - 337_{10}$ in 10-bit 2's complement? You must **show <u>all</u> work.**

3 min

$(256_{10}\text{-}337_{10})_2$ **10-bit 2's comp**: _____

(2%) e) What is $1011\ 1001_2 \div 010_2$ You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Show at least two digits to the right of the binary point. You must **show <u>all</u> work.**

4 min

Answer: _____

[2%] 2. What must you do to an active-low input in Quartus so that it understands that the signal is active-low? What about an active-low output?

2 min

_____

_____

_____

_____

_____

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[4%] 5 min

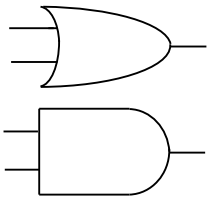
3. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. Show all steps. Give the solution in MSOP or MPOS form.

$$Tebow = \left[\overline{\left(\bar{G} + \bar{A} * T\right)} * O * \bar{R}\right] * \overline{\left(\bar{G} + \overline{\bar{R} * A} + T\right)}$$

Tebow = _____

[8%] 6 min

4. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. Use only real (as specified in class) gates, but you can **NOT** use OR gates or AND gates (or their equivalents). Minimize the total number of gates. Pick whatever activation levels you want for the signals not already specified.



74'32 OR and
74'08 AND gates
NOT allowed

$$UF = \overline{\left(\overline{B + E * \bar{A} * \bar{T}}\right) + \overline{\left(M + \overline{I * \bar{Z}}\right)}}$$

B(H)___

E(L)___

A( )___

T( )___ _____UF( )

M( )___

I( )____

Z(L)____

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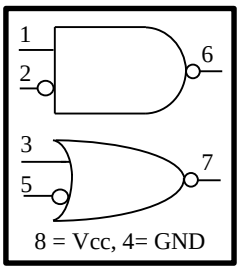
[13%] 5. Use the below circuit for this problem.

74'UF



(6%) 4 min

a) Draw the **mixed-logic circuit** diagram to directly implement the below two equations using parts from the 74'UF chip show. (These should be **circuit diagrams,** not layout diagrams.) **Label the pin numbers** on your circuit diagram. X must be active-high, i.e., X(H).

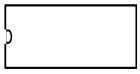
$$X = A * B$$
$$Y = \overline{A + B}$$

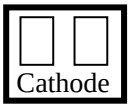
(4%) 2 min

b) Draw the required switch circuits and LED circuits to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

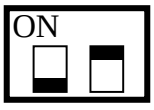
(3%) 5 min

c) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** from **part b** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. Label the wires for each of the inputs and outputs (A, B, X, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure to the right are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions. For any other required parts, you may use any size parts that you need.

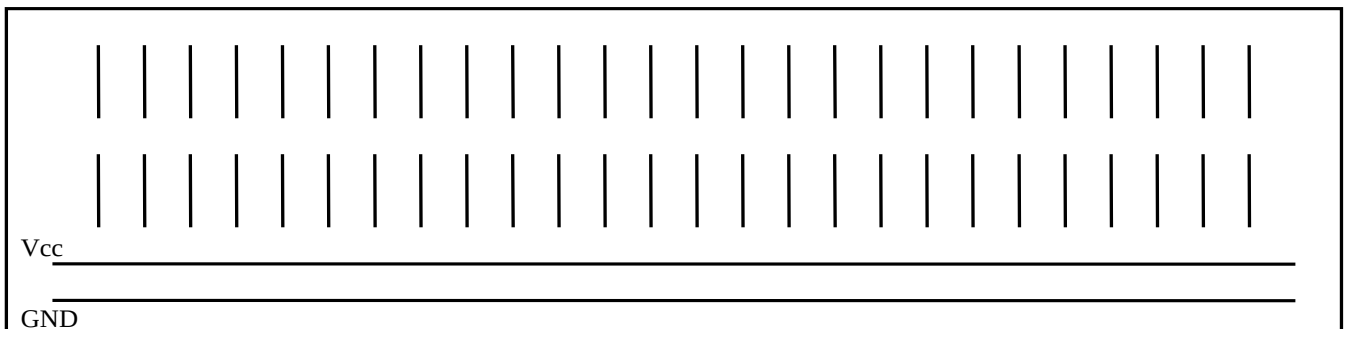

8-pin 74'UF Chip



LEDs



Switches



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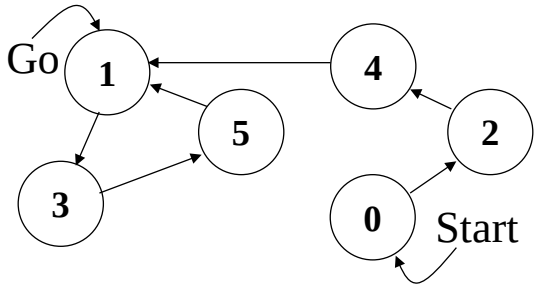


[19%] 6. Design a system that "counts" as shown. The system must **asynchronously** go to state "0" when **Start** (**active-low**) goes true and go to state "1" when **Go** (**active-high**) goes true. Assume that both Start and Go will never be simultaneously true. Use a **D-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and T-FF(s) for **any other** bits you might need. An **active-low** output, **Home** should be true in states "4" and "5." All other outputs should be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.

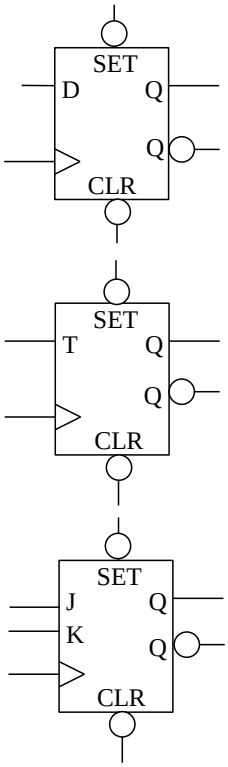
3 min

( ) a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

4 min

Inputs

Outputs



6 min

( ) b) Complete the next-state **truth** table (**in counting order**).

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( ) 6. c) Find the required **simplified** (MSOP or MPOS) equations.

6 min

( )

5 min

d) Design the complete circuit, **minimizing** the total number of components, but using the D-FF, JK-FF(s), and T-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronous** go to state "0" when **Start** (**active-low**) goes true and go to state "1" when **Go** (**active-high**) goes true. Assume that both Start and Go will never be simultaneously true.

Inputs

Outputs

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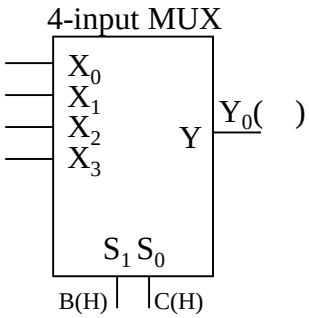
[10%] 7. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The four below problems are **independent**.)

2 min

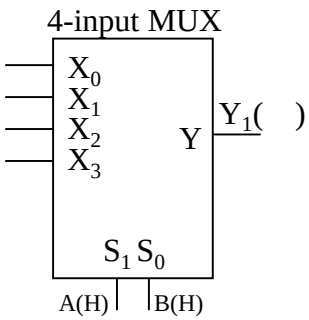
(%) a) **Y_0 = (A+/B) (/B +C) /C D**

5 min



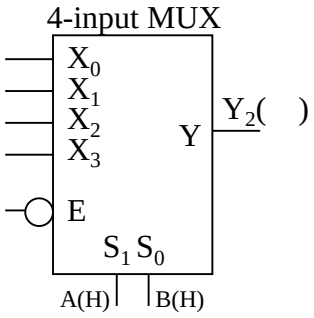
(%) b) **Y_1 = (A+/B) (/B +C) /C D**

3 min



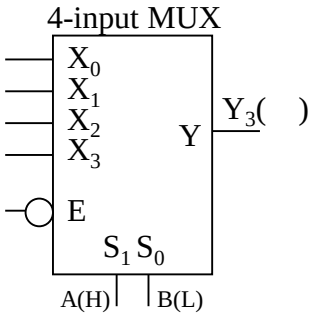
(%) c) **Y_2 = (A+/B) (/B +C) /C D** (Note the **NON** tri-state enable.)

3 min



(%) c) **Y_3 = (A+/B) (/B +C) /C D** (Note the **NON** tri-state enable.)

3 min



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[13%] 8. Use the below equation for this problem.

$$Y = (\bar{A} + B + \bar{C} + D)(A + \bar{C} + \bar{D}) * (\bar{A} + C + D) * (A + \bar{C} + D) * (\bar{B} + C + D) * (A + C + D)$$

(9%) a) Simply the above equation and put the result in MPOS **and** MSOP form.

8 min

AB
CD

AB
CD

Y_{MPOS} =

Y_{MSOP} =

(3%) b) If the terms ABCD=0001 and 1011, i.e., the textbook's d(1) and d(11), are **DON'T CARE (X)**, determine the new MPOS and MSOP equations

3 min

AB
CD

AB
CD

Y_{MPOS} =

Y_{MSOP} =

(1%) c) Are the above equations (in part b) **equivalent**? Why or why not?

1 min

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[18%] 9. Design the following decoders.

(6%) 7 min

a) Draw a functional block diagram, make a truth table, determine the equations, and then create a circuit design for a **1-to-2 Decoder**. Use only the minimum number of SSI gates. All inputs and outputs are active-high. Label inputs as Xi and outputs labeled Yj, where i and j are numbers (as done in class).

(4%) 4 min

b) Design a 1-to-2 Decoder with **two enables**, **E_0(H)** and **E_1(L)**. Use all the same steps of the design as in part a.

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(4%) 9. c) Design a **2-to-4 Decoder** with **one enable**, **E(H)**, using the minimum number of **1-to-2 Decoders** (from part b), as necessary, and the minimum number of additional SSI gates, as necessary. Do **NOT** draw the SSI gates that make up the **1-to-2 Decoders**; instead use the functional block diagram from part b. It is **NOT** necessary (but may be helpful) to go through each of the steps described in part a, but you must draw the functional block diagram along with the final circuit diagram.

5 min

(4%) d) Design a **3-to-8 Decoder** with **no enables**, using only **2-to-4 Decoders** of part c and SSI gates, if necessary. It is **NOT** necessary (but may be helpful) to go through each of the steps dfescribed in part a, but you must draw the functional block diagram along with the final circuit diagram.

4 min