University of Florida
Department of Electrical & Computer Engineering

EEL 3701—Spring 2018
Thursday, 1 March 2018

Dr. Eric. M. Schwartz



# Exam 1

*May the Schwartz be with you!*

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Last Name, First Name

*Instructions:*

- *Turn off all* ***cell phones*** *and other* ***noise making devices*** *and put away* ***all electronics****.*
- *Show* ***all*** *work on the* ***front*** *of the test papers.* ***Box*** *each answer. If you need more room, make a clearly indicated note on the front of the page, "****MORE ON BACK****", and use the back. The back of the page will* ***not*** *be graded without an indication on the front.*
- *You may not use any notes, HW, labs, other books, scratch paper, or calculators.*
- *This exam counts for* ***20****% of your total course grade.*
- *Read each question* ***carefully*** *and* ***follow the instructions****.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY*** *write your name at the top of* ***this*** *test page (and, if you remove the staple, all others). Be sure your exam consists of* ***13*** *distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *For anything undefined, if necessary, state a reasonable assumption.*
- *Failure to follow the below rules will result in* ***NO*** *partial credit*
  - *The* ***base*** *(radix) of all number should be indicated with a* ***subscript*** *or* ***prefix****.*
  - *Truth tables, voltage tables, and timing simulations must be in* ***counting*** *order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of* ***each*** *gate with the appropriate logic equations.*
  - *For K-maps, label* ***each*** *grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they* ***MUST*** *be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must* ***not*** *be used as replacements for circuit elements.*
  - *Boolean expression answers must be in* ***lexical order****, (i.e., /A before A, A before B, &* $D_3$ *before* $D_2$*).*


SubjuGator T-shirt in 2009.

***Please read carefully.***

3701 pun to get your mind primed before the exam (fill in the blank):
- Describe the 10 types of people in the world.

______________________________

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

______________________________
SIGN YOUR NAME

______________________________
DATE (1 March 2018)

| Regrade comments below: Give page # and problem # and reason for the petition. |
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| Pages | Available | Points |
|---|---|---|
| 2-3 | 15 | |
| 4 | 9 | |
| 5 | 8 | |
| 6 | 11 | |
| 7-9 | 19 | |
| 10 | 9 | |
| 11 | 11 | |
| 12-13 | 18 | |
| TOTAL | 100 | |

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[15%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min

a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $307_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: ____________________

Octal: ____________________

Hex: ____________________

BCD: ____________________

(3%) 4 min

b) Determine the **11-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number $-307_{10}$. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: ________________

1's Comp: ________________

2's Comp: ________________

(2%) 3 min

c) What is $512_{10}$ - $307_{10}$ in **11-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $512 = 2^9$. You must **show all work.**

$(512_{10} - 307_{10})_{2\ \text{11-bit 2's comp}}$: ____________________

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(2%) 3 min 1. d) What is $128_{10} - 307_{10}$ in **11-bit** 2's complement? Hint: $128 = 2^7$. You must **show <u>all</u> work.**

$(128_{10} - 307_{10})_{2\ \text{11-bit 2's comp}}$: ____________________

(2%) 2 min e) What is $-307_{10}$ in **<u>10-bit</u> 2's complement <u>and</u>** also in **<u>12-bit</u> 2's complement**? You must **show <u>all</u> work.**

$-307_2$ **10-bit 2's comp** ____________________

$-307_2$ **12-bit 2's comp** ____________________

[2%] 2 min 2. What must you do to an active-low input in Quartus so that it understands that the signal is active-low? What about an active-low output?

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[9%] 3. Use the below circuit for this problem.

(5%) 4 min

a) Draw the **mixed-logic circuit** diagram to directly implement these two equations with the **minimum number of gates**. (These should be **circuit diagrams,** not layout diagrams.) The A input and X output, must be active-low, i.e., A(L) and X(L). Y must be active-high, i.e., Y(H). Choose the optimal (best) activation-level for B.

$$X = A * \bar{\bar{B}}$$
$$Y = \overline{A + \bar{\bar{B}}}$$

(4%) 3 min

b) Draw the required switch circuits and LED circuits to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **<u>true</u>** positions.

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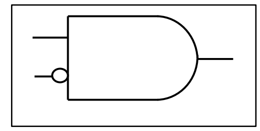
[8%] 4. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. A strange new chip with gates like the one shown are the only ones available for this problem. Use only these gates (or their equivalents). Minimize the total number of gates. Pick whatever activation levels you want for the signals not already specified.

7 min



$$UF = \overline{\left(\overline{\bar{B} * E} + A * \bar{T}\right) + \overline{\left(C + \overline{\overline{A * T} + S}\right)}}$$

B( )___

E(L)___

A(H)___

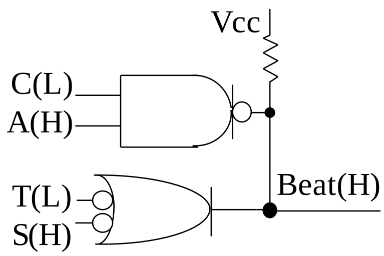
T( )___ __UF(H)

C( )___

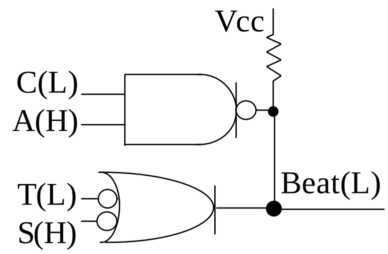
S( )___

[6%] 5. What are the MSOP or MPOS equations for the following circuits? Please look at each circuit carefully.

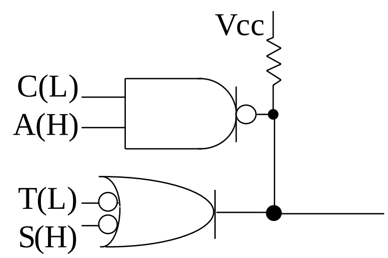
(2%) 4 min a)




(2%) 4 min b)




(2%) 3 min c) Take the result of either of the above circuits (shown again here) and AND it with Go * Gators, i.e., the "new Beat" output is the "above Beat"*Go*Gators. Use a minimum number of additional 2-input open-collector components and **no other parts**.




[5%] 6. Answer the below questions related to switch bouncing.

(2%) 3 min a) Draw a timing diagram, $V = f(t)$, where $V$ is the voltage and $t$ is the time, for a normal (SPST) switch circuit going from open to closed. Include bouncing in the diagram. Label your axes in the diagram with appropriate numerical values.

(3%) 4 min b) Design a debounced switch circuit. Do not use any MSI gates. Label the output as CLK.

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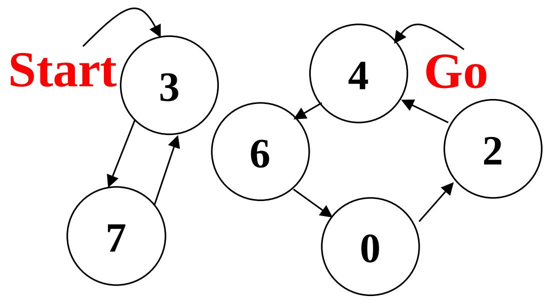
[19%] 7. Design a system that "counts" as shown. The system must **asynchronously** go to state "3" when **Start** (**active-high**) goes true and go to state "4" when **Go** (**active-low**) goes true. Assume that both Start and Go will never be simultaneously true. Use a **T-FF** for the **most** significant bit of your design, a **D-FF** for the **least** significant bit, and **JK-FF**(s) for **any other** bits you might need. An **active-low** output, **Win** should be true in states "6" or "7." All other outputs should be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.

3 min

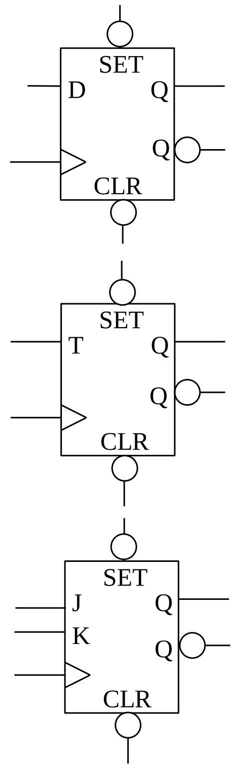



( ) 4 min

a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

Inputs

Outputs



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6 min

( ) 7. b) Complete the next-state **truth** table (**in counting order**).

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( ) c) Find the required **<u>simplified</u>** (MSOP or MPOS) equations.

6 min

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(    ) 6 min

7\. d) Design the complete circuit, **minimizing** the total number of components, but using the D-FF, JK-FF(s), and T-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated** **coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronous** go to state "**3**" when **Start** (**active-high**) goes true and go to state "**4**" when **Go** (**active-low**) goes true. Assume that both Start and Go will never be simultaneously true.

Inputs

Outputs

**Solution for** 3701 pun to get your mind primed before the exam (fill in the blank):

- Describe the 10 types of people in the world.

***The who understand binary, and those who do not! (Need subscript, $10_2$!)***

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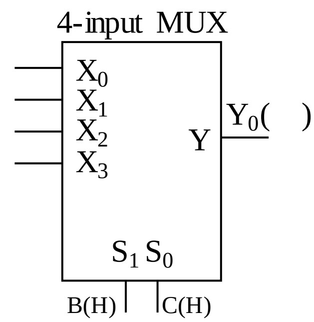
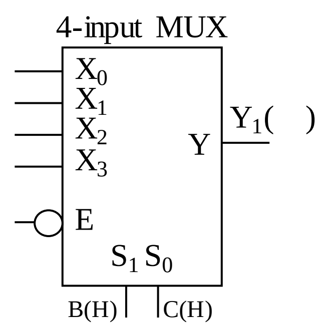
[9%] 2 min 8. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The three below problems are **independent**.)

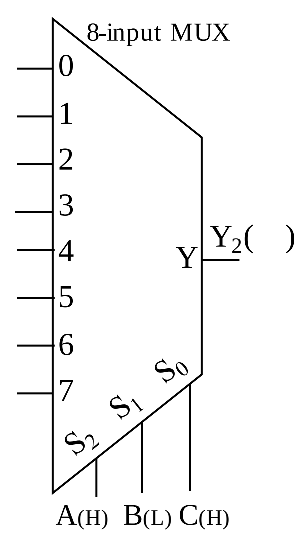
(4%) 5 min a) $\mathbf{Y_0 = (A + /B + C)\ (/A\ D + B)}$




(2%) 2 min b) $\mathbf{Y_1 = (A + /B + C)\ (/A\ D + B)}$ (Note the **NON** tri-state enable.)




(3%) 4 min c) $\mathbf{Y_2 = (A + /B)\ (/B + C)\ /C\ D}$ (**No enable!**)



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[11%] 9. Use the below equation for this problem.

$$Y = \bar{A}\bar{B}\bar{C} + A\bar{B}CD + A\bar{B}\bar{C}\bar{D} + A\bar{B}D + ABCD + A\bar{C}D + \bar{B}C\bar{D}$$

(7%) 8 min a) Simply the above equation and put the result in MPOS **and** MSOP form.

AB
CD

AB
CD

$Y_{MSOP}$ =

$Y_{MPOS}$ =

(3%) 4 min b) If the term ABCD=0011, i.e., the textbook's d(3), are **DON'T CARE (X)**, determine the new MSOP and MPOS equations

AB
CD

AB
CD

$Y_{MSOP}$ =

$Y_{MPOS}$ =

(1%) 1 min c) Are the above equations (in part b) **equivalent**? Why or why not?

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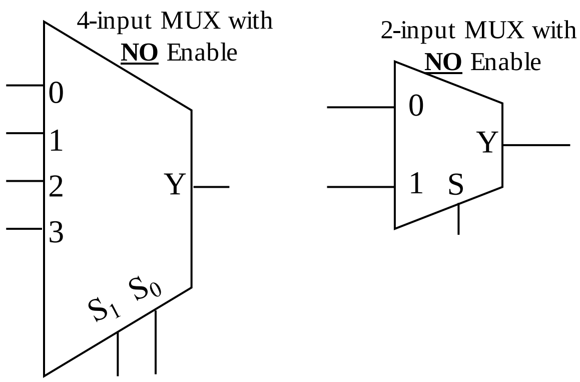
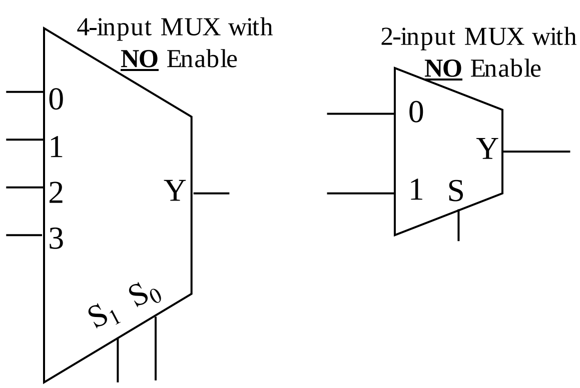
[18%] 10. Design the following multiplexers. The select lines must work as they normally do in selecting the proper MUX inputs.

(4%) 5 min a) Design a **5-input MUX** using **only** the two MUXes below. If possible, use **only one of each** of these two MUXes; if not possible, use a minimum amount **of these parts (but only these MUXes)**; if still not possible, use the minimum number of additional **SSI gates**. The active-high inputs are $X_J$, the active-high select lines are $S_K$, and the active-high output is Y.




(4%) 5 min b) Design a **6-input MUX** using only the two MUXes below. If possible, use **only one of each** of these two MUXes; if not possible, use a minimum amount **of these parts (but only these MUXes)**; if still not possible, use the minimum number of additional **SSI gates**. The active-high inputs are $X_J$, the active-high select lines are $S_K$, and the active-high output is Y.



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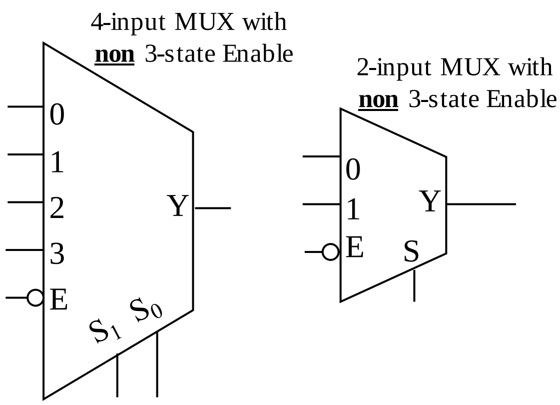
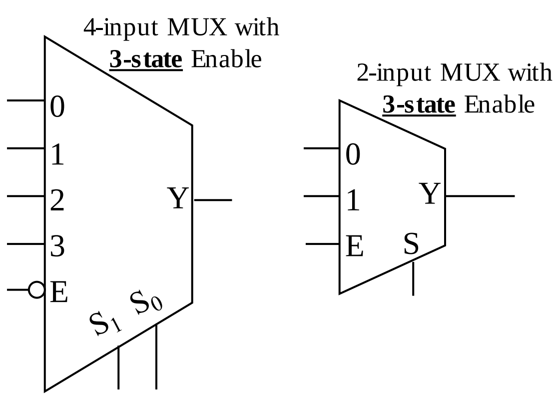
(4%) 5 min 10. c) Design a **6-input MUX** **<u>with</u>** a **<u>non</u> tri-state enable** using only the two MUXes below. If possible, use **only one of each** of these two MUXes; if not possible, use a minimum amount **of these parts (but only these MUXes)**; if still not possible, use the minimum number of additional **SSI gates**. The active-high inputs are $X_J$, the active-high select lines are $S_K$, the active-low **<u>non</u>** tri-state enable is E, and the active-high output is Y.




(4%) 5 min d) Design a **6-input MUX** using only the two MUXes below (both with **tri-state enables**). If possible, use **only one of each** of these two MUXes; if not possible, use a minimum amount **of these parts (but only these MUXes)**; if still not possible, use the minimum number of additional **SSI gates**. The active-high inputs are $X_J$, the active-high select lines are $S_K$, and the active-high output is Y.




(2%) 3 min e) Design an SSI circuit that can transform the design in part d to a **6-input MUX** **<u>with</u>** **<u>tri-state</u> enable**. Describe how it could be connected to the design in part d.