Exam 1

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Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good afternoon! Welcome!

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (1 July 2010)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2-3	19	
4	15	
5	10	
6	9	
7	10	
8	8	
9	11	
10-11	18	
TOTAL	100	

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[15%] 1. Do the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 3 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 55_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>7-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -55_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $60_{10} - 55_{10}$ in **<u>7-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Remember that you must **show <u>all</u> work.**

$(60_{10}–55_{10})_2$: _____

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(3%) 1 d) What is $92_{10} - 55_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

3 min

$(92_{10}–55_{10})_{2\ 8\text{-bit 2's comp}}$: _____

(3%) 1 e) What is $92_{10} + 55_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

3 min

$(92_{10}+55_{10})_{2\ 8\text{-bit 2's comp}}$: _____

[2%] 2. What is the difference in a functional compilation/simulation of a Quartus design and a full compilation/timing simulation?

2 min

_____

_____

_____

_____

_____

[1%] 3. When designing a circuit in Quartus with an active-low output, what special technique is required? Circle one of the below.

1 min

a) Use an inverter b) Nothing special c) Use a bubble d) Both a and c e) None of these

[1%] 4. When designing a circuit in Quartus with an active-low input, what special technique is required? Circle one of the below.

1 min

a) Use an inverter b) Nothing special c) Use a bubble d) Both a and c e) None of these

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[7%] 5. Use a 2-input NAND gate (drawn as a NAND gate) with inputs A(H) and B(L) and output C(H) for this problem.

(2%) a) Draw the mixed-logic circuit diagram. What is the mixed logic equation?

2 min

(2%) b) Draw the truth table and the voltage table (both in **counting order**).

2 min

(3%) c) Draw the Quartus simulation that would **easily** confirm the correct operation of this 2-input NAND gate.

2 min

A

B

C

[8%] 6. Directly implement the below equation with a mixed-logic circuit diagram. Use only one type gate, i.e., use as many of the **SAME** chips as needed (but with a minimum number of gates). Use the appropriate mixed-logic symbols. Pick whatever activation levels you want for the inputs and output, except **S** and **U** must be **active-high**.

5 min

$$Go = \overline{(\bar{S} * \bar{U} + B) + \overline{(T * \bar{E})} * (A + M)}$$

S(H)___

U(H)___

B( )

T( )___ _____Go( )

E( )___

A( )___

M( )___

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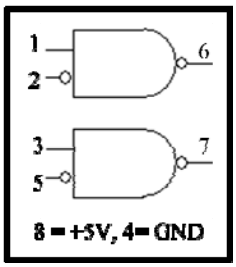
[10%] 7. Use the below circuit for this problem.

74'Gator



(5%) 4 min

a) Draw the **mixed-logic circuit** diagram to implement the below two equations using parts from the 74'Gator chip show. Also draw the required switch circuits and LED circuits. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions. A must be active-high, i.e., A(H).

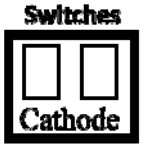
$$X = A * B$$

$$Y = A + B$$

(5%) 5 min

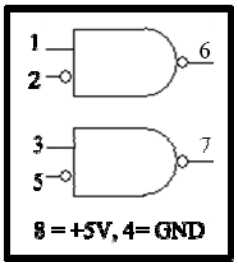
b) Now draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. Label the wires for each of the inputs and outputs (A, B, X and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.

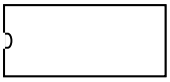
Switches



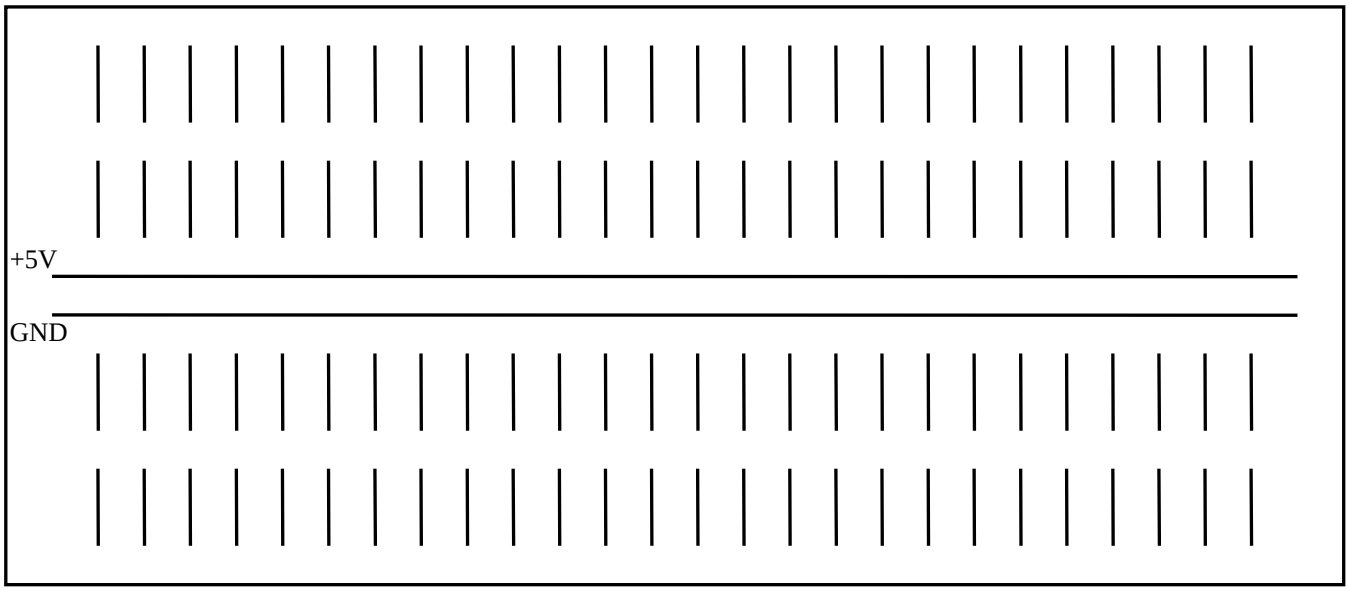
LEDs

74'Gator





8-pin Chip



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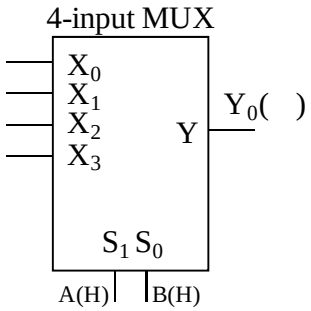
[9%] 8. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal to **minimize** the number of additional parts required. Use the **minimum** number of additional gates. Show all work. (The two below problems are **independent**.)

2 min

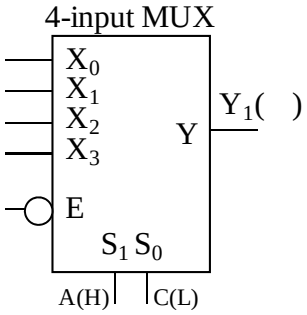
(4%) a) **Y_0 = A*/B + /B*C + /A*/B*D**

3 min



(5%) b) **Y_1 = A*/B + /B*C + /A*/B*D**

4 min



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[4%] 9. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

4 min

$$Y = \overline{(A + \overline{\bar{C} + D})} * \overline{\bar{A} + \overline{\bar{B} * C * D}}$$

Y = _____

[6%] 10. Determine the MSOP **and** MPOS equivalent of the below Boolean expression.

6 min

W = (/A + /C + D)*(A + /B + /C)*(B + C + /D)*(B + D)

W_{MSOP} = _____

W_{MPOS} = _____

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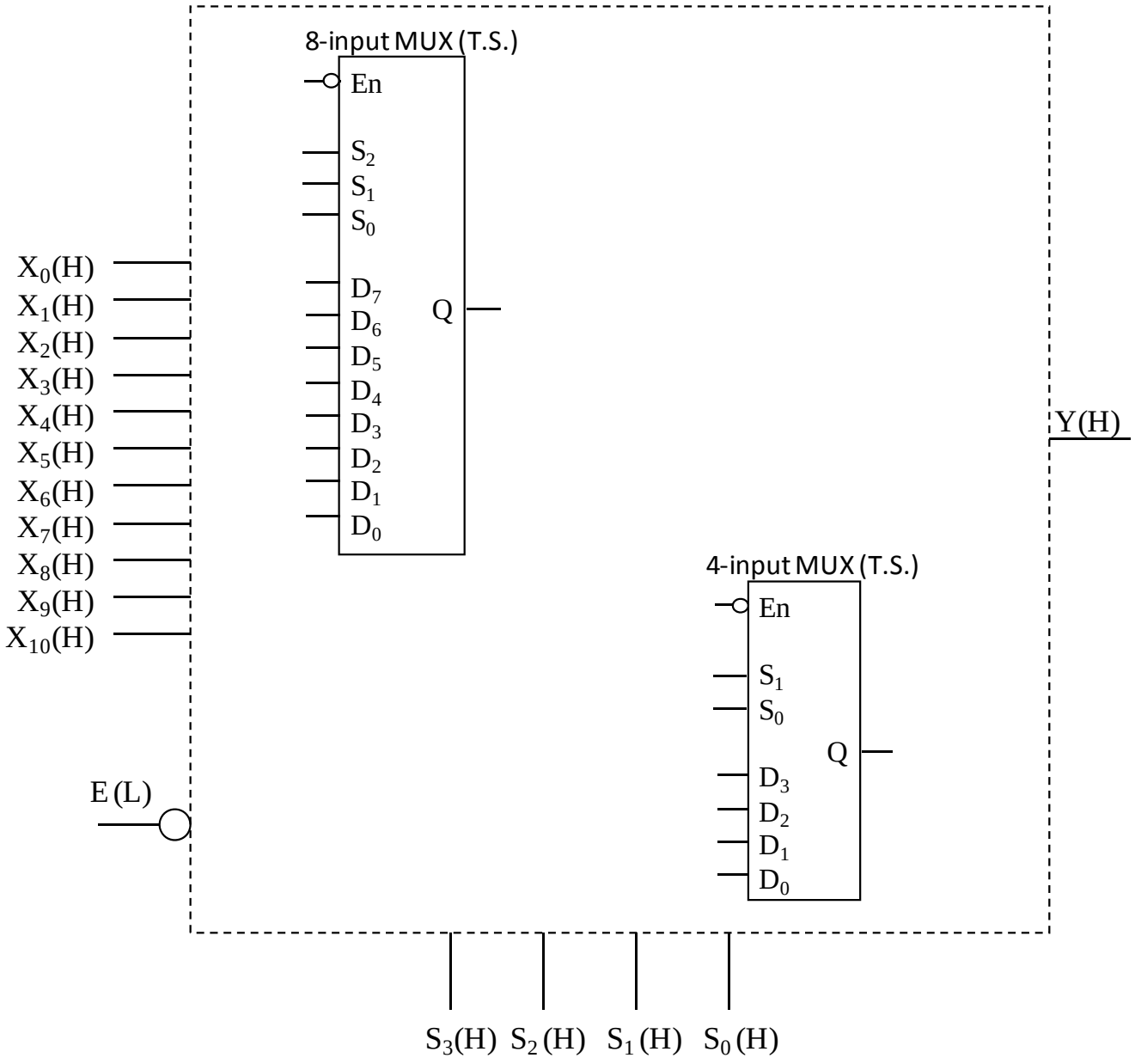
[8%] 8 min

11. Design an 11-input MUX using as many of the given elements as needed. The two given MUXs each have **tri-state** (T.S.) outputs such that if the chip is disabled, the output is tri-stated (high impedance). Note that you need a similar tri-state enable for the 11-input MUX. Use labels instead of wires. First try to minimize number of required components and then minimize the cost. The cost for available single MUXs are: big MUX=37¢ and little MUX=24¢. The cost per single **gates** are Inverter=3¢, 2-input NAND=7¢, and 2-input NOR=13¢. The 11-input MUX must work as expected, e.g., if $S_3S_2S_1S_0$ = j, then Y = X_j, j=0,1,…,10.



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[11%] 12. What is the **logic equation** of each of the following signals **in terms of the given signals**? Put all answers is SOP or POS form in **proper lexical order**. **Show your work!** Reminder: There are **no** activation levels in a logic equation.

(2%) a) $E(L) = f_E(A(L), B(H))$

2 min Answer: E = _____

(4%) b) $G(H) = f_G(C(L), D(H), E(L), F(H))$

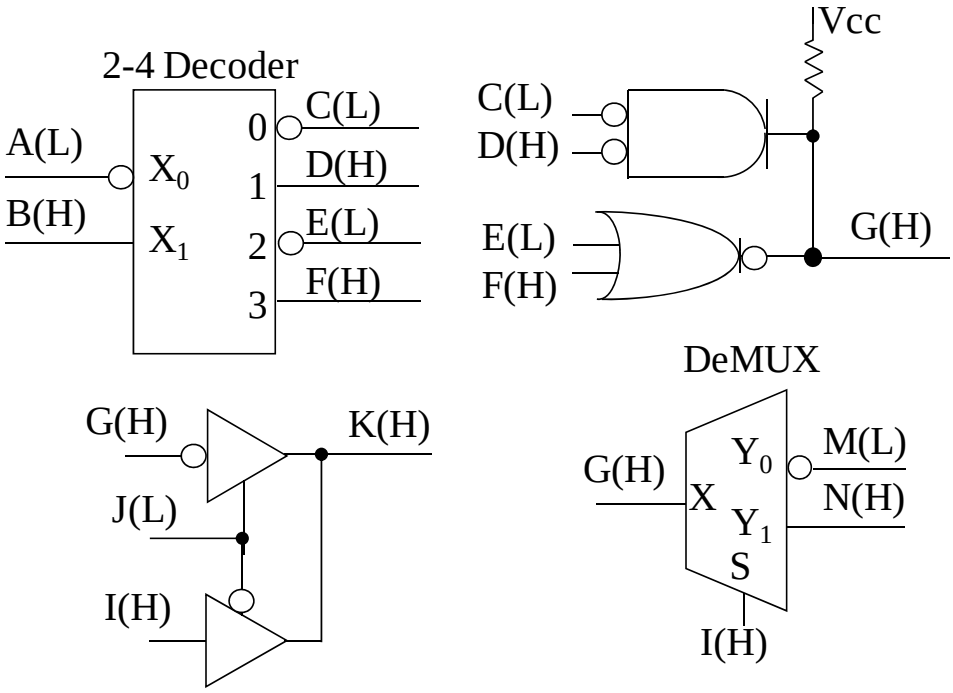
3 min Answer: G = _____

(4%) c) $K(H) = f_K(G(H), J(L), I(H))$

2 min Answer: K = _____

(1%) d) $N(H) = f_N(I(H), G(H))$

2 min Answer: N = _____



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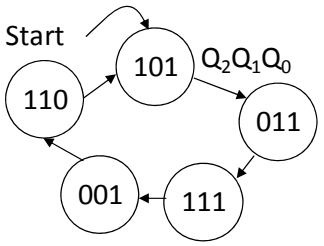
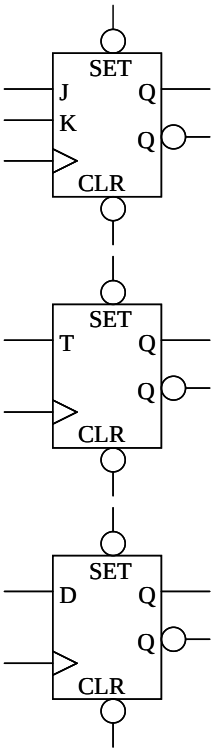
[18%] 13. Design a system that counts as shown. The system must **asynchronously** reset to state "**101**" when **Start** (active-low) goes true. Use a JK-FF for the **most** significant bit of the counter, a D-FF for the **least** significant bit, and a T-FF for **any other** bits you might need. An output **Bad** (active-high), should be true if the count somehow gets to a value that is not in the sequence. Note: All the given FFs have **asynchronous** clear and set inputs.



2 min

(1%) a) Determine the excitation tables for a JK-FF and a T-FF.

3 min



4 min

(6%) b) Complete the next-state **truth** table (**in counting order**).

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(1%) c) Draw a functional **block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in a box with the inputs and outputs going into or out of the box, on the left or right, respectively. This is **not** a circuit diagram.

2 min

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(6%) 13. d) Find the required **simplified** equations. Show **all** work.

6 min

(4%) e) Design the complete counter circuit, **minimizing** the total number of components, but using the JK-FF and D-FF [and T-FF(s), if necessary] as described above. All inputs and outputs of the circuit should be clearly indicated **coming into or out of the** below box. Your design must include the circuitry necessary to re-start the counter to the required $Q_2Q_1Q_0$ = 101 state **asynchronously**, after the **Start(L)** signal goes true. It should also include **Bad(H)**.

5 min