Exam 1

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Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **10** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good afternoon! Welcome!

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____
SIGN YOUR NAME DATE (30 June 2011)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2-3	21	
4	14	
5	14	
6	9	
7	12	
8	12	
9-10	18	
TOTAL	100	

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[21%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 3 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 99_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>7-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -99_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 2 min c) Determine the **<u>8-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -99_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

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(2%) 3 min

1. d) What is $99_{10} + 37_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

$(99_{10}+37_{10})_{2\ 8\text{-bit 2's comp}}$: _____

(3%) 2 min

e) What is $37_{10} - 99_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

$(37_{10}-99_{10})_{2\ 8\text{-bit 2's comp}}$: _____

(3%) 2 min

f) What is $-7_{10} - 99_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

$(-7_{10} - 99_{10})_{2\ 8\text{-bit 2's comp}}$: _____

(3%) 4 min

g) What is $99_{10} \div 7_{10}$ in **unsigned** binary? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.** Determine at least four digits past the binary point.

$(99_{10} \div 7_{10})_{2\ \text{unsigned}}$: _____

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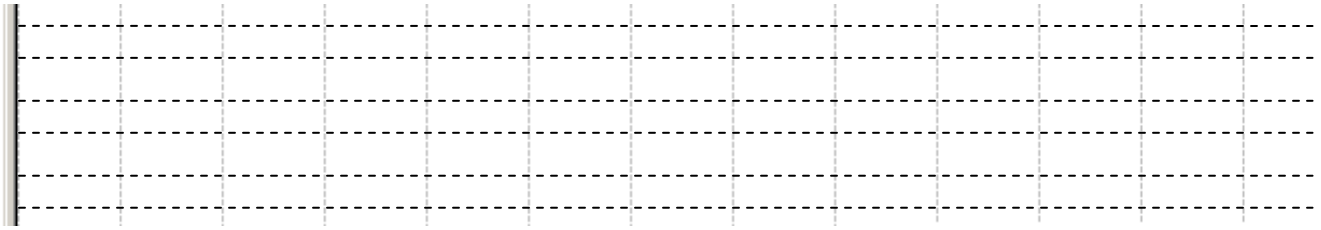
[14%] 2. Answer the following questions.

(3%) 2 min a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation Y = A * /B with A(L), B(H), Y(L) using the **minimum number** of gates.

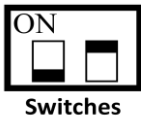
(3%) 3 min b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.



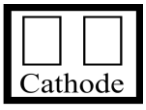
(4%) 2 min c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(4%) 5 min d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want, along with the normal power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.

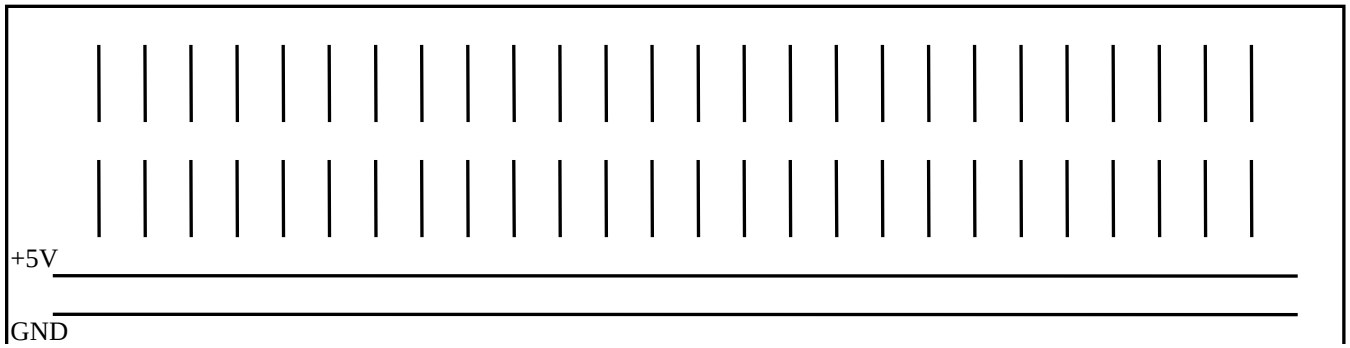
14-pin Chip



Switches



LEDs



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[8%] 5 min

3. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only **2-input** NAND or NOR gates (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. Pick whatever activation levels you want for the unspecified inputs, but **T** must be **active-high** and **M** and **Mow** must be **active-low**.

$$Mow = \overline{\overline{(\bar{T} + \bar{E} + A)} + \left[\overline{(M * \bar{W})} + O\right] * N}$$

T(H)___

E( )___

A( )

M(L)___ _____Mow(L)

W( )___

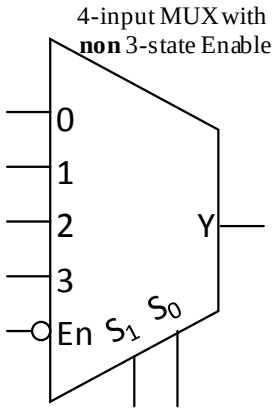
O( )___

N( )___

[6%] 5 min

4. Use the given multiplexer to **design a mixed-logic circuit diagram** for the given equation. Choose activation levels for each signal to **minimize** the number of additional parts required. Use the **minimum** number of additional gates. Show all work.

$$UF = G\bar{R}(A + \bar{T}) + \bar{R}A$$



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[4%] 5. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

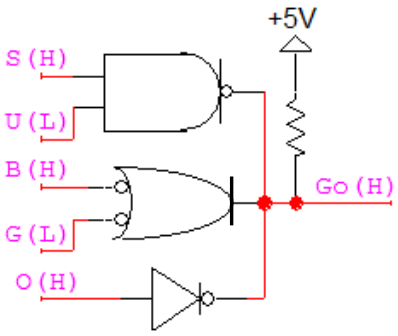
5 min

$$Mow = \overline{\overline{(\bar{M} + \bar{O} + W)} + \left[\overline{(M * \bar{W})} + O\right] * N}$$

Mow = _____

[5%] 6. What is the **logic equation** of the following circuit. Put the solution in SOP or POS form. **Show your work!** Reminder: There are **no** activation levels in a logic equation.

5 min



Go = _____

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[8%] 7. Determine the MSOP **and** MPOS for the truth table given. Are the solutions equivalent? Explain why or why not.

7 min

A	B	C	D	Y
0	0	0	0	X
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	X
1	0	0	1	0
1	0	1	0	X
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Y_{MSOP} = _____

Y_{MPOS} = _____

[4%] 8. Design a debounced switch for use as a clock input. The only **ICs** (chips) that you can use is one **<u>half</u>** of a "OR" chip and one "level shifter" chip. Draw the circuit diagram and label the CLK output.

5 min

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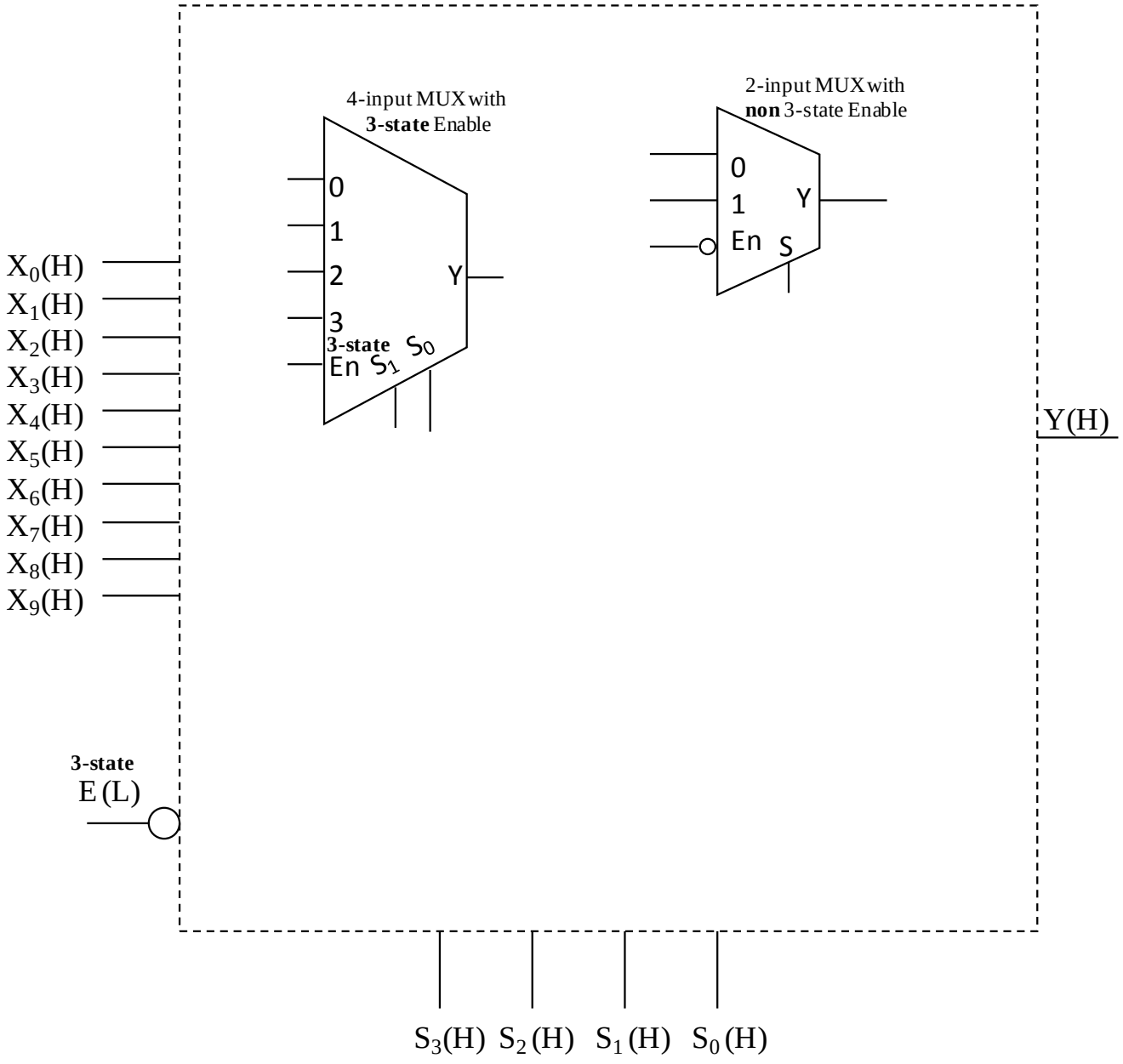
[12%] 9. Design a 10-input MUX using no more than two of each of the given elements. The given 4-input MUX has a **tri-state** output such that if the chip is disabled, the output is tri-stated (high impedance). The 2-input MUX does **not** have a tri-state output. Note that you need a tri-state enable for the 10-input MUX that you are designing. Use labels instead of wires. First try to minimize number of required components and then minimize the cost. The cost for available single MUXs are: 4-input MUX=37¢ and 2-input MUX=24¢. The cost per single **gates** are Inverter=3¢, Tri-state Buffer=5¢, 2-input NAND=7¢, and 2-input NOR=13¢. The 10-input MUX must work as expected, e.g., if $S_3S_2S_1S_0 = j$, then $Y = X_j$, j=0,1,…,9.

12 min



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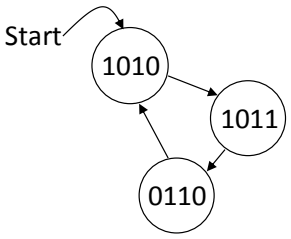
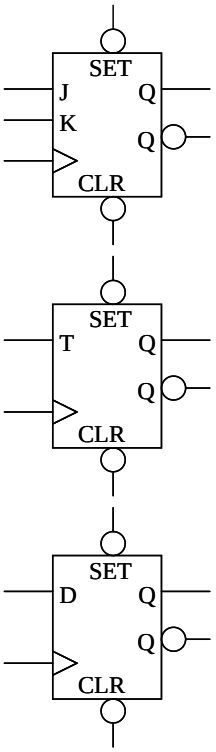
[18%] 10. Design a system that counts as shown. The system must **asynchronously** reset to the state shown when **Start** (**active-low**) goes true. Use a JK-FF for the **most** significant bit of your design, a T-FF for the **least** significant bit, and a D-FF for **any other** bits you might need. Note: All the given FFs have **asynchronous** clear and set inputs.



2 min

(1%) a) Determine the excitation tables for a T-FF and a JK-FF.

3 min



5 min

b) Complete the next-state **truth** table (**in counting order**).

(1%) c) Draw a functional **block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in a box with the inputs and outputs going into or out of the box, on the left or right, respectively. This is **not** a circuit diagram.

2 min

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10. d) Find the required **simplified** (MSOP or MPOS) equations.

6 min

e) Design the complete counter circuit, **minimizing** the total number of components, but using the JK-FF and T-FF [and D-FF(s), if necessary] as described above. All inputs and outputs of the circuit should be clearly indicated **coming into or out of the** below box. Your design must include the circuitry necessary to re-start the counter **asynchronously** after the **Start(L)** signal goes true to the required top state (with 1010). **Add an output circuit** for **GG** (GoGators, **active-low**) that should be true if **Start is false** and the system is in the **top state** (with 1010).

5 min